National Semiconductor

Programmable Array Logic (PAL®) 24-Pin Exclusive-OR PAL Family

General Description

The 24-pin Exclusive-OR PAL family contains four industry-standard PAL architectures optimized for a specific class of applications. National Semiconductor's advanced Schottky TTL process with titanium tungsten fusible links provides high-speed user-programmable replacements for conventional SSI/MSI logic with significant chip-count reduction.

Programmable logic devices provide convenient solutions for a wide variety of application-specific functions, including random logic, custom decoders, state machines, etc. By programming fusible links to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products. A large variety of programming units and software makes design development and functional testing of PAL devices quick and easy.

The PAL logic array has a total of 20 complementary inputs and 10 outputs generated by a single programmable AND-gate array with fixed OR-gate connections. Device outputs are either taken directly from the AND-OR functions (combinatorial) or passed through exclusive-OR gates and D-type flip-flops (registered). Registers allow the PAL device to implement sequential logic circuits. The exclusive-OR functions provide easy implementation of the "hold" operation used in counters and other state sequences. TRI-STATE® outputs facilitate busing and provide bidirectional I/O capability. The exclusive-OR PAL family offers a variety of combinatorial and registered output mixtures, as shown in the Device Types table below.

Series-A devices have power-up reset and register preload features available. On power-up, all registers are reset to simplify sequential circuit design and testing. Direct register preload is also provided to facilitate device testing. Security fuses can be programmed to prevent direct copying of proprietary logic patterns.

Features

- As fast as 30 ns maximum propagation delay (combinatorial)
- Exclusive-OR function facilitates design of counters and state sequences
- User-programmable replacement for TTL logic
- Large variety of JEDEC-compatible programming equipment and design development software available
- Fully supported by National PLAN™ development software
- Power-up reset for registered outputs (Series-A)
- Register preload facilitates device testing (Series-A)
- Security fuse prevents direct copying of logic patterns

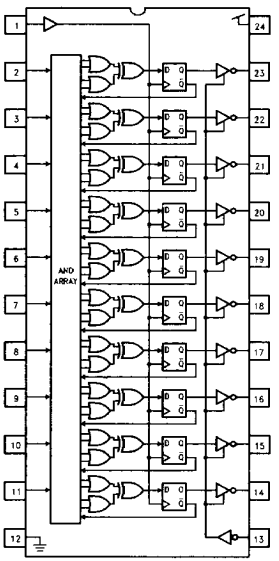
Device Types

Device Type	Dedicated Inputs	Registered Outputs (With Feedback)	Combinatorial	
			I/Os	Outputs
PAL20L10	14	—	6	2
PAL20X4	12	4	4	—
PAL20X8	12	6	2	—
PAL20X10	12	8	—	—

Speed/Power Versions

Series	Example	Commercial		Military	
		t_{PD}	I_{CC}	t_{PD}	I_{CC}
Standard	PAL20L10	50 ns	165 mA	60 ns	165 mA
A	PAL20L10A	30 ns	165 mA	35 ns	165 mA

Block Diagram—PAL20X10



TL/L/9998–1

Standard Series (PAL20L10, PAL20X4, PAL20X8, PAL20X10)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 2)	−0.5V to +7.0V
Input Voltage (Notes 2 and 3)	−1.5V to +5.5V
Off-State Output Voltage (Note 2)	−1.5V to +5.5V
Input Current (Note 2)	−30 mA to +5.0 mA
Output Current (I_{OL})	+100 mA
Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−65°C to +125°C
Junction Temperature	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter		Military			Commercial			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature		−55			0		75	°C
T_C	Operating Case Temperature				125				°C
t_W	Clock Pulse Width	Low	40	20		35	20		ns
		High	30	10		25	10		ns
t_{SU}	Setup Time from Input or Feedback to Clock		60	38		50	38		ns
t_H	Hold Time of Input after Clock		0	−15		0	−15		ns
f_{CLK}	Clock Frequency (Note 4)	With Feedback		17.2	10.0		17.2	12.5	MHz
		Without Feedback		33.3	14.3		33.3	16.7	MHz

Electrical Characteristics Over Recommended Operating Conditions (Note 5)

Symbol	Parameter	Test Conditions			Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage (Note 6)						0.8	V
V_{IH}	High Level Input Voltage (Note 6)				2			V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I = −18 mA				−0.8	−1.5	V
I_{IL}	Low Level Input Current (Note 7)	V_{CC} = Max, V_I = 0.4V				−0.02	−0.25	mA
I_{IH}	High Level Input Current (Note 7)	V_{CC} = Max, V_I = 2.4V					25	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V					1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 12 mA	MIL		0.3	0.5	V
			I_{OL} = 24 mA	COM				
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2 mA	MIL	2.4	2.9		V
			I_{OH} = −3.2 mA	COM				
I_{OZL}	Low Level Off-State Output Current (Note 7)	V_{CC} = Max	V_O = 0.4V				−100	μA
I_{OZH}	High Level Off-State Output Current (Note 7)	V_{CC} = Max	V_O = 2.4V				100	μA
I_{OS}	Output Short-Circuit Current (Note 8)	V_{CC} = 5V, V_O = 0V			−30	−70	−130	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open	20L10			90	165	mA
			20X4, 20X8, 20X10			120	180	

Standard Series (PAL20L10, PAL20X4, PAL20X8, PAL20X10) (Continued)

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 13 (DIP) are connected directly to the security fuses, and the security fuses may be damaged preventing subsequent programming and verification operations.

Note 4: f_{CLK} with feedback is derived as $(t_{CLK} + t_{SU})^{-1}$.
f_{CLK} without feedback is derived as $(t_{WLOW} + t_{WHIGH})^{-1}$.

Note 5: All typical values are for $V_{CC} = 5.0V$ and $T_A = 25°C$.

Note 6: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

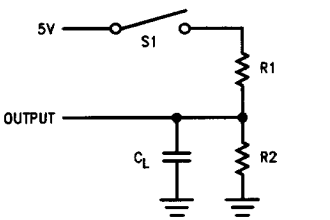
Note 7: Leakage current for bidirectional I/O pins is the worst case between I_{IL} and I_{OZL} or between I_{IH} and I_{OZH}.

Note 8: To avoid invalid readings in other parameter tests it is preferable to conduct the I_{OS} test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec. each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Military			Commerical			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or Feedback to Combinatorial Output	C_L = 50 pF, S1 Closed		35	60		35	50	ns
t_{CLK}	Clock to Registered Output or Feedback	C_L = 50 pF, S1 Closed		20	40		20	30	ns
t_{PZXG}	$\overline{G}$ Pin to Registered Output Enabled	C_L = 50 pF, Active High: S1 Open, Active Low: S1 Closed		20	45		20	35	ns
t_{PXZG}	$\overline{G}$ Pin to Registered Output Disabled	C_L = 5 pF, from V_{OH}: S1 Open, from V_{OL}: S1 Closed		20	45		20	35	ns
t_{PZXI}	Input to Combinatorial Output Enabled via Product Term	C_L = 50 pF, Active High: S1 Open, Active Low: S1 Closed		35	55		35	45	ns
t_{PXZI}	Input to Combinatorial Output Disabled via Product Term	C_L = 5 pF, from V_{OH}: S1 Open, from V_{OL}: S1 Closed		35	55		35	45	ns

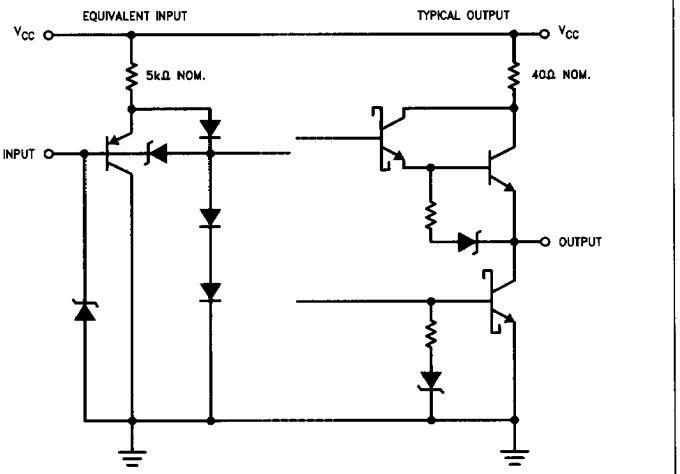
Test Load



TL/L/9998–2

MIL	COM'L
R1 = 390	R1 = 200
R2 = 750	R2 = 390

Schematic of Inputs and Outputs



TL/L/9998–3

Series—A (PAL20L10A, PAL20X4A, PAL20X8A, PAL20X10A)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.5V to +5.5V
Off-State Output Voltage (Note 2)	−1.5V to +5.5V
Input Current (Note 2)	−30 mA to +5.0 mA
Output Current (I_{OL})	+100 mA
Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−65°C to +125°C
Junction Temperature	−65°C to +150°C
ESD Tolerance (Note 3)	2000V

C_{ZAP} = 100 pF
R_{ZAP} = 1500Ω
Test Method: Human Body Model
Test Specification: NSC SOP-5-028

Recommended Operating Conditions

Symbol	Parameter		Military			Commercial			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature		−55			0		75	°C
T_C	Operating Case Temperature				125				°C
t_W	Clock Pulse Width	Low	35	15		25	15		ns
		High	20	7		15	7		ns
t_{SU}	Setup Time from Input or Feedback to Clock		40	20		30	20		ns
t_H	Hold Time of Input after Clock		0	−15		0	−15		ns
f_{CLK}	Clock Frequency (Note 4)	With Feedback			15.4			22.2	MHz
		Without Feedback			18.2			25.0	MHz

Electrical Characteristics Over Recommended Operating Conditions (Note 5)

Symbol	Parameter	Test Conditions			Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage (Note 6)						0.8	V
V_{IH}	High Level Input Voltage (Note 6)				2			V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I = −18 mA				−0.8	−1.5	V
I_{IL}	Low Level Input Current (Note 7)	V_{CC} = Max, V_I = 0.4V				−0.04	−0.25	mA
I_{IH}	High Level Input Current (Note 7)	V_{CC} = Max, V_I = 2.4V					25	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V					100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 12 mA	MIL		0.3	0.5	V
			I_{OL} = 24 mA	COM				
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2 mA	MIL	2.4	2.9		V
			I_{OH} = −3.2 mA	COM				
I_{OZL}	Low Level Off-State Output Current (Note 7)	V_{CC} = Max	V_O = 0.4V				−100	μA
I_{OZH}	High Level Off-State Output Current (Note 7)	V_{CC} = Max	V_O = 2.4V				100	μA
I_{OS}	Output Short-Circuit Current (Note 8)	V_{CC} = 5V, V_O = 0V			−30	−70	−130	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open	20L10A			115	165	mA
			20X4A, 20X8A, 20X10A			135	180	

Series—A (PAL20L10A, PAL20X4A, PAL20X8A, PAL20X10A) (Continued)

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 13 (DIP) are connected directly to the security fuses, and although the input circuitry can withstand the specified ESD conditions, the security fuses may be damaged preventing subsequent programming and verification operations.

Note 4: f_{CLK} with feedback is derived as $(t_{CLK} + t_{SU})^{-1}$.
f_{CLK} without feedback is derived as $(t_{WLOW} + t_{WHIGH})^{-1}$.

Note 5: All typical values are for $V_{CC} = 5.0V$ and $T_A = 25°C$.

Note 6: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

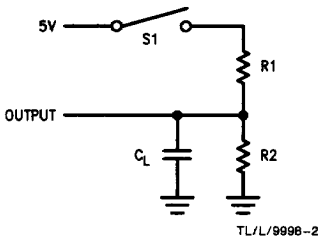
Note 7: Leakage current for bidirectional I/O pins is the worst case between I_{IL} and I_{OZL} or between I_{IH} and I_{OZH}.

Note 8: To avoid invalid readings in other parameter tests it is preferable to conduct the t_{OS} test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec. each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Military			Commerical			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or Feedback to Combinatorial Output	C_L = 50 pF, S1 Closed		23	35		23	30	ns
t_{CLK}	Clock to Registered Output or Feedback	C_L = 50 pF, S1 Closed		10	25		10	15	ns
t_{PZXG}	$\overline{G}$ Pin to Registered Output Enabled	C_L = 50 pF, Active High: S1 Open, Active Low: S1 Closed		11	25		11	20	ns
t_{PXZG}	$\overline{G}$ Pin to Registered Output Disabled	C_L = 5 pF, from V_{OH}: S1 Open, from V_{OL}: S1 Closed		10	25		10	20	ns
t_{PZXI}	Input to Combinatorial Output Enabled via Product Term	C_L = 50 pF, Active High: S1 Open, Active Low: S1 Closed		19	35		19	30	ns
t_{PXZI}	Input to Combinatorial Output Disabled via Product Term	C_L = 5 pF, from V_{OH}: S1 Open, from V_{OL}: S1 Closed		15	35		15	30	ns
t_{RESET}	Power-Up to Registered Output High			600	1000		600	1000	ns

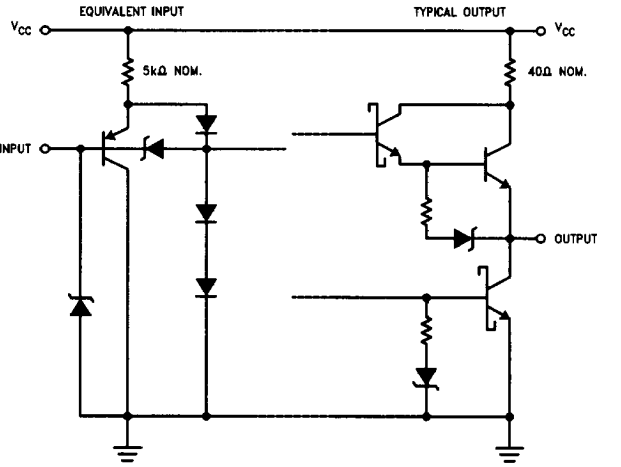
Test Load



TL/L/9998–2

MIL	COM'L
R1 = 390	R1 = 200
R2 = 750	R2 = 390

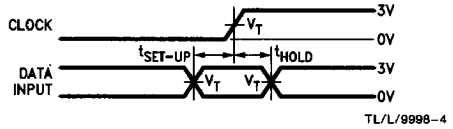
Schematic of Inputs and Outputs



TL/L/9998–3

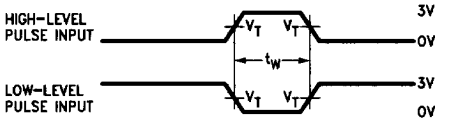
Test Waveforms

Set-Up and Hold



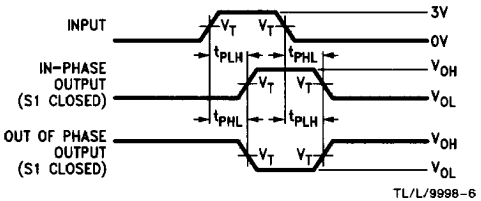
TL/L/9998–4

Pulse Width



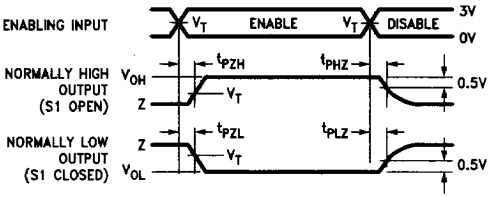
TL/L/9998–5

Propagation Delay



TL/L/9998–6

Enable and Disable



TL/L/9998–7

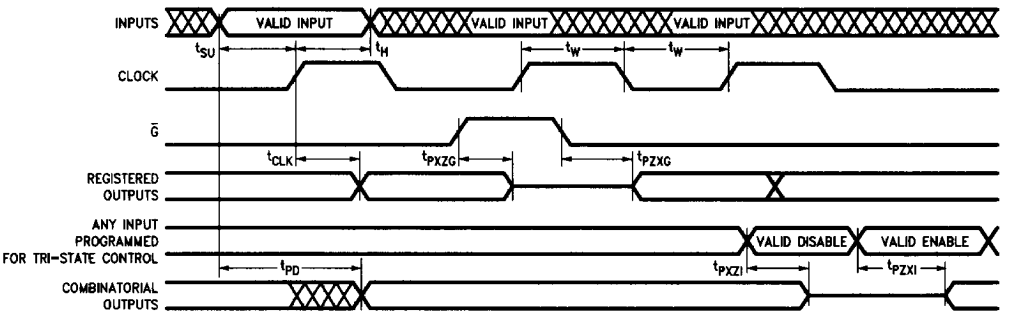
Notes:

V_T = 1.5V

C_L includes probe and jig capacitance.

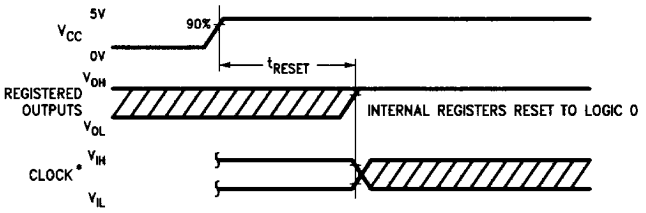
In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Switching Waveforms



TL/L/9998–8

Power-Up Reset Waveform (Series-A only)



TL/L/9998–9

*The clock input should not be switched from low to high until after time t_{RESET}.

Functional Description

All of the 24-pin Exclusive-OR PAL logic arrays consist of 20 complementary input lines and 40 product-term lines with a programmable fuse link at each intersection (1600 fuses). The product terms are organized into ten groups of four each. Three or four of the product terms in each group connect into OR-gates to produce the output logic function, depending on whether the output is combinatorial or registered.

An unprogrammed (intact) fuse establishes a connection between an input line (true or complement phase of an array input signal) and a product term; programming the fuse removes the connection. A product term is satisfied (logically true) while all of the input lines connected to it (via unprogrammed fuses) are in the high logic state. Therefore, if both the true and complement of at least one array input is left connected to a product line, that product term is always held in the low logic state (which is the state of all product terms in an unprogrammed device). Conversely, if all fuses on a product term were programmed, the product term would be held in the high state.

The exclusive-OR PAL family consists of four device types with differing mixtures of combinatorial and registered outputs. The 20L10, 20X4, 20X8 and 20X10 architectures have 0, 4, 8 and 10 registered outputs, respectively, with the balance of the 10 outputs combinatorial. All outputs are active-low and have TRI-STATE capability.

Each combinatorial output has a three product-term logic function, with the fourth product term being used for TRI-STATE control. A combinatorial output is enabled while the TRI-STATE product term is satisfied (true). Combinatorial outputs also have feedback paths from the device pins into the logic array (except for two outputs on the 20L10). This allows a pin to perform bidirectional I/O or, if the associated logic function were left unprogrammed, the output driver would remain disabled and the pin could be used as an additional dedicated input.

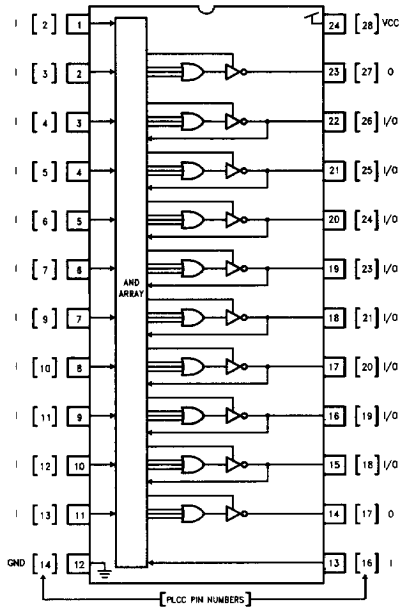
For the registered outputs, the groups of the four product terms are segmented into two OR-sums of two product terms each; which are then combined by an exclusive-OR gate at the input of the D-type flip-flop. All registers are triggered by the high-going edge of the clock input pin. All registered outputs are controlled by a common output enable ($\overline{G}$) pin (enabled while low). The output of each register is also fed back into the logic array via an internal path. This provides for sequential logic circuits (state machines, counters, etc.) which can be sequenced even while the outputs are disabled.

The 24-pin Exclusive-OR PAL Series-A devices reset all registers to a low state upon power-up (active-low outputs assume high logic levels if enabled). This may simplify sequential circuit design and test. To ensure successful power-up reset, V_{CC} must rise monotonically until the specified operating voltage is attained. During power-up, the clock input should assume a valid, stable logic state as early as possible to avoid interfering with the reset operation. The clock input should also remain stable until after the power-up reset operation is completed to allow the registers to capture the proper next state on the first high-going clock transition.

As with any TTL logic circuits, unused inputs to a PAL device should be connected to ground, V_{OL}, V_{OH}, or resistively to V_{CC}. However, switching any input not connected to a product term or logic function has no effect on its output logic state.

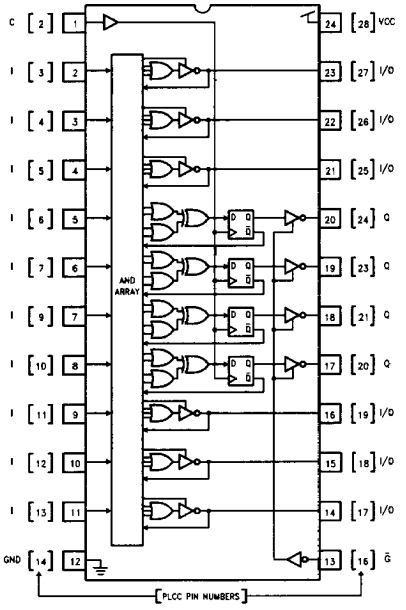
24-Pin Exclusive-OR PAL Family Block Diagrams—DIP Connections

PAL20L10



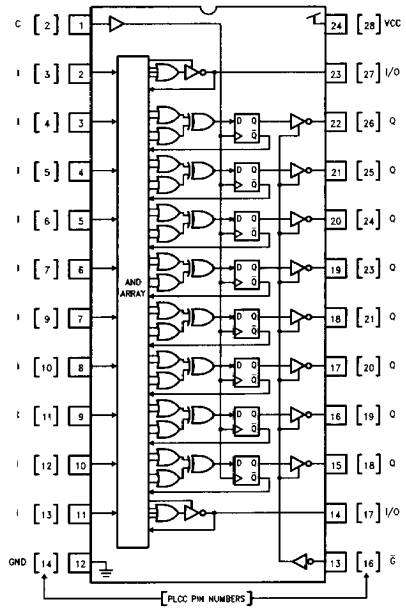
TL/L/9998–10

PAL20X4



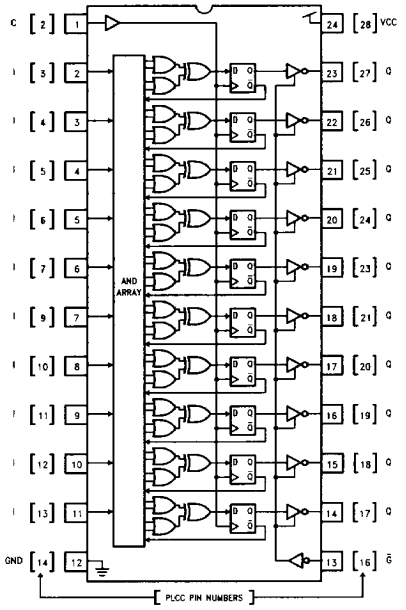
TL/L/9998–11

PAL20X8



TL/L/9998–12

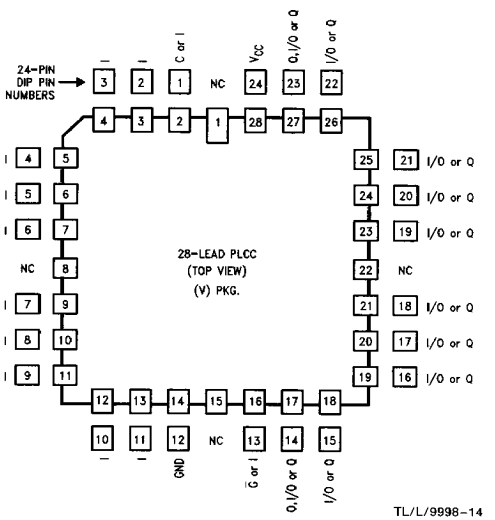
PAL20X10



TL/L/9998–13

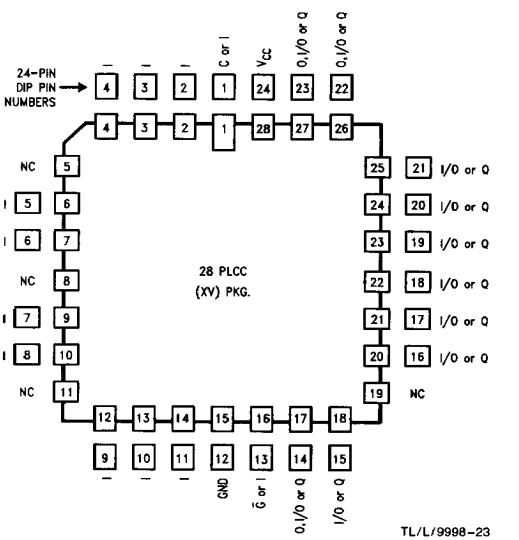
28-Lead PLCC Connection Conversion Diagram*

JEDEC PLCC Diagram



TL/L/9998-14

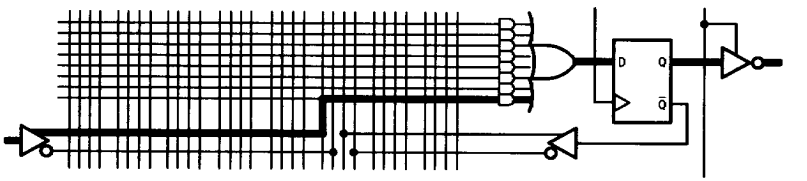
Non-JEDEC PLCC Diagram



TL/L/9998-23

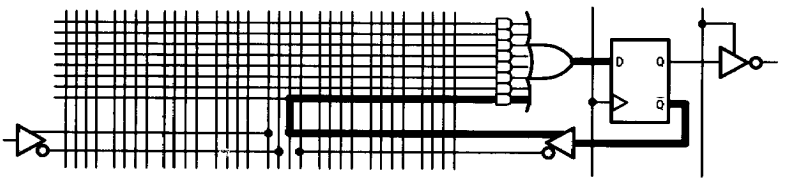
*For availability of old (Non-JEDEC) pinout, please contact your local National Semiconductor sales representative or distributor. PAL20L10 (Standard Series) is not available in the JEDEC pinout shown above.

Typical Registered Logic Function Without Feedback



TL/L/9998-15

Typical Registered Logic Function With Feedback



TL/L/9998-16

Functional Description (Continued)

CLOCK FREQUENCY SPECIFICATION

The clock frequency (f_{CLK}) parameter specifies the maximum speed at which a registered PAL device is guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, where the logic functions fed into the registers are not dependent on register feedback from the previous cycle (i.e., based only on external inputs), the minimum required cycle period (f_{CLK}^{-1} without feedback) is defined as the greater of the minimum clock period (t_W high + t_W low) and the minimum "data window" period (t_{SU} + t_H). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period (f_{CLK}^{-1} with feedback) is defined as t_{CLK} + t_{SU}. This provides sufficient time for outputs from the registers to feed back through the logic array and set-up on the inputs to the registers before the end of each cycle.

Output Register Preload (Series-A)

The preload function allows the registers to be loaded asynchronously from data placed on the output pins. This feature simplifies device testing since any state may be loaded into the registers at any time during the functional test sequence. This allows complete verification of sequential logic circuits, including states that are normally impossible or difficult to reach. Register preload is not an operational mode and is not intended for board level testing because elevated voltage levels are required. The programming system normally provides the preload capability as part of its functional test facility.

The register preload procedure is as follows:

1. V_{CC} is raised to 4.5V.
2. Registered outputs are disabled by raising output enable ($\overline{G}$) to V_{IH}.
3. The desired data values are applied to all registered output pins (V_{IL} = set, V_{IH} = reset).
4. DIP pin 10 (PCC pin 12) is pulsed to V_P, then back to V_{IL}. (V_P = 18.0V ±0.5V).
5. Data inputs are removed from registered output pins.
6. $\overline{G}$ is lowered to V_{IL} to enable registered outputs.
7. The desired data values are verified at all registered outputs (V_{OL} = Set, V_{OH} = Reset).

Note: The minimum recommended time delay (t_D) between successive input transitions (including the V_P pulse width on DIP pin 8) is 100 ns.

Security Fuse

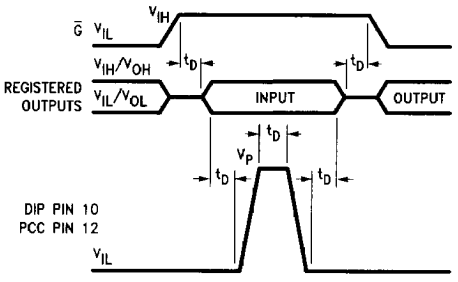
Security fuses are provided on all 24-pin Exclusive-OR PAL devices which, when programmed, inhibit any further programming or verifying operations. This feature prevents direct copying of proprietary logic patterns. The security fuses should be programmed only after programming and verifying all other device fuses. Register preload is not affected by the security fuses.

Design Development Support

A variety of software tools and programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible "fuse maps". The industry-standard JEDEC format ensures that the resulting fuse-map files can be down-loaded into a large variety of programming equipment. Many software packages and programming units support a large variety of programmable logic products as well. The PLAN™ software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer's Boolean logic equations.

Detailed logic diagrams showing all JEDEC fuse-map addresses for the 24-pin Exclusive-OR PAL family are provided for direct map editing and diagnostic purposes. For a list of current software and programming support tools available for these devices, please contact your local National Semiconductor sales representative or distributor. If detailed specifications of the PAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support Department.

Register Preload Waveform

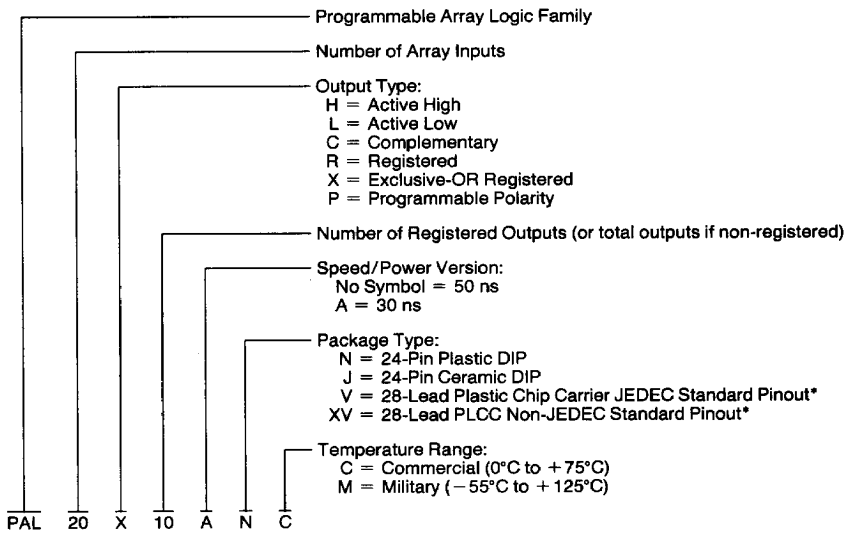


TL/L/9998-17

Note: V_P = 18.0V ±0.5V, t_D min. = 100 ns

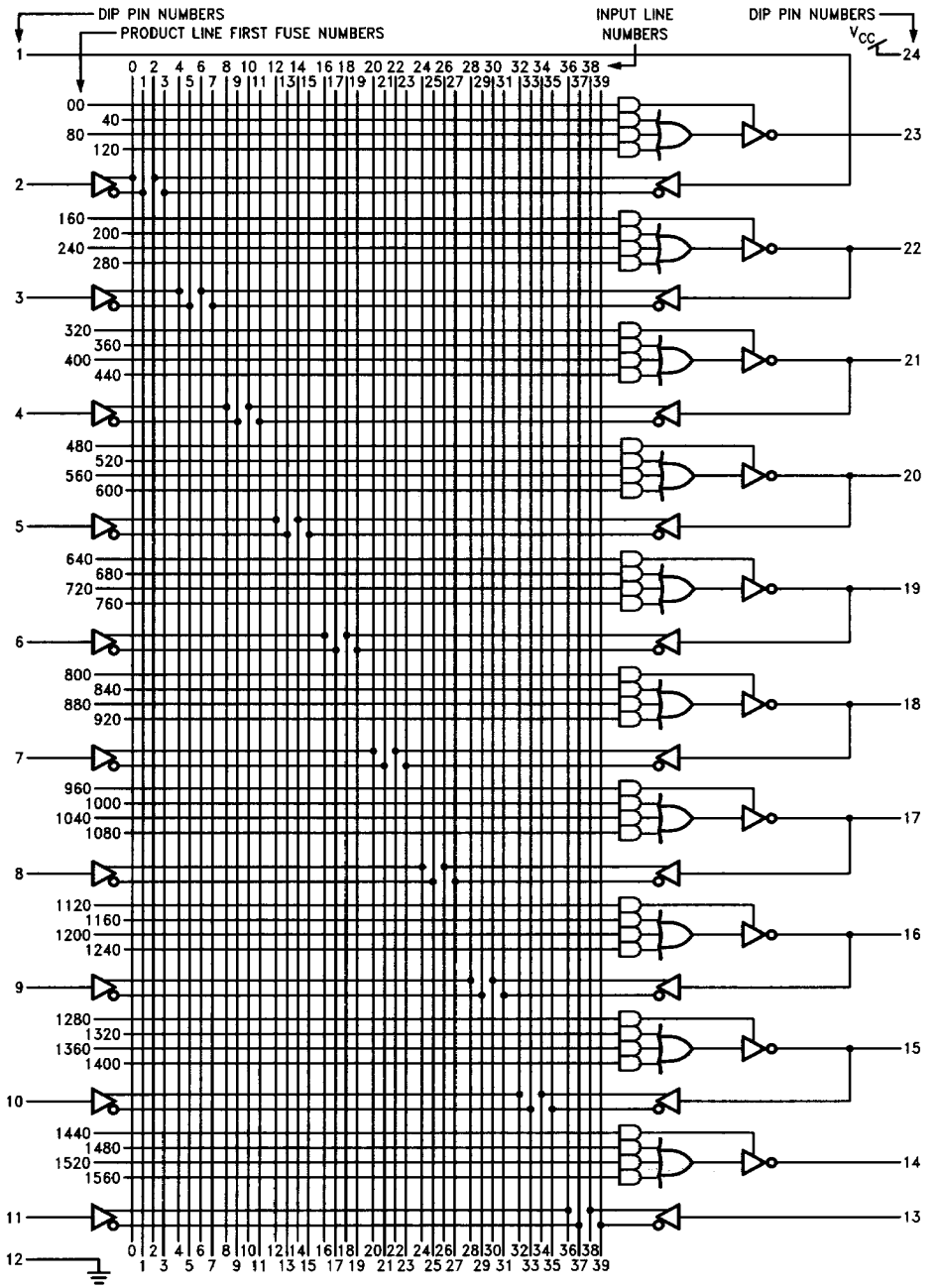
Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



*For availability of PAL20L10 in PLCC package, please contact your sales office.

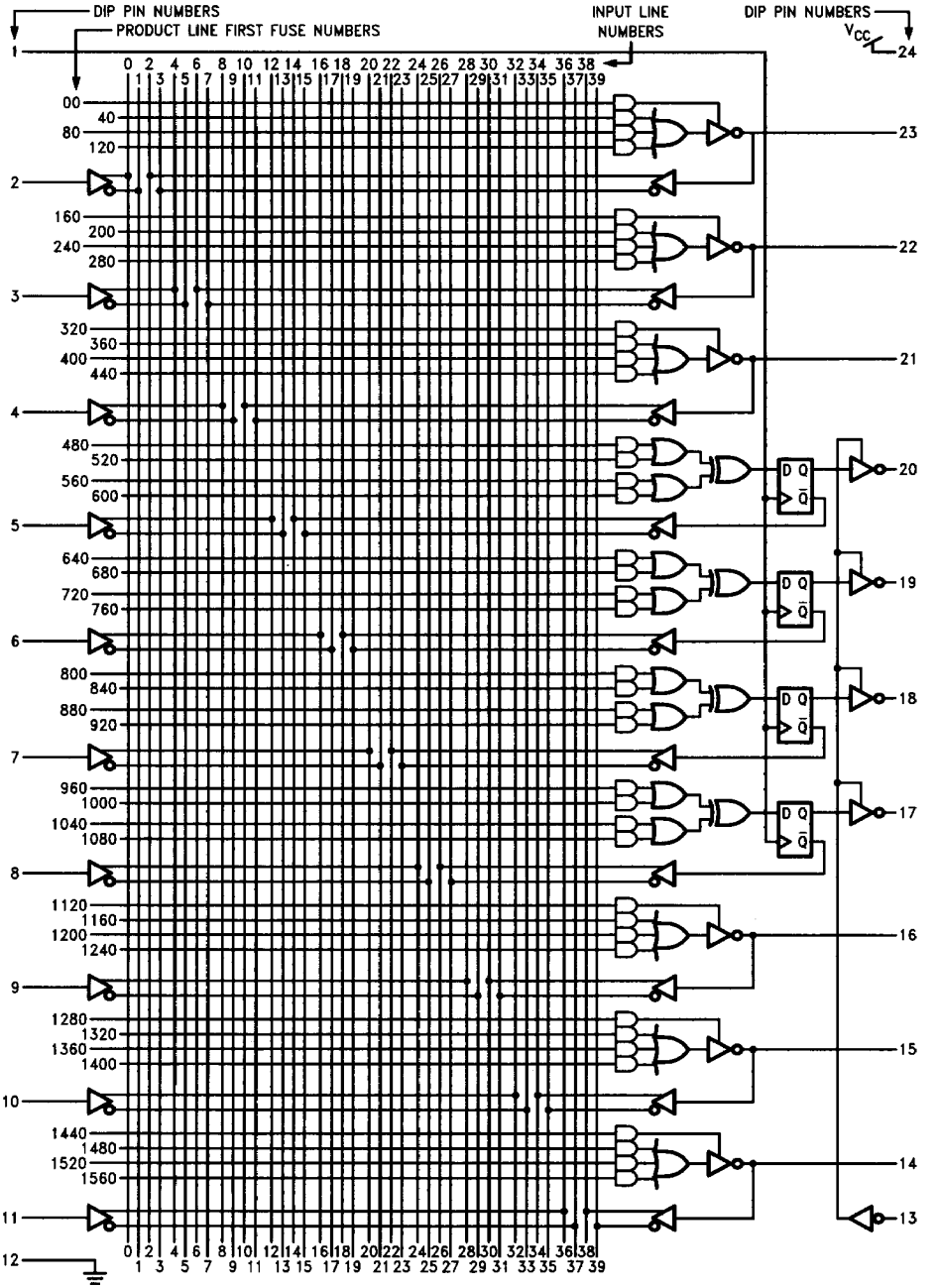
Logic Diagram PAL20L10



TL/L/9998–19

JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.

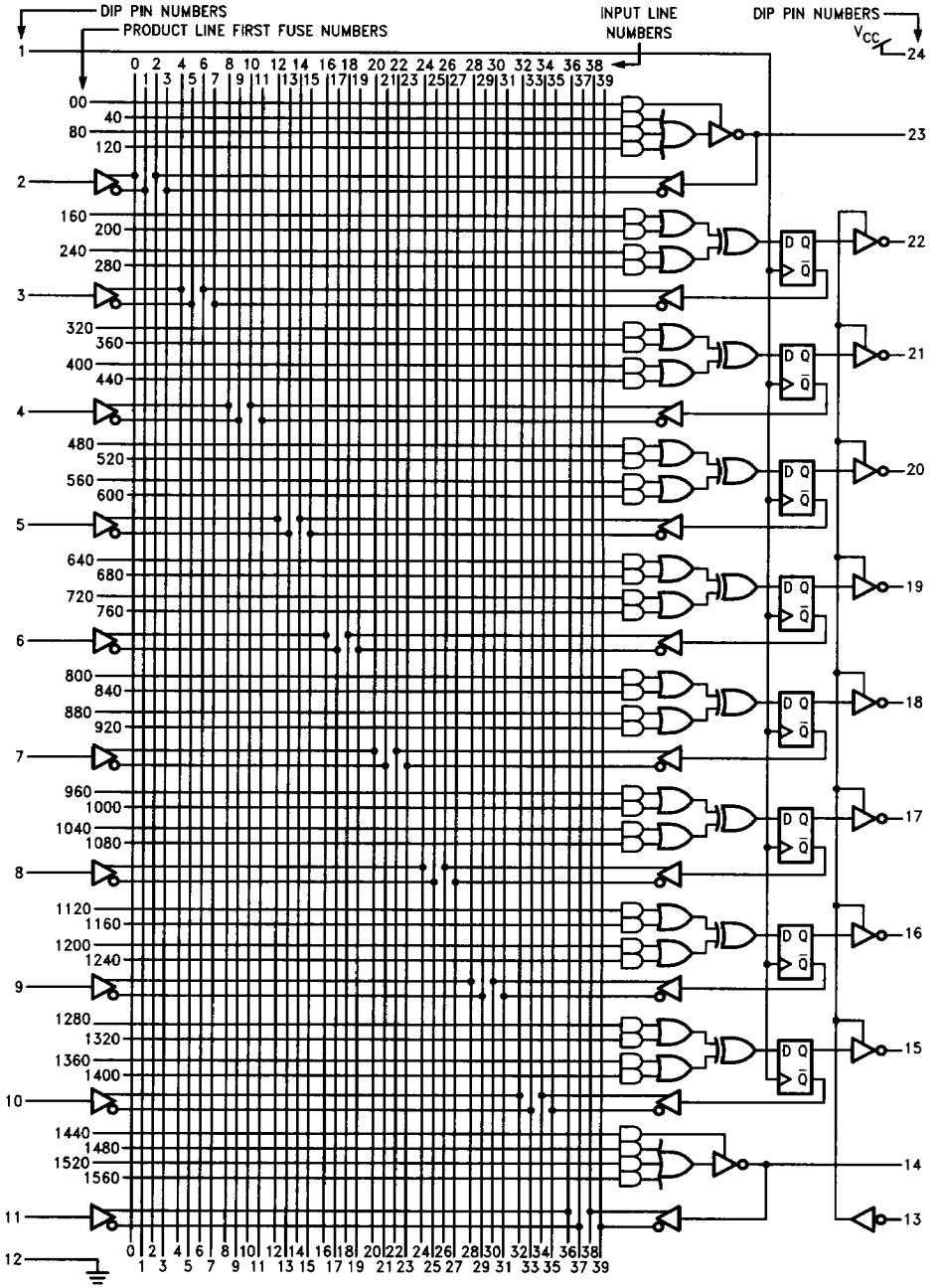
Logic Diagram PAL20X4



TL/L/9998–20

JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.

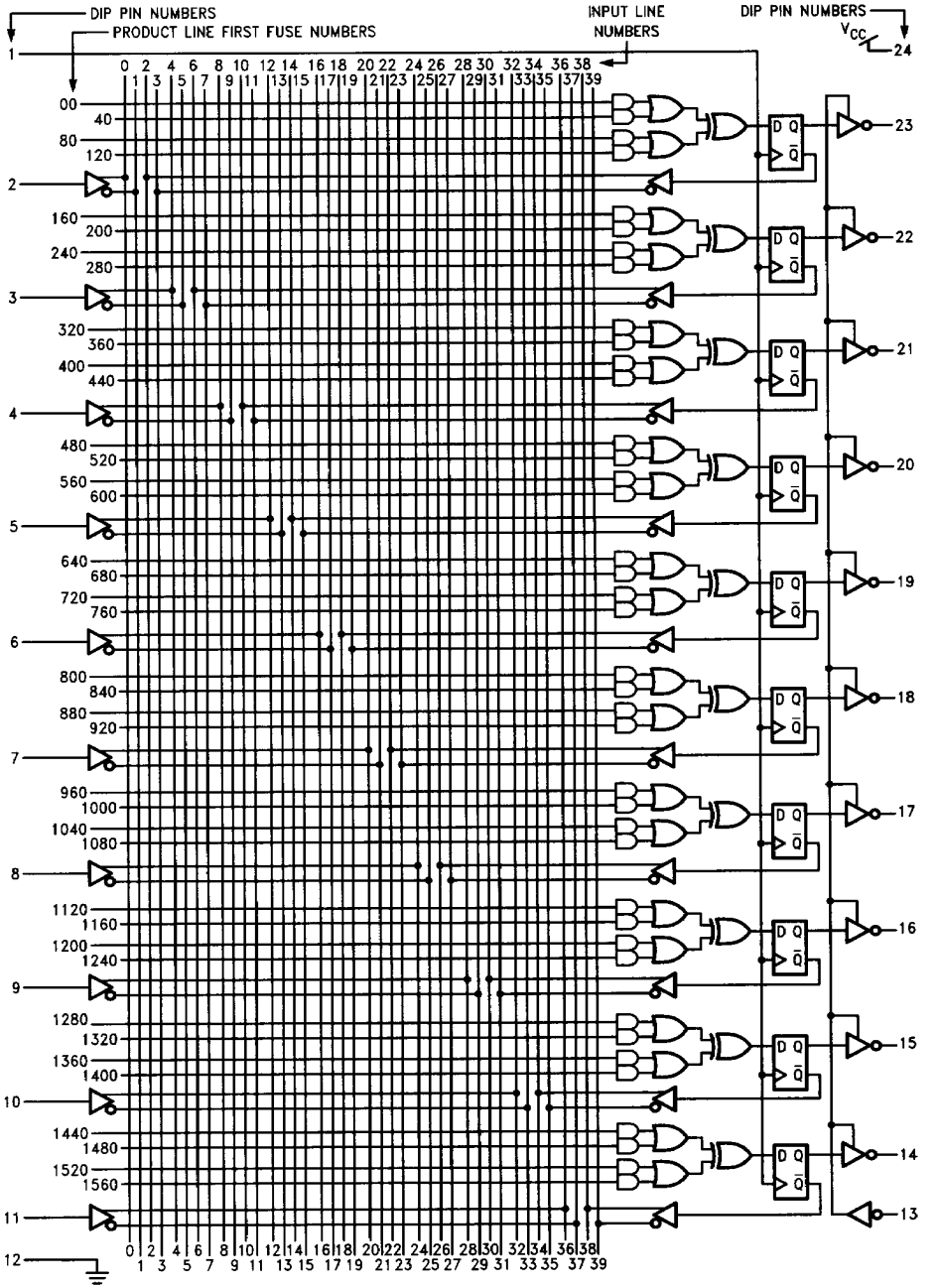
Logic Diagram PAL20X8



TL/L/9998–21

JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.

Logic Diagram PAL20X10



TL/L/9998–22

JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.