PDSP1640
20MHz ADDRESS GENERATOR

The PDSP1640 is an 8-bit address generator which will cascade efficiently to wider address fields at very high speed, without the need for external carry logic.

Three PDSP1640s allow 24-bit addresses to be generated at up to 10MHz; four allow 32-bit addressing at up to 7MHz. A single PDSP1640 will address an 8-bit field at 20MHz.

FEATURES
- 20MHz 8-Bit Address Generator
- Fast Cascade Logic gives 10MHz Operation at 24Bits
- Five On-chip User-Programmable Registers
- Output Mask Logic
- 300mW Maximum Power Dissipation
- 28-Pin DIL or LCC Package

APPLICATIONS
- DSP Address Generation
- Database Addressing
- DMA Controllers
- Modulo Counting

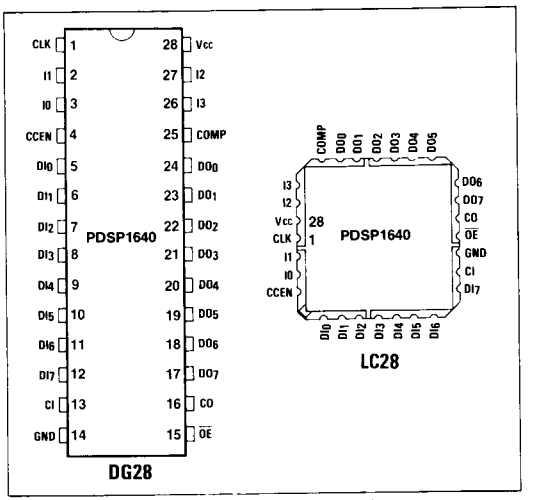


Fig.1 Pin connections - top view

ASSOCIATED PRODUCTS
PDSP16318 Complex Accumulator
PDSP16112 Complex Number Multiplier
PDSP1601 ALU and Barrel Shifter

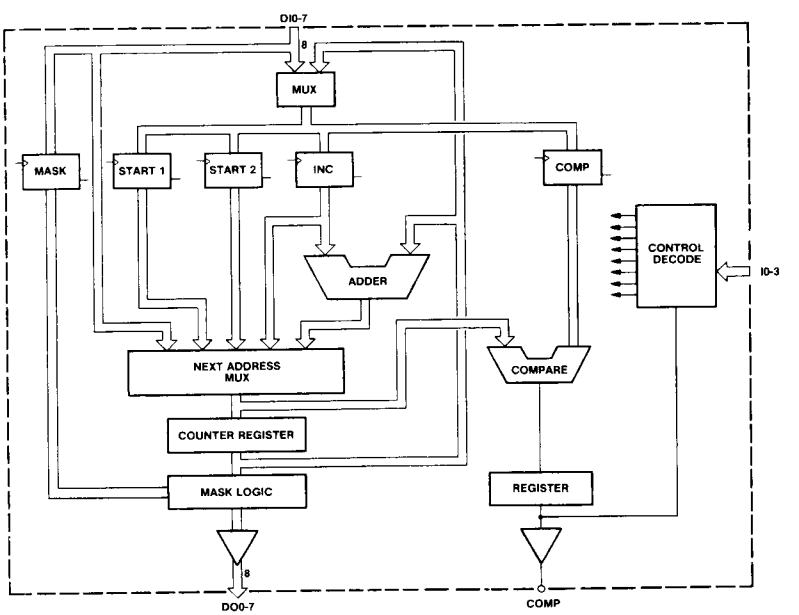


Fig.2 PDSP1640 simplified block diagram

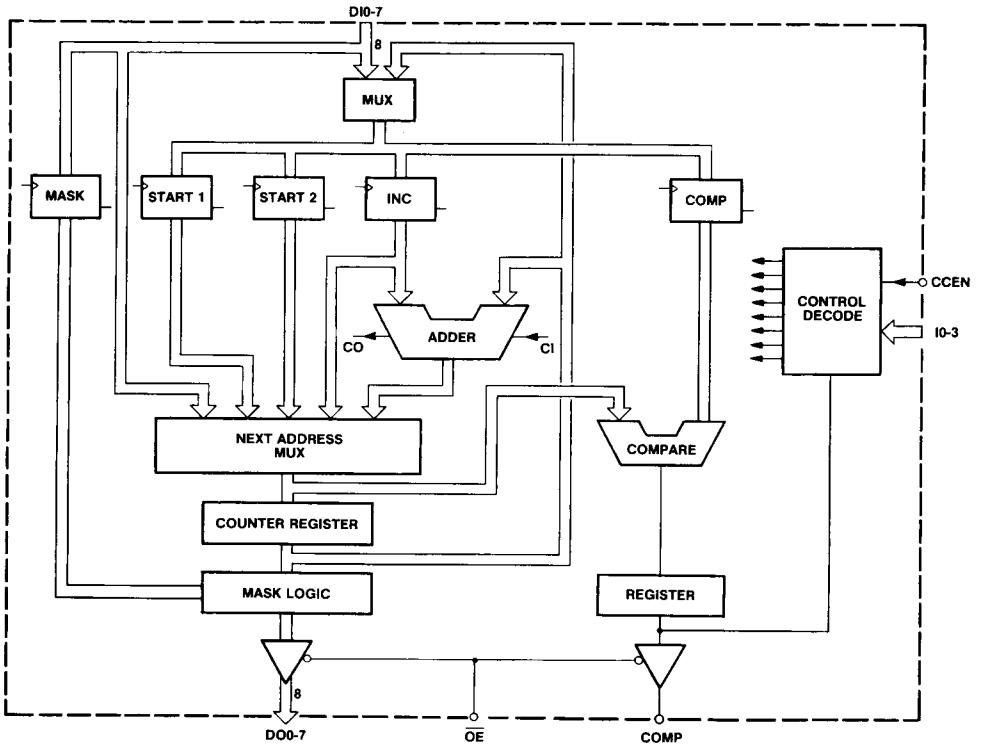


Fig.3 PDSP1640 block diagram

PIN DESCRIPTIONS

Symbol	Pin No.	Pin name and description
CLK	1	**Common clock** to all registered internal elements. All registers are loaded, and outputs change on the rising edge of CLK.
I0-3	3,2, 27,26	**Instruction inputs.** The 16 instructions executable by the PDSP1640 are encoded onto these four lines. The instruction for any cycle must be valid at the inputs prior to the rising edge of CLK defining the start of the cycle in which the instruction is to be executed. The I0-3 inputs are internally latched by the rising edge of CLK.
CCEN	4	**Conditional Instruction Enable.** The Conditional Instructions during the current cycle are enabled if CCEN goes high before the end of the cycle. CCEN may be controlled directly by microcode or, where multiple 1640's are used, this input is used for expansion. See Figs.6 and 7.
COMP	25	**Comparator Flag Output.** This indicates that the comparator has detected an 'equal to' condition, COMP changes when CLK goes HIGH.
CI	13	**Carry In.** Carry in to least significant bit of the 8-bit adder.
CO	16	**Carry Out.** Carry out from the MSB of the adder.
DI0-7	5-12	**Data Inputs.** 8-bit data input to PDSP1640. The data on this port is loaded into the on-board registers on the rising edge of CLK.
DO0-7	24-17	**Data Outputs.** The 8-bit output from the counter. The output changes on the rising edge of CLK.
$\overline{OE}$	15	**3-State Output Control.** When high, this signal forces the DO0-7 and COMP outputs into a high-impedance state.
GND	14	0V supply.
Vcc	28	+5V supply.

FUNCTIONAL DESCRIPTION

The PDSP1640 contains six main blocks; the five user programmable registers, an 8-bit Adder, the Mask Logic, a Comparator, the Control Decoder and the Next Address MUX and Counter Register.

The Registers

There are five user programmable registers; MASK, START1, START2, INC and COMP.

MASK Data loaded into the MASK register operates on the data fed to the Mask Logic from the Counter Register. Loading new data into the MASK register automatically enables the Mask Logic. The Mask Logic is disabled either by loading zeros into the MASK register or by executing OP CODE <7> (Clear Counter Register/Mask disable). The Mask Logic will remain disabled until new data is loaded into the MASK register.
N.B. The MASK register can only be loaded from DI0-7.

START1 The START1 register can be loaded from either the DI0-7 inputs, or from the Counter Register. The contents of the START1 register may be forced into the Counter Register (OP CODE <6>), or may be used as a jump address in a conditional instruction.

START2 The START2 register can be loaded from either the DI0-7 inputs, or from the Counter Register. The contents of the START2 Register may be used as the jump address in a conditional instruction.

INC The INC register contains the value by which the counter will increment. This may be a positive or negative number, represented in 2's complement.
The INC register may be loaded either from the DI0-7 inputs, or from the Counter Register.

COMP The COMP register contains the value used by the comparator. It may be programmed from either the DI0-7 inputs or from the Counter Register.

8-Bit Adder

The 8-BIT ADDER adds the contents of the Inc and Counter Registers and loads the result into the Counter Register conditional on the current instruction.
The ADDER has a fast carry system which eliminates the need for external carry look-ahead circuitry when cascaded. Cascading is achieved by chaining CO to CI of the next most significant stage (see Fig.6).

Mask Logic

The MASK LOGIC is controlled by the contents of the Mask Register. 1's in the Mask Register will cause the corresponding outputs from the PDSP1640 to be frozen, even if the data in the Counter Register changes. In this manner 'windows' can be created within the counter's address field.
The MASK LOGIC is enabled whenever new data is loaded into the Mask Register. A zero word in the Mask Register will disable the MASK LOGIC as will executing OP CODE <7>.

Comparator

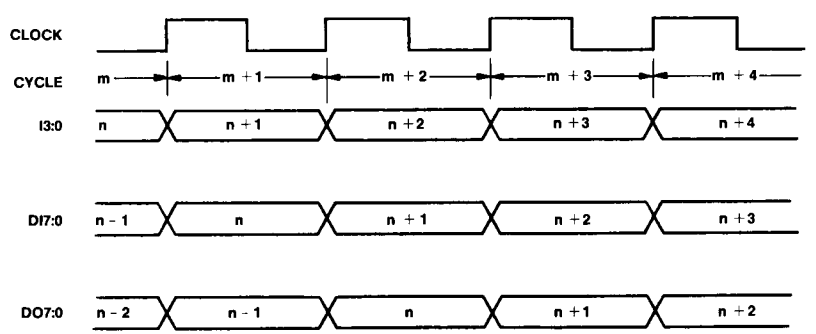
The COMPARATOR compares the value in the Comp Register with the output from the NEXT ADDRESS MUX. If the values are the same, then a signal is sent to the Control Decoder and onto the COMP output via the output register.

Control Decoder

The CONTROL DECODER has six inputs; the four instruction lines I0-3, CCEN, and an internal Comp Flag.
The CONTROL DECODER latches all except the CCEN input and the internal Comp Flag, on the rising edge of CLK. The I0-3 inputs are decoded to implement the operations shown in Table 2. CCEN and the Comp Flag change the instruction executed in the current cycle, where appropriate.

Next Address Mux and Counter Register

The contents of the COUNTER REGISTER at the start of a new cycle are determined by the NEXT ADDRESS MUX under the control of the Control Decoder.
The NEXT ADDRESS MUX selects between the DI0-7 inputs, the contents of START1 and 2, the contents of the Inc Register, and the output of the 8-bit Adder. The COUNTER REGISTER may be cleared by OP CODE <7>. The COUNTER REGISTER clock is inhibited for all instructions except those marked * in Table 2, this is to prevent the counter incrementing during register loads.



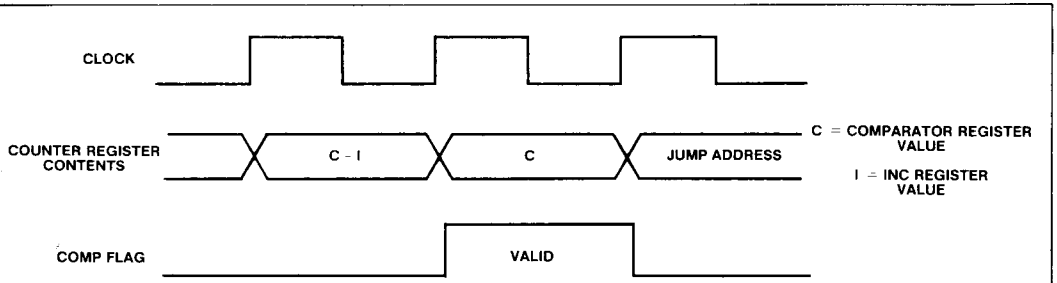
EXAMPLE
The result on DO7:0 on cycle m +3 is generated from data (DI7:0) applied on cycle m + 2 and the instruction (I3:0) applied on cycle m + 1.

Fig.4 Register delays

INSTRUCTION SET

Mnemonic	Op Code	Function
CCJDI	<0>	On the next cycle the contents of the Counter Register will be added to the contents of the Increment Register and the result loaded into the Counter Register. If the COMP flag and CCEN become active, then on the following cycle, the Counter Register will be loaded with the data on DI0-7.
CCJS1	<1>	On the next cycle the contents of the Counter Register will be added to the contents of the Increment Register and the result loaded into the Counter Register. If the COMP flag and CCEN become active, then on the following cycle, the Counter Register will be loaded with the contents of the Start1 Register.
CCJS2	<2>	On the next cycle the contents of the Counter Register will be added to the contents of the Increment Register and the result loaded into the Counter Register. If the COMP flag and CCEN become active, then on the following cycle, the Counter Register will be loaded with the contents of the Start2 Register.
LMRDI	<3>	Data present on DI0-7 will be loaded into the Mask Register by the rising edge of CLK at the end of the cycle in which this instruction is executed.
LCRDI	<4>	The data present on DI0-7 will be loaded into the Counter Register by the rising edge of CLK at the end of the cycle in which this instruction is executed.
LCRIR	<5>	The Counter Register will be loaded with the contents of the Inc Register by the rising edge of CLK at the end of the cycle in which this instruction is executed.
LCRS1	<6>	The Counter Register will be loaded with the contents of the Start1 Register by the rising edge of CLK at the end of the cycle in which this instruction is executed.
CLRCR	<7>	The Counter Register will be cleared and the Mask Logic disabled by the rising edge of CLK at the end of this instruction cycle.
LS1DI	<8>	The data present on DI0-7 will be loaded into the Start1 Register by the rising edge of CLK at the end of this instruction cycle.
LS1CR	<9>	The Start1 Register will be loaded with the contents of the Counter Register by the rising edge of CLK at the end of this instruction cycle.
LS2DI	<A>	The data present on DI0-7 will be loaded into the Start2 Register by the rising edge of CLK at the end of this instruction cycle.
LS2CR	<B>	The Start2 Register will be loaded with the contents of the Counter Register by the rising edge of CLK at the end of this instruction cycle.
LIRDI	<C>	The data present on the DI0-7 input will be loaded into the Inc Register by the rising edge of CLK at the end of this instruction cycle.
LIRCR	<D>	The Inc Register will be loaded with the contents of the Counter Register by the rising edge of CLK at the end of this instruction cycle.
LCPDI	<E>	The data present on the DI0-7 inputs will be loaded into the Comp Register by the rising edge of CLK at the end of this instruction cycle.
LCPCR	<F>	The Comp Register will be loaded with the contents of the Counter Register by the rising edge of CLK at the end of this instruction cycle.

Table 1 Instruction descriptions



NOTE
A jump can also be forced by following LCPCR with CCJXX, provided the LCPCR instruction is held for two cycles prior to CCJXX.

Fig.5 Comparison flag timing

INSTRUCTION SET

Mnemonic	Code	I_3	I_2	I_1	I_0	Operation	Jump To
*CCJDI	0	0	0	0	0	Count by IR	DI0-7
*CCJS1	1	0	0	0	1	Count by IR	START1
*CCJS2	2	0	0	1	0	Count by IR	START2
LMRDI	3	0	0	1	1	Ld MR from DI0-7	
*LCRDI	4	0	1	0	0	Ld CR from DI0-7	
*LCRIR	5	0	1	0	1	Ld CR from IR	
*LCRS1	6	0	1	1	0	Ld CR from S1	
CLRCR	7	0	1	1	1	Clear CR/MR	
LS1DI	8	1	0	0	0	Ld S1 from DI0-7	
LS1CR	9	1	0	0	1	Ld S1 from CR	
LS2DI	A	1	0	1	0	Ld S2 from DI0-7	
LS2CR	B	1	0	1	1	Ld S2 from CR	
LIRDI	C	1	1	0	0	Ld IR from DI0-7	
LIRCR	D	1	1	0	1	Ld IR from CR	
LCPDI	E	1	1	1	0	Ld CP from DI0-7	
LCPCR	F	1	1	1	1	Ld CP from CR	

All instructions executed on the next rising edge of CLK. * indicates instructions which do not inhibit the counter register clock.

Table 2 Instruction set codes

Key

IR = Increment Register
MR = Mask Register
CR = Counter Register
S1 = Start1 Register
S2 = Start2 Register
CP = Comparator Register

Mnemonics

CCJXX = Conditional Count, Jump to XX
LXXYY = Load Destination XX from Source YY
CLRCR = Clear Counter Register/Reset Mask Logic

COUNTER CONFIGURATIONS

Fig.6 illustrates chaining of PDSP1640s to 16 bits and Fig.7 the configuration for a 24-bit address generator. The cascaded devices have exactly the same functions as a single device.

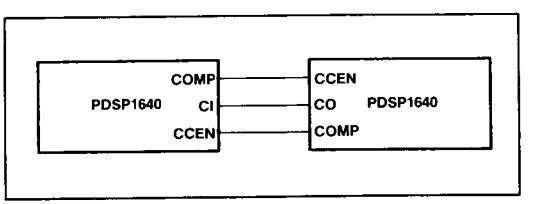


Fig.6 Chaining to 16 bits

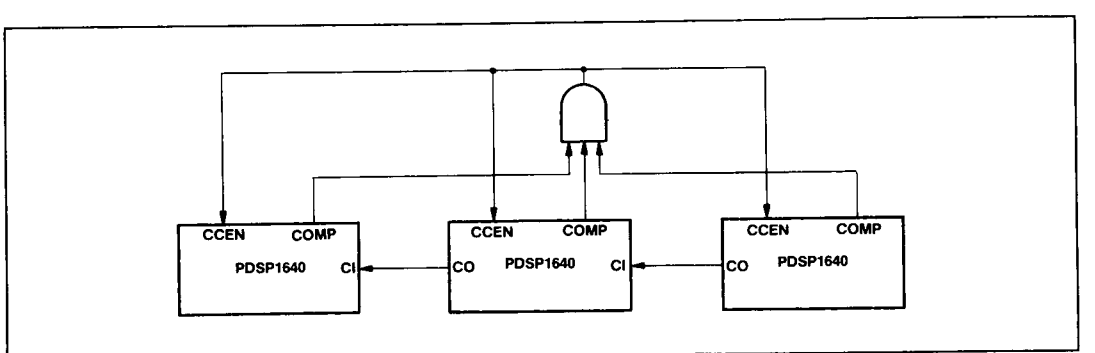


Fig.7 Chaining to 24 bits

TYPICAL APPLICATION

In the application shown in Fig.8 two PDSP1640s are used as an address generator in a digital waveform generator capable of producing complex waveforms at very high speeds. The programmable registers in the PDSP1640 allow the host microprocessor to control both frequency (by altering Step Size) and waveshape (by selecting different wavetables by Start Address).

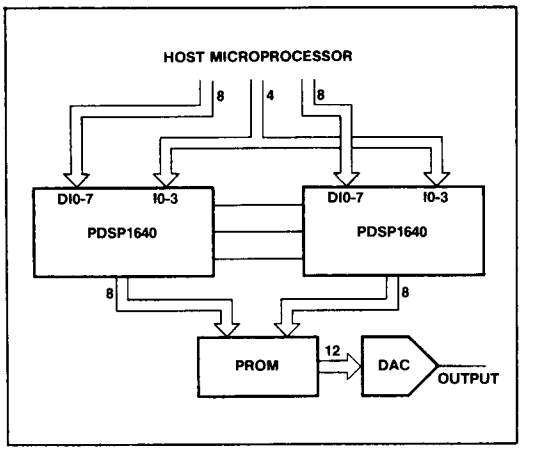


Fig.8 Arbitrary waveform generation

TYPICAL APPLICATION

Mnemonic	Op Code	Operation	Data
CLRCR	<7>	Clear CR/MR	X
LCRDI	<4>	Load CR	X
LIRDI	<C>	Load Inc Register	Start addr
LS1DI	<8>	Ld SR1 with branch addr	Step size
LCPDI	<E>	Ld COMPR with stop addr	Branch addr
CCJS1	<1>	Count by INC/goto SR1	Stop addr

Table 3 Typical instruction sequence for Fig.8

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} (Industrial) = –40°C to + 85°C, V_{CC} = 5.0V ± 10%, GND = 0V

T_{amb} (Military) = –55°C to + 125°C, V_{CC} = 5.0V ± 10%, GND = 0V

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4			V	I_{OH} = 8mA
Output low voltage	V_{OL}			0.6	V	I_{OL} = -8mA
Input high voltage	V_{IH}	2.2			V	
Input low voltage	V_{IL}			0.8	V	
Input leakage current	V_{IL}	-10		10	μA	GND ≤ Vin ≤ Vcc
Output leakage current	I_{OZ}	-50		50	μA	GND ≤ V_{OUT} ≤ Vcc = Vcc max.
Output short cct current (Note 2)	I_{OS}	40		250	mA	Vcc = max.
Input capacitance	C_{IN}		9		pF	LC package
			12		pF	DG package

Switching Characteristics

Characteristic	Value				Units	Conditions
	Industrial		Military			
	PDSP1640 B0		PDSP1640 A0			
	Min.	Max.	Min.	Max.		
CLK frequency		20		20	MHz	
CLK high period	20		20		ns	
CLK low period	15		15		ns	
CLK to CO		44		44	ns	1 LSTTL + 5pF load
CLK to DO		34		34	ns	2 LSTTL + 20pF load Opcode 3
CLK to DO		28		28	ns	2 LSTTL + 20pF load, remainingOpcodes
CLK to COMP		35		35	ns	50pF load (Opcodes 0, 1, 2)
CI to CO		20		20	ns	1 LSTTL + 5pF load
Setup DI to CLK	10		10		ns	
Hold DI to CLK	3		3		ns	
Setup CI to CLK	20		20		ns	
Hold CI to CLK	3		3		ns	
Setup I to CLK	15		15		ns	
Hold I to CLK	3		3		ns	
Setup CCEN to CLK	30		30		ns	
Hold CCEN to CLK	0		0		ns	
$\overline{OE}$ high to DO high Z		30		30	ns	See $\overline{OE}$ test diagrams, Fig. 9
$\overline{OE}$ low to DO/COMP valid		22		22	ns	
V_{CC} current		20		20	mA	V_{CC} = Max., outputs unloaded, CLK freq = Max.

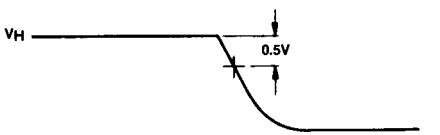
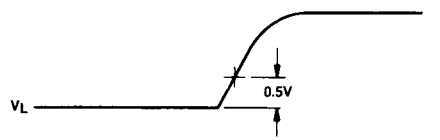
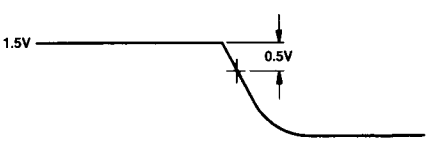
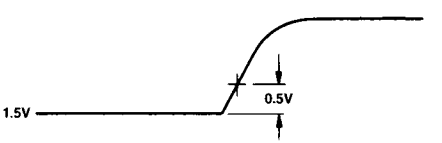
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage V_{CC}	-0.5 to 7.0V
Input voltage V_{IN}	-0.9 to V_{CC} +0.9V
Output voltage V_{OUT}	-0.9 to V_{CC} +0.9V
Clamp diode current per pin I_K (see Note 2)	±18mA
Static discharge voltage (HMB)	500V
Storage temperature range T_S	-65°C to +150°C
Ambient temperature with power applied T_{amb}	
Military	-55°C to +125°C
Industrial	-40°C to +85°C
Junction temperature	150°C
Package power dissipation	1000mW

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Package Type	θ_{JC} °C/W	θ_{JA} °C/W
DG	12	40
LC	13	56

Test	Waveform - measurement level
Delay from output high to output high impedance	
Delay from output low to output high impedance	
Delay from output high impedance to output low	
Delay from output high impedance to output high	

NOTES
1. V_H - Voltage reached when output driven high.
2. V_L - Voltage reached when output driven low.

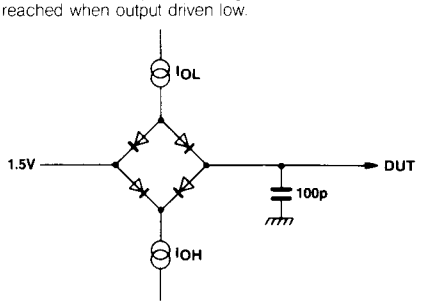


Fig.9 Three state delay measurement load

ORDERING INFORMATION

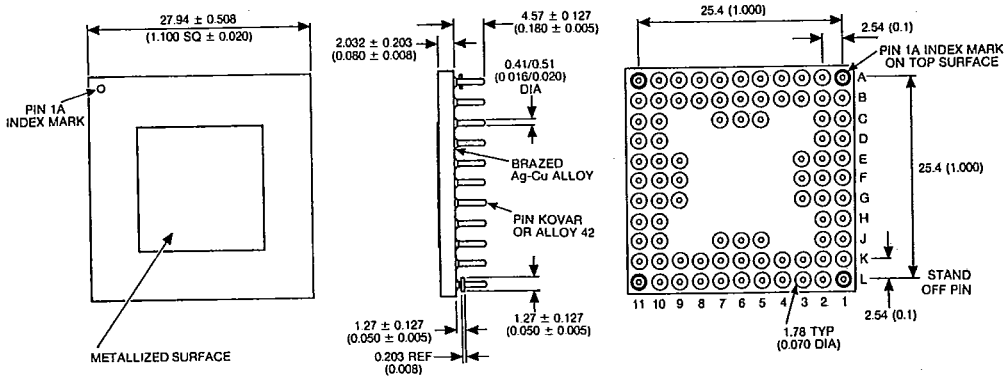
Industrial (-40°C to +85°C)

PDSP1640 B0 DG (Ceramic DIL package)
PDSP1640 B0 LC (Leadless chip carrier)

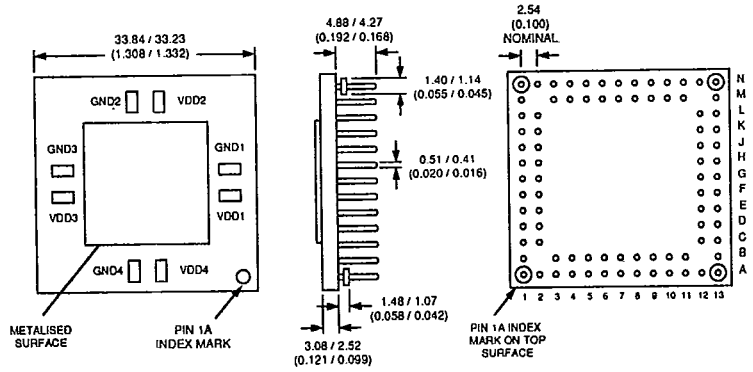
Military (-55°C to +125°C)

PDSP1640 A0 DG (Ceramic DIL package)
PDSP1640 A0 LC (Leadless chip carrier)

T-90-20

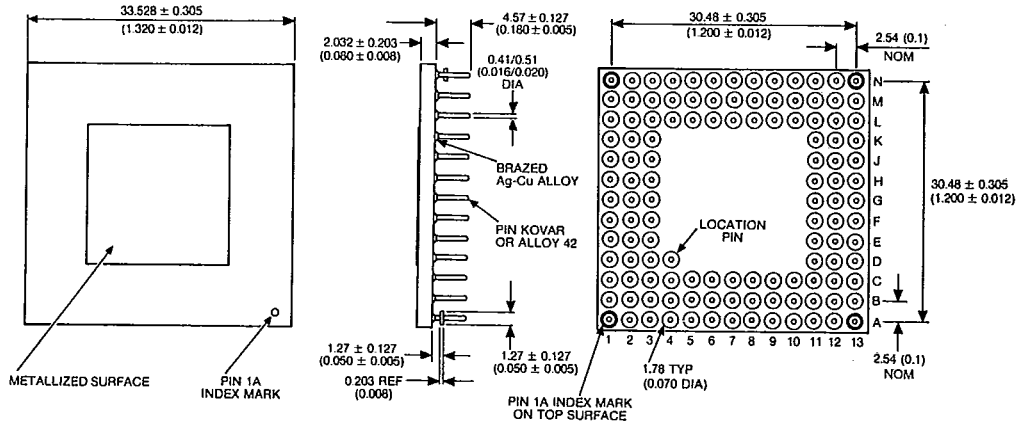


84-PIN GRID ARRAY PACKAGE — AC84

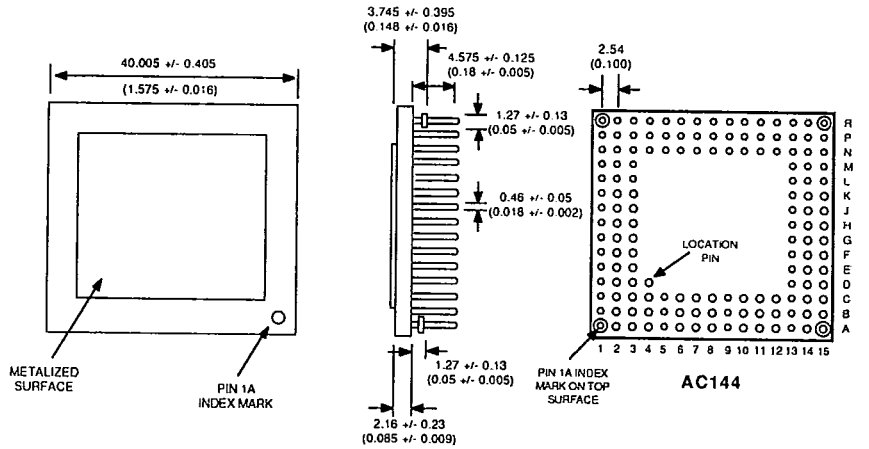


84-PIN GRID ARRAY POWER PACKAGE - AC84

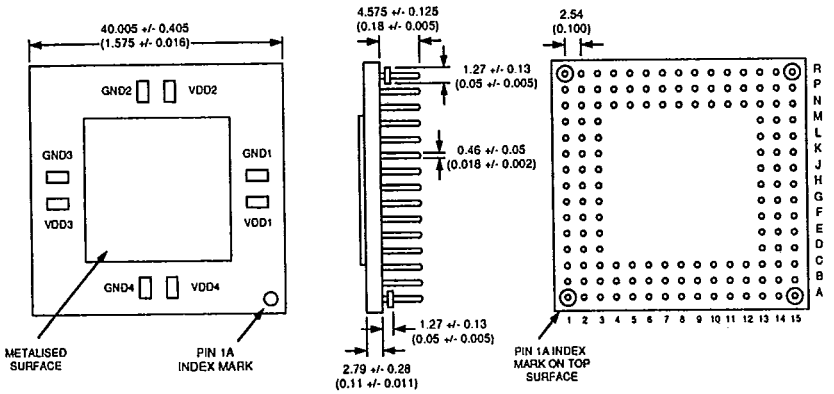
(Used for the PDSP 16340, PDSP16350, PDSP16488 and PDSP16510)



120-PIN GRID ARRAY PACKAGE — AC120

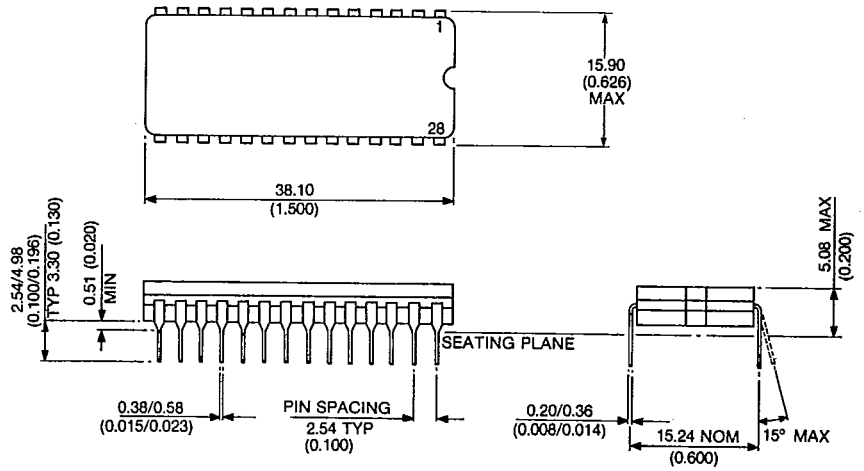


144-PIN GRID ARRAY PACKAGE - AC144

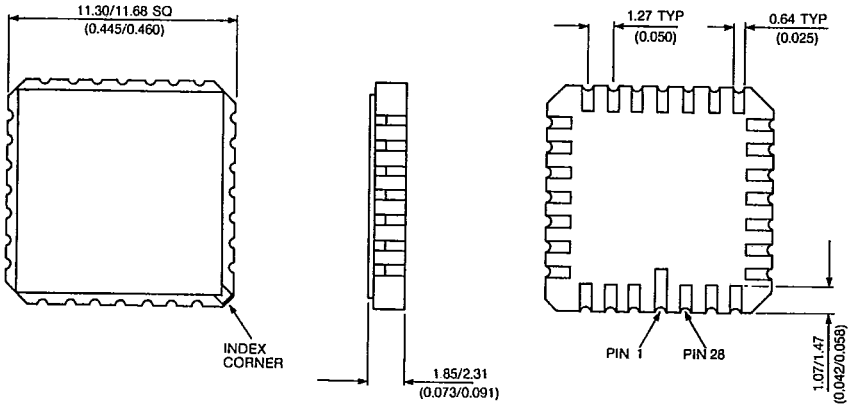


144-PIN GRID ARRAY POWER PACKAGE - AC144

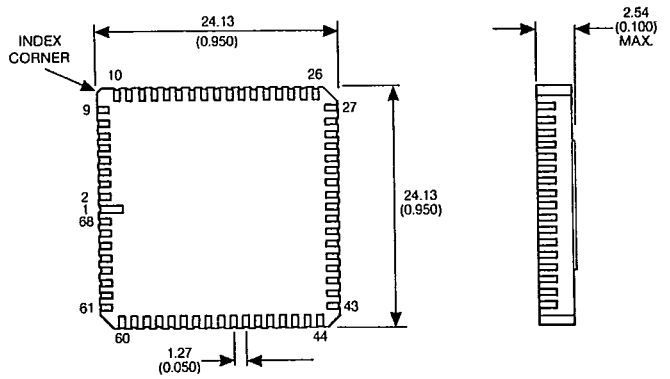
(Used for the PDSP 16256)



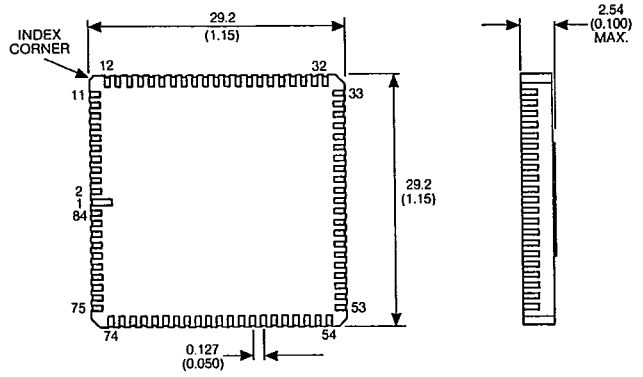
28-LEAD CERAMIC DIL - DG28



28-PIN LEADLESS CHIP CARRIER - LC28
(HERMETIC)



68 CONTACT LCC PACKAGE — LC68



84-PIN LEADLESS CHIP CARRIER - LC84 (HERMETIC)