

54LS138, 54S138 Decoders/Demultiplexers

Military Logic Products

1-of-8 Decoder/Demultiplexer

Product Specification

FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Direct replacement for Intel S205

DESCRIPTION

The '138 decoder accepts three binary weighted inputs (A_0 , A_1 , A_2) and when enabled, provides eight mutually exclusive, active Low outputs (0 - 7). The device features three Enable inputs: two active Low

(E_1 , E_2) and one active High (E_3). Every output will be High unless E_1 and E_2 are Low and E_3 is High. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four '138s and one inverter.

The device can be used as an eight output demultiplexer by using one of the active Low Enable inputs as the Data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active High or active Low state.

ORDERING INFORMATION

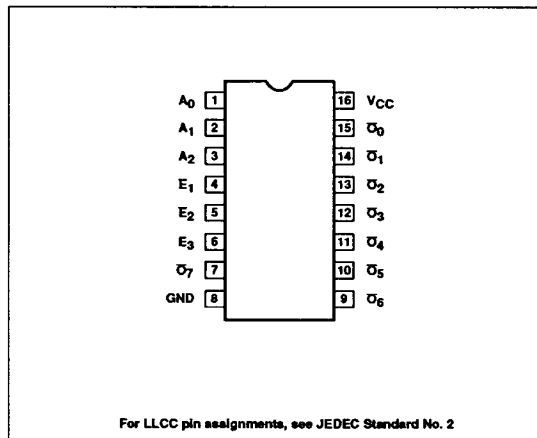
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS138/BEA, 54S138/BEA
16-Pin Ceramic FlatPack	54LS138/BFA, 54S138/BFA
16-Pin Ceramic LLCC	54LS138/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

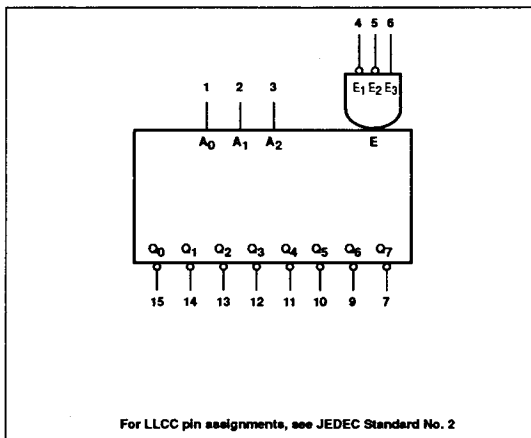
PINS	DESCRIPTION	54S	54LS
All	Inputs	1SUL	1LSUL
All	Outputs	10SUL	10LSUL

NOTE: Where a 54S Unit Load (SUL) is 50 μ A I_{IH} and -2.0mA I_{IL} , and 54LS Unit Load (LSUL) is 20 μ A I_{IH} and -0.4mA I_{IL} .

PIN CONFIGURATION



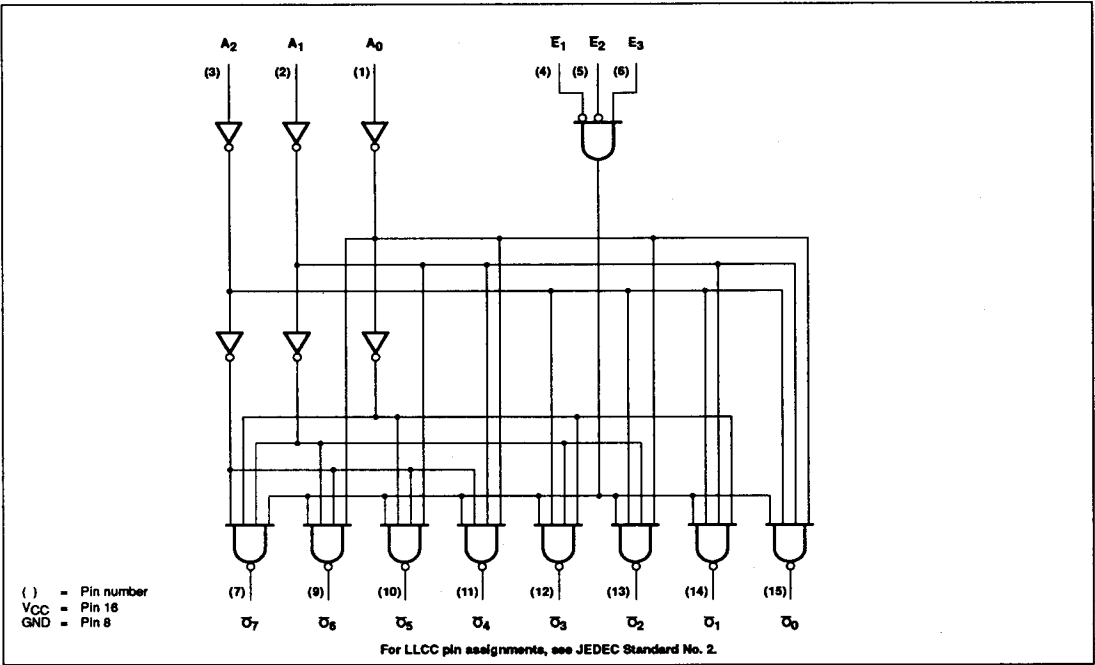
LOGIC SYMBOL



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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS							
E ₁	E ₂	E ₃	A ₀	A ₁	A ₂	0	1	2	3	4	5	6	7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	L	L	H	H	H	H	H	H
L	L	H	L	H	L	L	H	L	H	H	H	H	H
L	L	H	H	H	L	L	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54LS	54S	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _I	Input voltage range	-0.5 to +7.0	-0.5 to +7.0	V
I _I	Input current range	-30 to +1	-30 to +5	mA
V _O	Voltage applied to output in High output state range	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _{STG}	Storage temperature range	-65 to +150		°C

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54LS			54S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			2.0			V
V _{IL}	Low-level input voltage			+0.7			+0.8	V
I _{IK}	Input clamp current			-18			-18	mA
I _{OH}	High-level output current			-400			-1000	μA
I _{OL}	Low-level output current			4			20	mA
T _A	Operating free-air temperature range	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	54LS138			54S138			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH}	High-level output voltage	V _{CC} = Min, V _{IH} = Min, V _{IL} = Max, I _{OH} = Max	2.5	3.4		2.5	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = Min, V _{IH} = Min, V _{IL} = Max, I _{OL} = Max		0.25	0.4			0.5	V
V _{IK}	Input clamp voltage	V _{CC} = Min, I _I = I _{IK}			-1.5			-1.2	V
I _{IH2}	Input current at maximum input voltage	V _{CC} = Max	V _I = 5.5V						1.0
			V _I = 7.0V						mA
I _{IH1}	High-level input current	V _{CC} = Max, V _I = 2.7V			20			50	μA
I _{IL}	Low-level input current	V _{CC} = Max	V _I = 0.4V						mA
			V _I = 0.5V						-2
I _{OS}	Short-circuit output current ³	V _{CC} = Max	-20		-100	-40		-110	mA
I _{CC}	Supply current ⁴ (total)	V _{CC} = Max		6.3	10		49	74	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54LS ⁵		54S		UNIT
			C _L = 15pF		C _L = 15pF		
			Min	Max	Min	Max	
t _{PLH}	Propagation delay Address to output	Waveform 2 2 logic levels		20		7	ns
t _{PHL}				41		10.5	ns
t _{PLH}	Propagation delay Address to output	Waveform 1 3 logic levels		27		12	ns
t _{PHL}				39		12	ns
t _{PLH}	Propagation delay Enable to output	Waveform 2 2 logic levels		18		8	ns
t _{PHL}				32		11	ns
t _{PLH}	Propagation delay Enable to output	Waveform 1 3 logic levels		26		11	ns
t _{PHL}				38		11	ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S ⁵		UNIT
			C _L = 50pF		C _L = 50pF		
			Min	Max	Min	Max	
t _{PLH}	Propagation delay Address to output	Waveform 2 2 logic levels		25		9.5	ns
t _{PHL}				46		13.0	ns
t _{PLH}	Propagation delay Address to output	Waveform 1 3 logic levels		32		14.5	ns
t _{PHL}				44		14.5	ns
t _{PLH}	Propagation delay Enable to output	Waveform 2 2 logic levels		23		10.5	ns
t _{PHL}				37		13.5	ns
t _{PLH}	Propagation delay Enable to output	Waveform 1 3 logic levels		31		13.5	ns
t _{PHL}				43		13.5	ns

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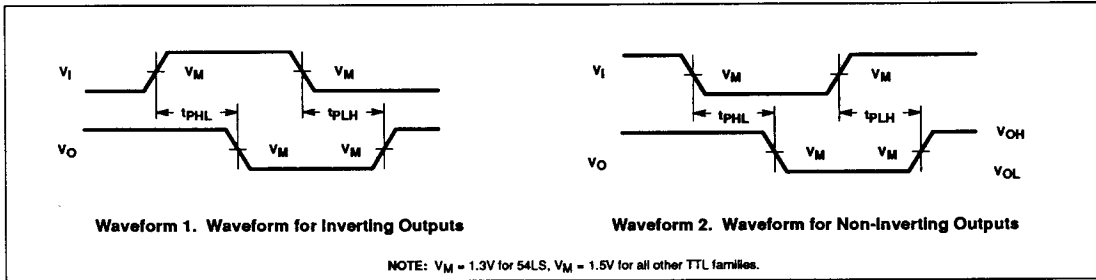
AC ELECTRICAL CHARACTERISTICS $T_A = -55^{\circ}\text{C}$ and $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V}^6$

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			C _L = 50pF		C _L = 50pF		
			Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Address to output	Waveform 2 2 logic levels		32 59		12.5 17	ns ns
t _{PLH} t _{PHL}	Propagation delay Address to output	Waveform 1 3 logic levels		41 57		19 19	ns ns
t _{PLH} t _{PHL}	Propagation delay Enable to output	Waveform 2 2 logic levels		30 48		13.5 17.5	ns ns
t _{PLH} t _{PHL}	Propagation delay Enable to output	Waveform 1 3 logic levels		40 56		17.5 17.5	ns ns

NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. To measure I_{CC} , outputs must be enabled and open.
5. These parameters are guaranteed, but not tested.

AC WAVEFORMS



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TEST CIRCUIT AND WAVEFORM

