REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
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SHEET	15	16																		

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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APPROVED BY

DRAWING APPROVAL DATE 92-03-11

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS, 4 X 8-BIT MULTILEVEL PIPELINE REGISTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-91762

SHEET 1

DESC FORM 193
JUL 91

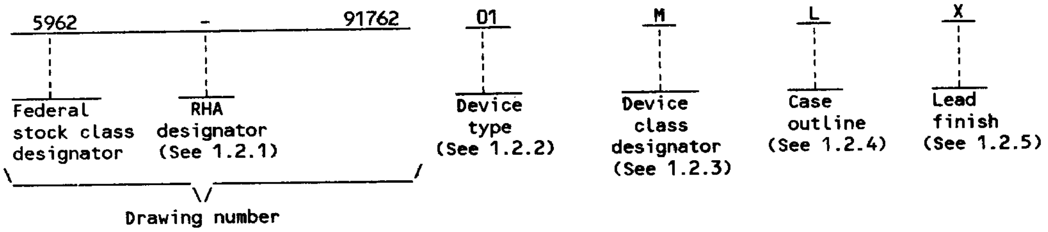
5962-E451

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Propagation Delay
01	L29C520	4 x 8-bit multilevel pipeline register	30 ns
02	L29C520	4 x 8-bit multilevel pipeline register	24 ns
03	L29C520	4 x 8-bit multilevel pipeline register	16 ns
04	L29C521	4 x 8-bit multilevel pipeline register	30 ns
05	L29C521	4 x 8-bit multilevel pipeline register	24 ns
06	L29C521	4 x 8-bit multilevel pipeline register	16 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). For device classes M, B, and S, case outline(s) shall meet the requirements in appendix C of MIL-M-38510 and as listed below. For device classes Q and V, case outline(s) shall meet the requirements of MIL-I-38535, appendix C of MIL-M-38510, and as listed below.

Outline letter	Case outline
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
3	C-4 (28-terminal, .460" x .460" x .100" maximum), square leadless chip carrier package
K	F-6 (24-lead, .640" x .420" x .090"), flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Storage temperature	-65°C to +150°C
Operating ambient temperature	-55°C to +125°C
V_{CC} supply voltage with respect to ground	-0.5 V to +7.0 V
Input signal with respect to ground	-3.0 V to +7.0 V
Signal applied to high impedance output	-3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-M-38510, appendix C
Power dissipation (P_D)	250 mW
Junction temperature	+175°C
Lead temperature (soldering, 10 seconds)	+275°C

1.4 Recommended operating conditions.

Supply voltage	$4.50\text{ V} \le V_{CC} \le 5.50\text{ V}$
Operating case temperature (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY
MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY
MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY
MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY
MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Values will be added when they become available.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block diagram. The functional block diagram shall be as specified on figure 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 40 (see MIL-M-38510, appendix E).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified 1/		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, V_{IN} = 0.8 V, 2.0 V	I_{OH} = -15 mA	1,2,3	All	2.4		V
Output low voltage	V_{OL}		I_{OL} = 24 mA	1,2,3	All		0.5	V
Input high voltage	V_{IH}			1,2,3	All	2.0	V_{CC}	V
Input low voltage	V_{IL}	2/		1,2,3	All		0.8	V
Input current	I_{IX}	Ground $\le V_{IN} \le V_{CC}$		1,2,3	All		±20	µA
Output leakage current	I_{OZ}	Ground $\le V_{OUT} \le V_{CC}$		1,2,3	All		±20	µA
Output short current	I_{OS}	V_{OUT} = Ground, V_{CC} = 5.5 V 3/ 4/		1,2,3	All		-125	mA
V_{CC} current, dynamic	I_{CC1}	5/ 6/		1,2,3	All		30	mA
V_{CC} current, quiescent	I_{CC2}	7/		1,2,3	All		1.5	mA
Input capacitance	C_{IN}	See 4.4.1c		4	All		12	pF
Output capacitance	C_{OUT}	See 4.4.1c		4	All		10	pF
Functional tests		See 4.4.1b, V_{CC} = 4.5 V, 5.5 V		7,8	All			
CLK to Y_7-Y_0	t_{PD}	V_{CC} = 4.5 V, 8/ 9/ see figure 4		9,10,11	01,04		30	ns
					02,05		24	ns
					03,06		16	ns
S_1, S_0 to Y_7-Y_0	t_{SEL}			9,10,11	01,04		30	ns
					02,05		22	ns
					03,06		15	ns
D_7-D_0 to CLK setup	t_{SD}			9,10,11	01,04	15		ns
					02,05	10		ns
					03,06	6		ns
CLK to D_7-D_0 hold	t_{HD}			9,10,11	01,04	5		ns
					02,05	3		ns
					03,06	2		ns
I_1, I_0 to CLK setup	t_{SI}			9,10,11	01,04	15		ns
					02,05	10		ns
					03,06	6		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ $4.5\ V \leq V_{CC} \leq 5.5\ V$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CLK to I_1, I_0 hold	t_{HI}	V_{CC} = 4.5 V, 8/ 9/ see figure 4	9,10,11	01,04	5		ns
				02,05	3		ns
				03,06	2		ns
$\overline{OE}$ to output disable	t_{DIS}	V_{CC} = 4.5 V, 8/ 9/ 10/ see figure 4	9,10,11	01,04		20	ns
				02,05		16	ns
				03,06		13	ns
$\overline{OE}$ to output enable	t_{ENA}		9,10,11	01,04		25	ns
				02,05		22	ns
				03,06		16	ns
Clock pulse width	t_{PW}	V_{CC} = 4.5, 8/ 9/ see figure 4	9,10,11	01,04	15		ns
				02,05	10		ns
				03,06	8		ns

See footnotes on next page.

TABLE I. Electrical performance characteristics - Continued.

1/ All testing shall be conducted at worst-case conditions, unless otherwise specified.

2/ This device provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at GND - 0.6 V.

3/ Duration of the output short circuit should not exceed 30 seconds.

4/ These parameters are guaranteed but not 100 percent tested.

5/ Supply current for a given application can be accurately approximated by: $(NCV^2F)/4$, where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6/ Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7/ Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8/ AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENA} and t_{DIS} measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

9/ Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of the external system driving the chip. Setup time, for example is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as maximum since worst-case operation of any device always provides data within that time.

10/ Transition is measured ±200 mV from steady-state voltage with specified loading.

Device type	All				
Case outline	L and K	3	Case outline	L and K	3
Terminal number	Terminal symbol	Terminal symbol	Terminal number	Terminal symbol	Terminal symbol
1	I_0	I_0	15	Y_6	$\overline{OE}$
2	I_1	I_1	16	Y_5	Y_7
3	D_0	D_0	17	Y_4	Y_6
4	D_1	NC	18	Y_3	NC
5	D_2	D_1	19	Y_2	Y_5
6	D_3	D_2	20	Y_1	Y_4
7	D_4	D_3	21	Y_0	Y_3
8	D_5	D_4	22	S_1	Y_2
9	D_6	D_5	23	S_0	Y_1
10	D_7	D_6	24	V_{CC}	Y_0
11	CLK	NC	25	---	NC
12	GND	D_7	26	---	S_1
13	$\overline{OE}$	CLK	27	---	S_0
14	Y_7	GND	28	---	V_{CC}

NC = No Connection.

FIGURE 1. Terminal connections.

Device type		01, 02, 03				04, 05, 06			
I_1	I_0	R1	R2	R3	R4	R1	R2	R3	R4
L	L	D → R1	R1 → R2	R2 → R3	R3 → R4	D → R1	R1 → R2	R2 → R3	R3 → R4
L	H	HOLD	HOLD	D → R3	R3 → R4	HOLD	HOLD	D → R3	HOLD
H	L	D → R1	R1 → R2	HOLD	HOLD	D → R1	HOLD	HOLD	HOLD
H	H	HOLD	HOLD	HOLD	HOLD	HOLD	HOLD	HOLD	HOLD

Device type		All
S_1	S_0	Register selected
L	L	Register 4
L	H	Register 3
H	L	Register 2
H	H	Register 1

FIGURE 2. Truth table.

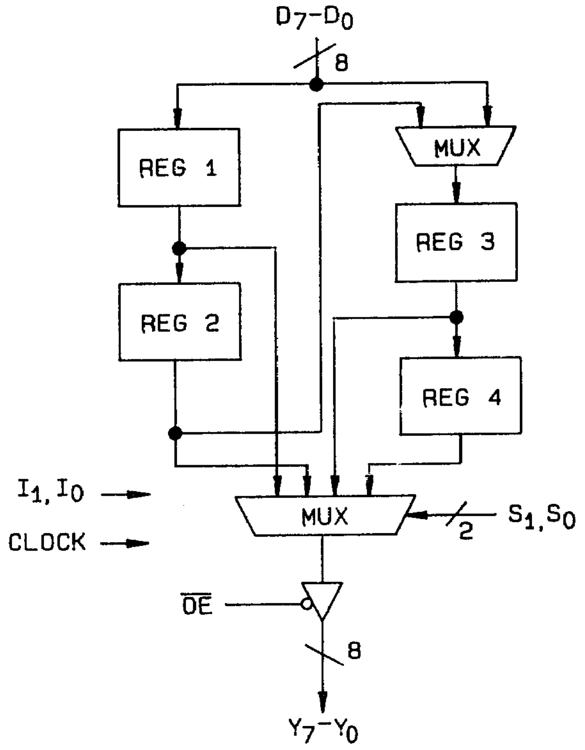


FIGURE 3. Functional block diagram.

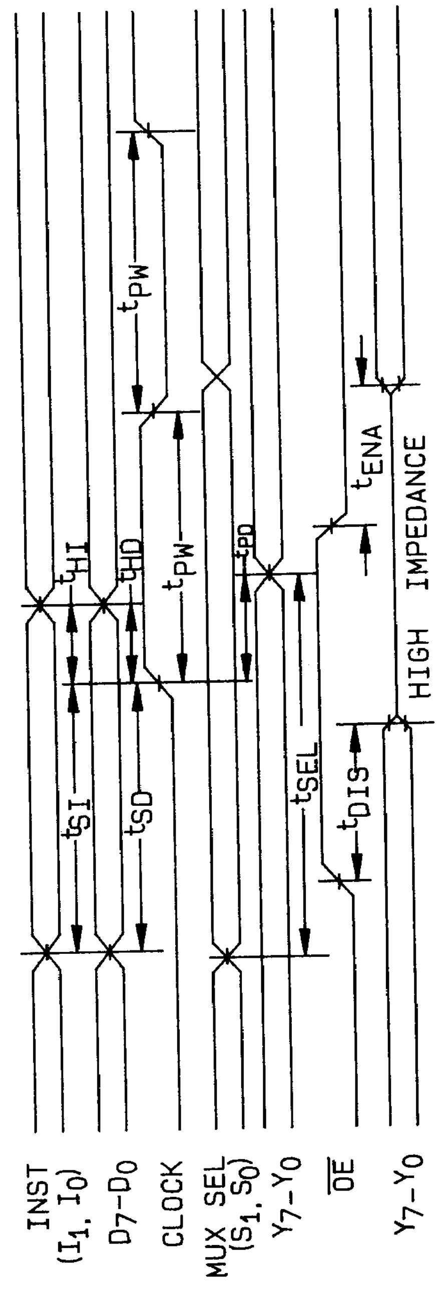


FIGURE 4. Switching waveforms.

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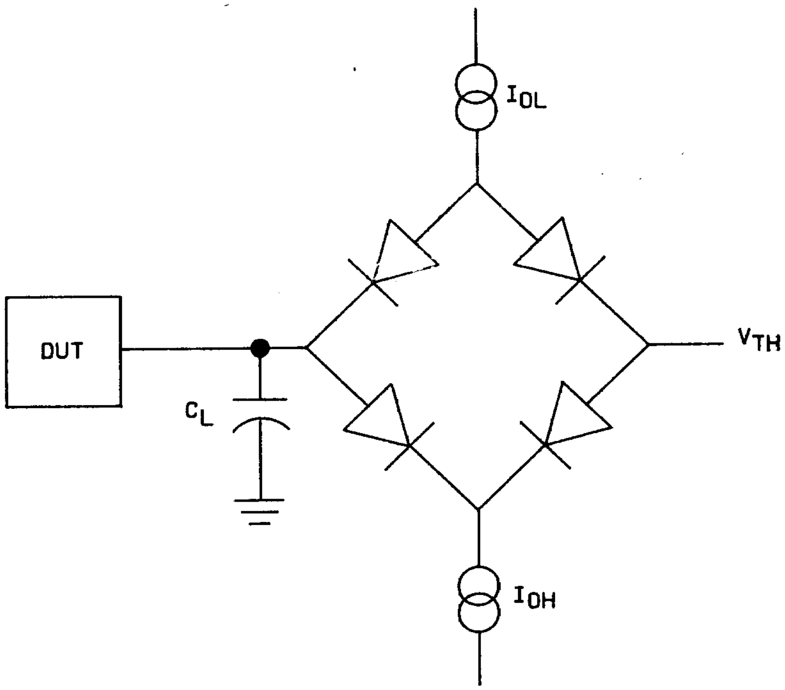

NOTE: Test conditions shall be as follows: C_L = 30 pF, V_{TH} = 1.5 V, I_{OL} = 8 mA, I_{OH} = -2 mA for all ac parameters with the exception of t_{ENA}/t_{DIS}. For t_{ENA}/t_{DIS}, test conditions shall be: C_L = 30 pF, V_{TH} = steady-state - 0.2 V, I_{OL} = 10 mA, I_{OH} = 10 mA.

FIGURE 4. Switching waveforms and test circuit - Continued.

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall consist of verifying the functionality of the device. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 ($C_{I/O}$ measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)		1,7,9	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1/ 1, 2,3,7,8, 9,10,11	2/ 1, 2,3,7,8, 9,10,11	2/ 1, 2,3,7,8 9,10,11	1/ 1, 2,3,7,8 9,10,11	1/ 1, 2,3,7,8, 9,10,11
Group A test requirements (see 4.4)	1,2,3,4, 7,8,9, 10,11	1,2,3,4, 7,8,9, 10,11	1,2,3,4, 7,8,9, 10,11	1,2,3,4, 7,8,9, 10,11	1,2,3,4, 7,8,9, 10,11
Group B end-point electrical parameters (see 4.4)			1,7,9		1,7,9
Group C end-point electrical parameters (see 4.4)	1,7,9	1,7,9		1,7,9	
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device classes M, B, and S. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
Reverse bias burn-in	1015	100%
Burn-in	1015, total of 240 hours at +125°C	100%
Radiographic	2012	100%

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IIA herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table IIA herein.

d. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes M, B, and S, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-8526.

6.4 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8526.

6.5 Symbols, definitions, and functional descriptions. See table III.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.

TABLE III. Pin descriptions.

Symbol	Functional description
D_7 - D_0	Data inputs
I_1, I_0	Instruction inputs (see figure 2)
S_1, S_0	Register select inputs (see figure 2)
CLK	System clock
$\overline{OE}$	Output enable; when a high level is applied to this pin, it forces outputs into the high-impedance state.
Y_7 - Y_0	Data outputs
GND	System ground
V_{CC}	System power supply

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