82HS189
82HS189A
8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82HS189 is a programmable read only memory containing D-type, master-slave data registers. The 82HS189 contains 1024 words of 8 bits each. The unprogrammed state is with all outputs at a High level and can be selectively programmed to a Low level by following the Signetics Generic II programming method. The output structure is 3-State for ease in connection to bus-organized systems. The combination of on-chip registers and 3-State outputs will substantially reduce cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register.

All outputs will go into the third state or Hi-Z condition if the Asynchronous Chip Enable ($\overline{G}$) is held High. The outputs are enabled when ($\overline{GS}$) is brought Low before the rising edge of the clock and ($\overline{G}$) is held Low. The ($\overline{GS}$) flip-flop is designed to power-up in the third state or Hi-Z condition with the application of V_{CC}.

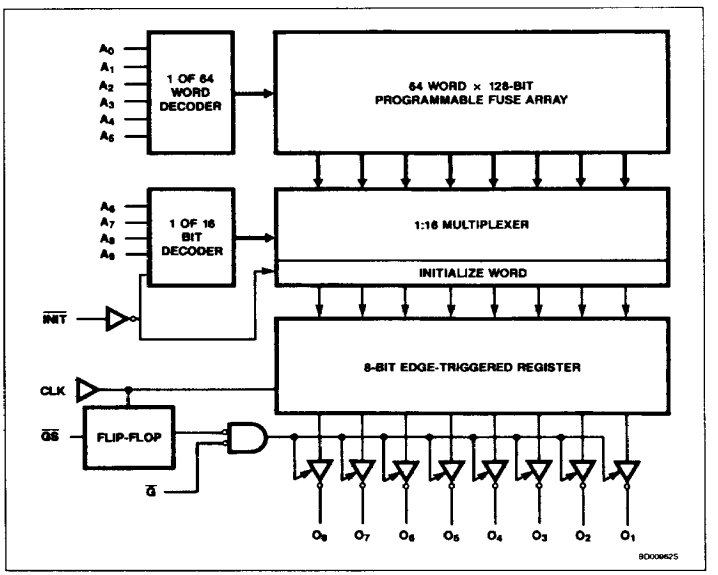
The 82HS189 also features an initialize function, $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single-pin control by applying a Low on $\overline{INIT}$. The initialize function is synchronous and is loaded into the Output Register on the next rising edge of the clock. The unprogrammed state of $\overline{INIT}$ is all ones.

Data is read from the PROM by first applying an address to inputs A_0 to A_9. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (Low-to-High transition) of the clock, the data is transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition, the Addresses and Synchronous Chip Enable can be removed and the output data will remain stable.

FEATURES

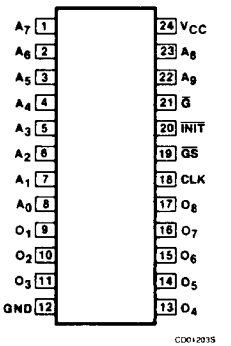
- **On-chip edge-triggered registers**
- **Asynchronous and Synchronous Enables for word expansion**
- **Programmable register with synchronous initialize function**
- **24-pin 300mil-wide package**
- **Read cycle "Address setup plus clock to output delay"**
  - **N82HS189: 55ns max**
  - **N82HS189A: 45ns max**
- **Unprogrammed outputs are High level**
- **Outputs: 3-State**

BLOCK DIAGRAM

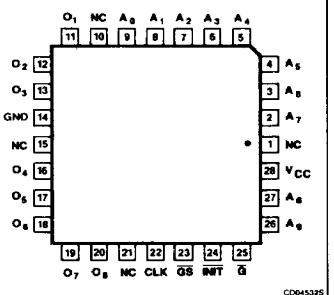


PIN CONFIGURATIONS

N Package



A Package



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 300mil-wide	N82HS189 N • N82HS189A N
28-pin Plastic Leaded Chip Carrier 450mil-square	N82HS189 A • N82HS189A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage[2]						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	$I_{IN} = -18mA$		−0.8	−1.2	V
Output voltage[2]						
V_{OL}	Low	$\overline{G}$, $\overline{GS}$ = Low $I_{OUT} = 16mA$			0.5	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			V
Input current[1]						
I_{IL}	Low	$V_{IN} = 0.45V$			−250	μA
I_{IH}	High	$V_{IN} = 5.25V$			40	μA
Output current[1]						
I_{OZ}	Hi-Z State	$\overline{G}$ = High, $V_{OUT} = 5.25V$			40	μA
		$\overline{G}$ = High, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit[3]	$\overline{G}$, $\overline{GS}$ = Low, $V_{OUT} = 0V$ High stored	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		125	175	mA
Capacitance						
C_{IN}	Input	$\overline{G}$ = High, $V_{CC} = 5.0V$ $V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

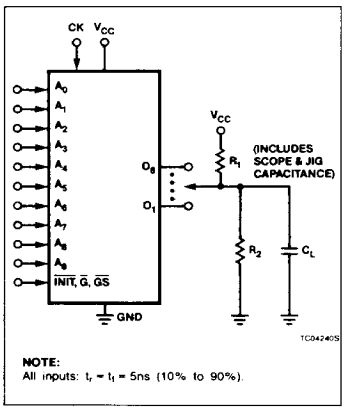
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER[4]	TO	FROM	N82HS189			N82HS189A			UNIT
				Min	Typ[5]	Max	Min	Typ	Max	
t_{CSA} t_{CHA}	Setup Hold	CLK	Address	35 0			30 0			ns
t_{OC}	Delay	Output	CLK		10	20	0		15	ns
t_{WC}	Width	H & L	CLK	20	10		15			ns
t_{CSGS} t_{CHGS}	Setup Hold	CLK	$\overline{GS}$	15 5			10 5			ns
t_{CSIN} t_{CHIN}	Setup Hold	CLK	$\overline{INIT}$	25 0	8		20 0			ns
t_{OG}	Delay	Output	$\overline{G}$		11	25			20	ns
t_{OZC}[6]	Delay	Output	CLK		16	25			20	ns
t_{OZG}[6]	Delay	Output	$\overline{G}$		14	25			20	ns

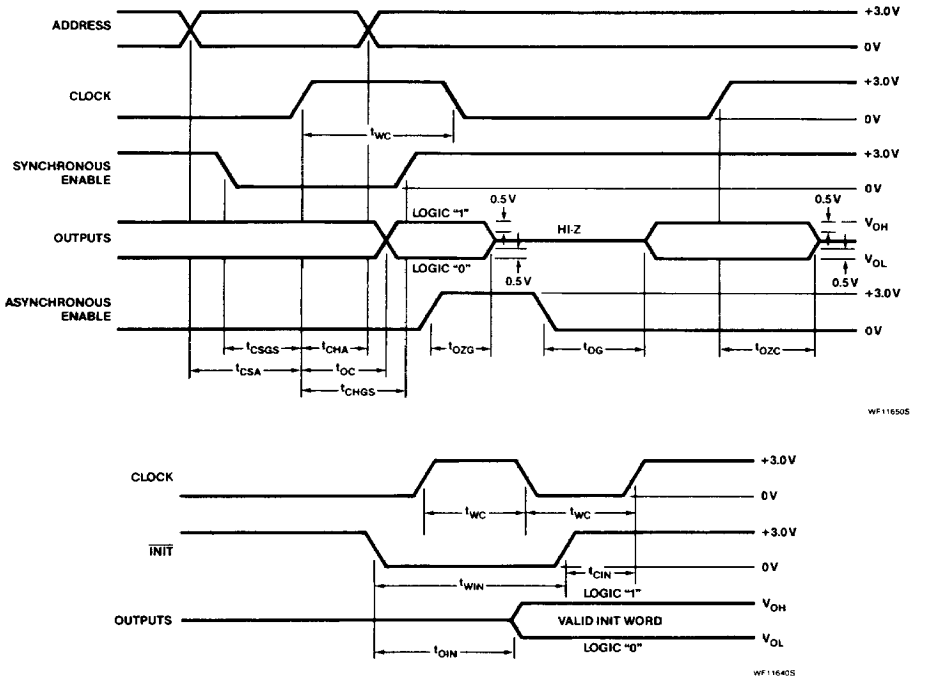
NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



NOTE:
All inputs: $t_r = t_f = 5ns$ (10% to 90%).

VOLTAGE WAVEFORMS



NOTE:
All AC parameters are measured at 1.5V unless otherwise specified.