Preliminary

Am29CPL141/Am29CPL151

CMOS Field Programmable Controller (FPC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Implements complex state machines**
- **High-speed, low-power CMOS EPROM technology**
- **Direct plug-in replacement for the bipolar Am29PL141**
- **Seven conditional inputs (each can be registered as a programmable option), 16 outputs**
- **64-word by 32-bit CMOS EPROM**
- **Up to 30-MHz clock rate**
- **Available in a wide selection of 28-pin packages, including SKINNYDIP™**
  0.6" CERDIP windowed, 0.3" CERDIP windowed, 0.3" plastic DIP OTP, PLCC OTP
- **29 instructions**
  Conditional branching, conditional looping, conditional subroutine call, multiway branch

GENERAL DESCRIPTION

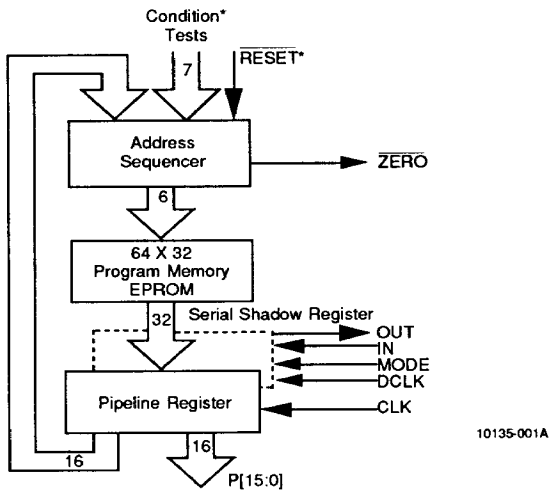
The Am29CPL141, a direct plug-in replacement for the Am29PL141, is a CMOS, single-chip Field Programmable Controller (FPC). It allows implementation of complex state machines and controllers by programming the appropriate sequence of instructions. Jumps, loops, and subroutine calls, conditionally executed based on the test inputs, provide the designer with powerful control flow primitives.

Intelligent control may be distributed throughout the system by using FPCs to control various self-contained functional units, such as register file/ALU, I/O, interrupt, diagnostic, and bus control units. An Address sequencer, the heart of the FPC, provides the address to an internal 64-word by 32-bit EPROM.

The Am29CPL151 is electrically and functionally identical to the Am29CPL141 but is manufactured in a space-saving 300 mil DIP package as well as being offered in surface mount packaging.

This UV-erasable and reprogrammable device utilizes proven floating-gate CMOS EPROM technology to ensure high reliability, easy programming, and better than 99.9% programming yields. The Am29CPL141/151 is offered in both windowed and One-Time Programmable (OTP) packages. OTP plastic DIP and PLCC devices are ideal for volume production.

SIMPLIFIED BLOCK DIAGRAM



*Each condition test input can be individually registered as a programmable option; the RESET input can be registered as a programmable option.

SKINNYDIP is a trademark of Advanced Micro Devices, Inc.

Publication #	Rev.	Amendment
10135	B	/0

Issue Date: May 1989

Part No.	Technology	Memory	Word	Input	Output	Package
Am29CPL141	CMOS	EPROM	64	7	16	600 mil 28-pin CERDIP Windowed
Am29CPL142	CMOS	EPROM	128	8	16	600 mil 28-pin CERDIP Windowed
Am29CPL151	CMOS	EPROM	64	7	16	300 mil 28-pin CERDIP Windowed Plastic OTP, PLCC OTP
Am29CPL152	CMOS	EPROM	128	8	16	300 mil 28-pin CERDIP Windowed, Plastic OTP, PLCC OTP
Am29CPL154	CMOS	EPROM	512	8	16	300 mil 28-pin CERDIP Windowed, Plastic OTP, PLCC OTP

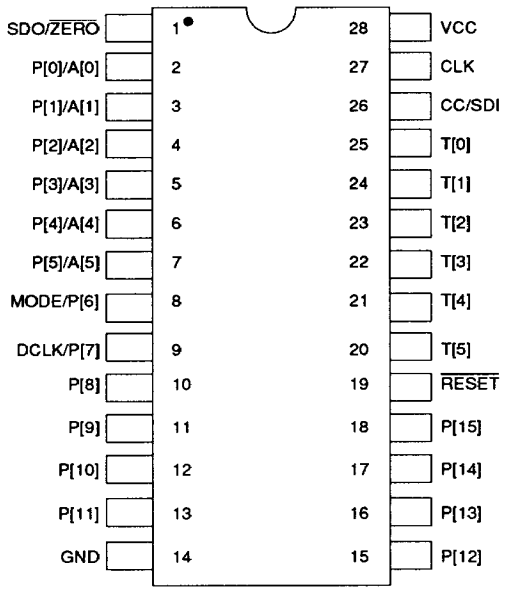
RELATED AMD PRODUCTS

Part No	Description
Am27S35A	1024 x 8 Registered PROM
Am29C01	CMOS 4-Bit Slice Microprogrammable CPU
Am2914	Vectored Priority Interrupt Controller
Am2925	Clock Generator
Am2940	DMA Address Generator
Am29C101	CMOS 16-Bit Microcontroller Slice
Am29C116	CMOS 16-Bit Microprocessor
Am29C117	CMOS 2-Port Version of Am29C116
Am29C3XX	CMOS 32-Bit Microprogrammable Family
Am29C325	CMOS Single-Precision Floating-Point Processor
Am29C327	CMOS Double Precision Floating-Point Processor
Am29C8XX	CMOS High-Performance Bus Interface Family
Am29C818	CMOS SSR™ Diagnostics Pipeline Register

SSR is a trademark of Advanced Micro Devices, Inc.

CONNECTION DIAGRAMS
Top View

DIP*



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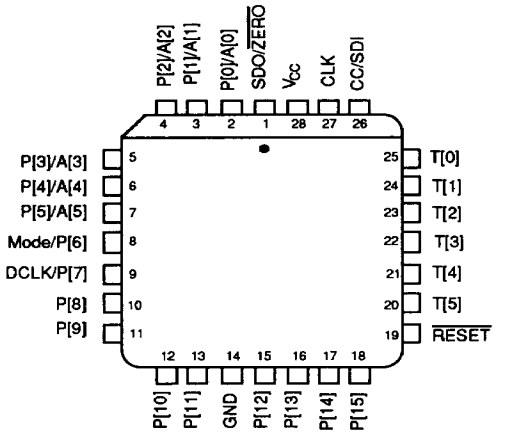
PLCC*



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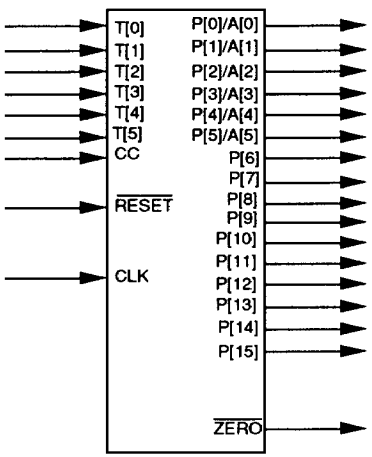
Note: Pin 1 is marked for orientation.

*Also available in 28-pin LCC; pinout identical to PLCC. Plastic DIP and PLCC are One-Time Programmable (OTP), non-windowed packages.

LOGIC SYMBOLS



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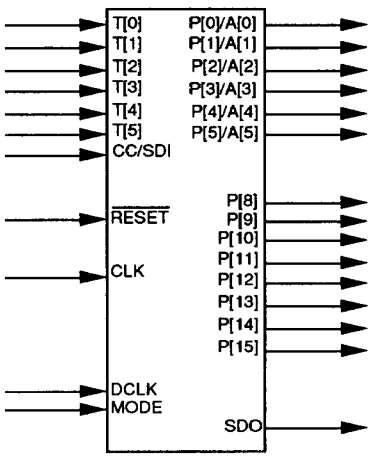
Normal Configuration



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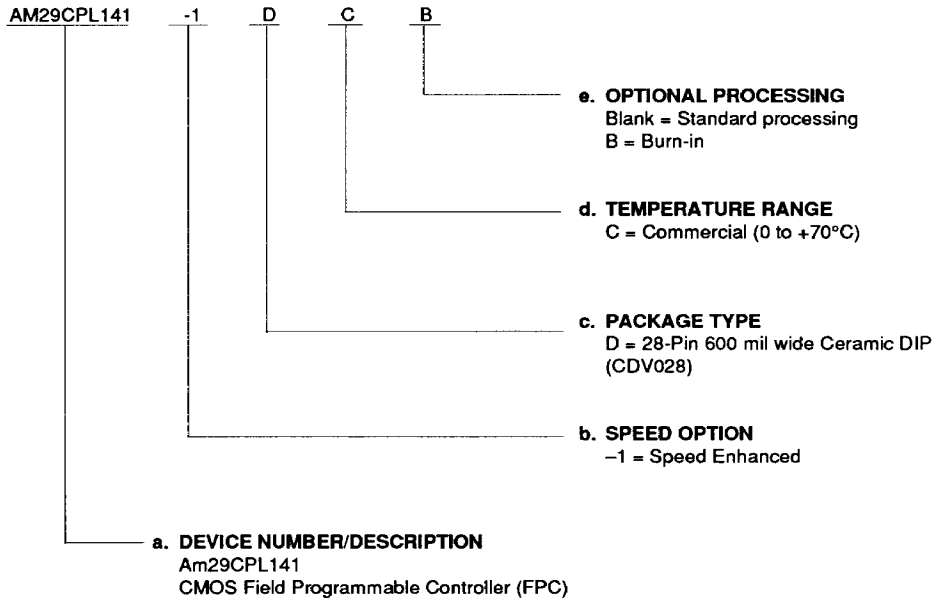
SSR Diagnostics Configuration

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29CPL141	DC, DCB
AM29CPL141-1	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

Note: The Am29CPL141 is the ordering part number for devices packaged in 28-pin, 0.6" ceramic windowed DIP packages. All specifications and functional description in this data sheet refer equally to the Am29CPL141 and Am29CPL151 except for package drawings.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
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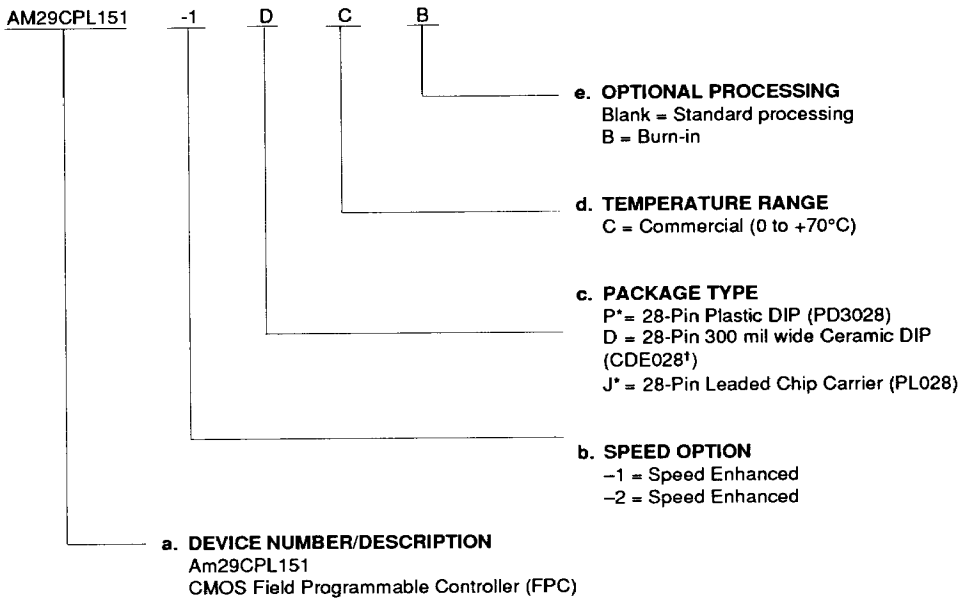
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29CPL151	PC, DC, DCB, JC
AM29CPL151-1	
AM29CPL151-2	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

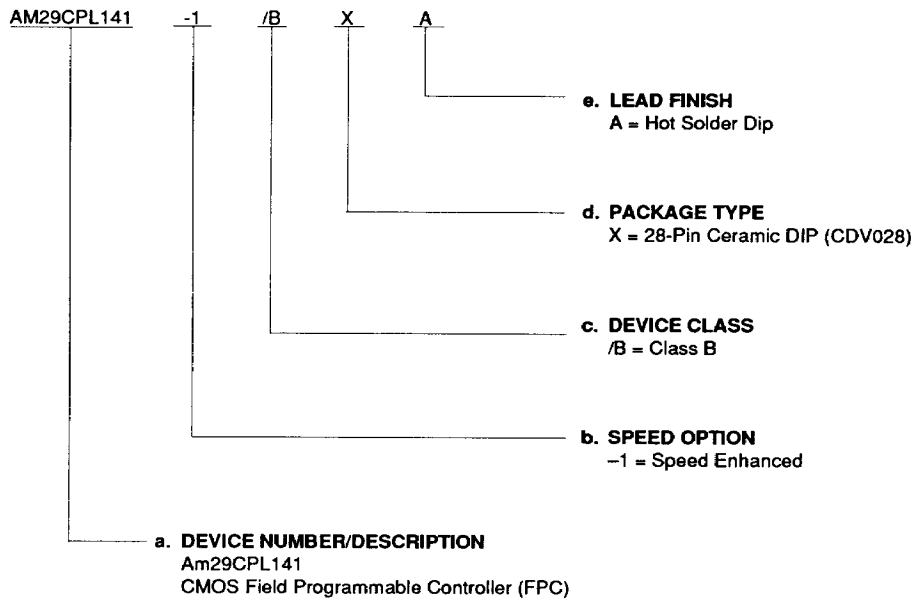
*Plastic DIP and PLCC are One-Time Programmable (OTP), non-windowed packages.
†Preliminary; package in development

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM29CPL141	/BXA
AM29CPL141-1	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

Group A Tests

Group A tests consists of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

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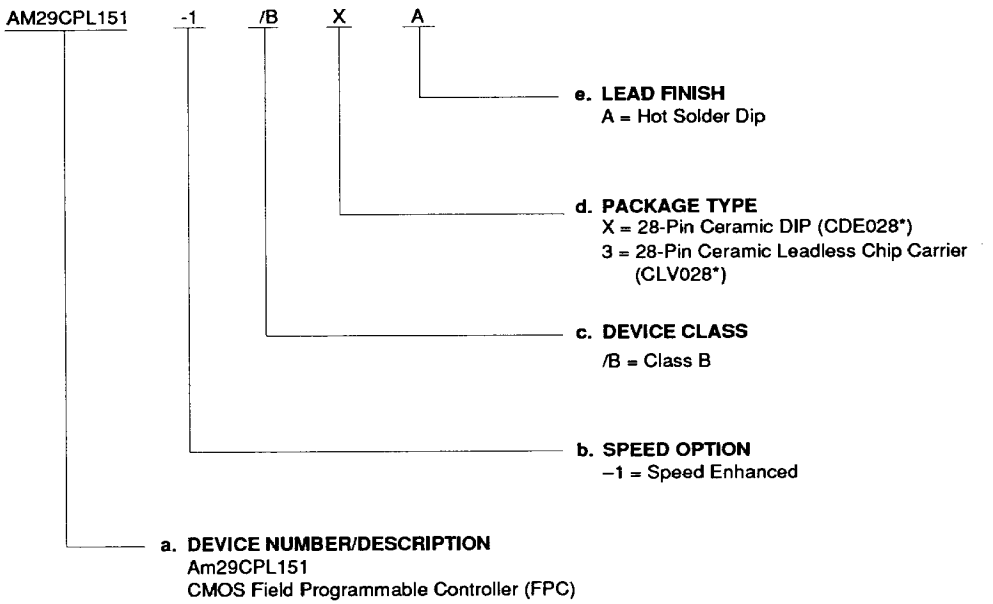
a. Device Number
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM29CPL151	/BXA, /B3A
AM29CPL151–1	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

Group A Tests

Group A tests consists of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

*Preliminary; package in development

PIN DESCRIPTION

CC[SDI] Optionally Registered Condition Code-TEST (Input)

When the TEST (P[24:22]) field of the executing instruction is set to 6 (binary 110), CC is selected to be the conditional input. In SSR diagnostic configuration, CC is also the Serial Data Input (SDI). An EPROM bit associated with this input may be programmed to make this input a registered input. The default state of this input is unregistered.

CLK Clock (Input)

The rising edge of the clock latches the program counter, count register (CREG), subroutine register (SREG), pipeline register, and EQ flag. The rising edge of the clock also latches the test input registers, CC register, and the $\overline{\text{RESET}}$ register if their respective configuration bits are set to enable internal synchronizing registers.

P[15:8] (Outputs)

The upper eight general-purpose control outputs are enabled by the OE signal from the pipeline register. When OE is HIGH, P[15:8] are enabled, and when LOW, P[15:8] are three-stated.

P[7:6], P[5:0]/A[5:0] [DCLK, MODE] (Outputs)

The lower eight general-purpose control outputs are permanently enabled. In the SSR diagnostic configuration, P[7] becomes the diagnostic clock input DCLK and P[6] becomes the diagnostic control input MODE. In expand mode (when the EXP bit is programmed) bits P[5:0] become the Program Memory address outputs A[5:0].

$\overline{\text{RESET}}$ Optionally Registered $\overline{\text{Reset}}$ (Input; Active LOW)

When the reset input is LOW, the output of the PC MUX is forced to the uppermost program address (63). On the next rising edge of the clock, this address (63) is loaded into the program counter; the instruction at location 63 is loaded into the pipeline register, and the EQ flag is cleared. A programmable configuration bit allows the option of making this a registered input. If $\overline{\text{RESET}}$ is internally registered, the first rising edge of the clock latches it. On the next rising edge of the clock, the EQ flip-flop is cleared and the contents of memory location 63 are loaded into the pipeline register. The default state of this input is unregistered.

T[5:0] Optionally Registered Test (Inputs)

In conditional instructions, the TEST inputs can be used as individual condition codes selected by the TEST field in the pipeline register. The T[5:0] inputs can also be used as a branch address when performing a program branch or as a count value to be loaded into the CREG. Each of these inputs has an EPROM bit associated with it. This bit may be programmed such that the corresponding input becomes a registered input. The default state of these inputs is unregistered.

$\overline{\text{ZERO}}$ [SDO] Zero (Output; Active LOW)

A LOW state on the $\overline{\text{ZERO}}$ output indicates that the CREG value is zero. In the SSR diagnostic configuration, $\overline{\text{ZERO}}$ becomes the Serial Data Output (SDO). This change is only on the output pin; internally, the zero-detect function is unchanged.

FUNCTIONAL DESCRIPTION

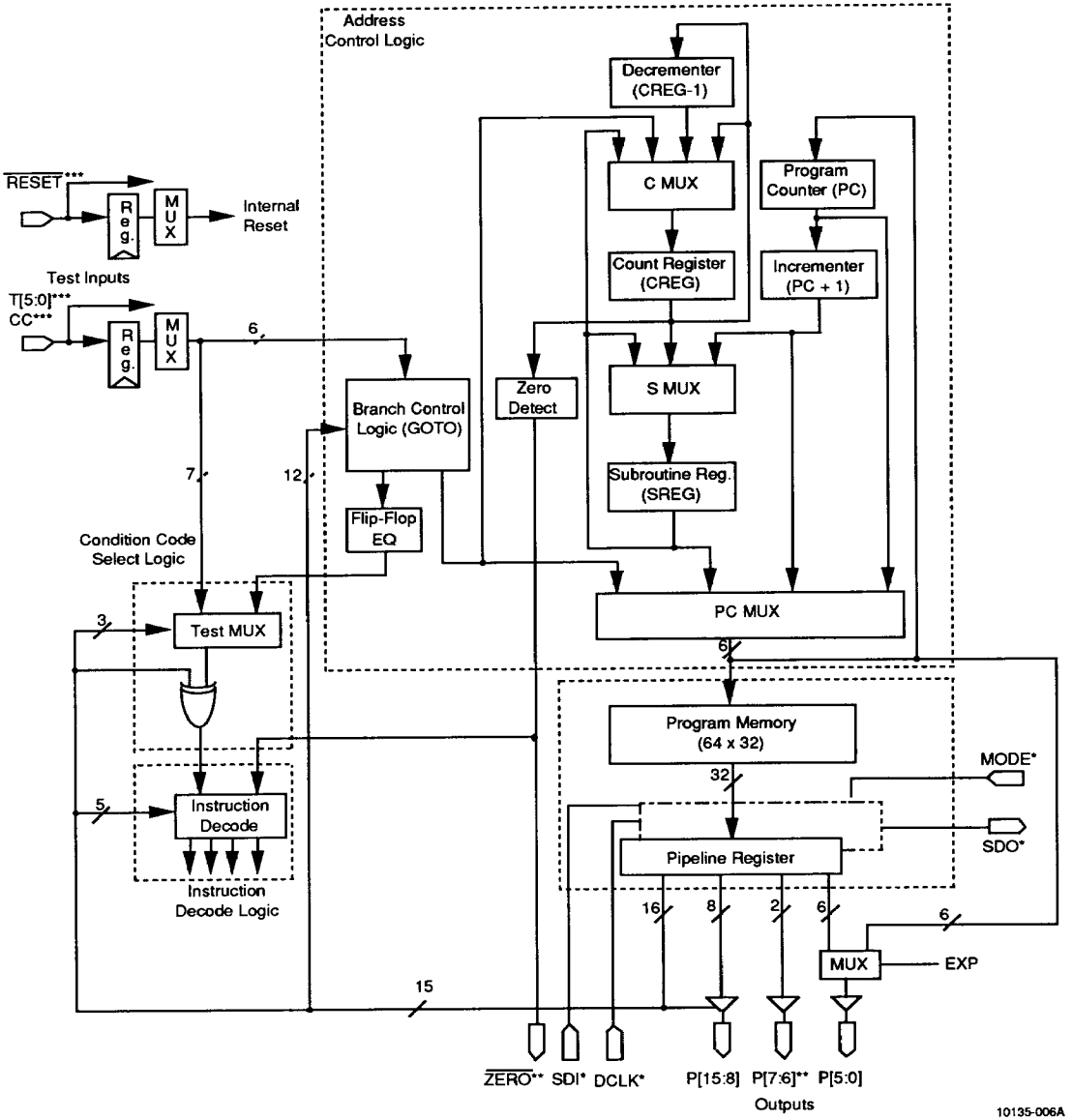
Figure 1, the detailed block diagram of the Am29CPL141 PIC, shows logic blocks and interconnecting buses that permit parallel performance of different operations in a single instruction. The FPC consists of four main logic blocks: the program memory, address control logic, condition code selection logic, and instruction decode. A fifth optional block is the Serial Shadow Register (SSR).

The program memory contains the user-defined instruction flow and output sequence. The address control logic addresses the program memory. This control logic supports high-level instruction functions including conditional branches, subroutine calls and returns, loops, and multiway branches. The condition code selection logic selects the condition code input to be tested when a conditional instruction is executed. The polarity of the selected condition code input is controlled by the POL bit in the microword. The instruction decode generates the control signals necessary to perform the instruction specified by the instruction part (P[31:16]) of the microword. The SSR enables in-system testing to isolate problems down to the IC level.

Program Memory

The FPC program memory is a 64-word by 32-bit EPROM with a 32-bit pipeline register at its output. The upper 16 bits (P[31:16]) of the pipeline register are internal to the PIC and form the instruction to control address sequencing. The format for instructions is: a one-bit synchronous Output Enable OE, a five-bit OP-CODE, a one-bit test polarity select POL, a three-bit TEST condition select field, and a six-bit immediate DATA field. The DATA field is used to provide branch addresses, test input masks, and counter values.

The lower 16 bits (P[15:0]) of the pipeline register are brought out as user-defined, general-purpose control outputs. The upper eight control outputs (P[15:8]) are three-stated when OE is programmed as a LOW. The lower eight control bits (P[7:0]) are always enabled. Outputs P[5:0] will contain the next instruction address when the optional EXP EPROM cell is programmed.



* These pins available only in SSR mode.
** These pins available only in normal mode.
*** Each of the T[5:0], $\overline{\text{RESET}}$, and CC inputs can be individually registered or left unregistered as a programmable option.

Figure 1. Am29CPL141 Detailed Block Diagram

Address Control Logic

The address control logic consists of five smaller logic blocks. These are:

PC MUX - Program counter multiplexer
P CNTR - Program counter (PC) and incrementer (PC + 1)
SUBREG - Subroutine register (SREG) with subroutine mux (S MUX)
CNTR - Count register (CREG) with counter mux (C MUX), decrementer (CREG-1), and zero detect
GOTO - Specialized branch control logic

The PC MUX is a six-bit, four-to-one multiplexer. It selects either the PC, PC + 1, SREG, or GOTO output as the next microaddress input to the Program Memory and to the PC. The PC thus always contains the address of the instruction in the pipeline register. During a Reset, the PC MUX output is forced to all ones, selecting location 63 from Program Memory.

The P CNTR block consists of a six-bit register (PC) driving a six-bit combinatorial incrementer (PC + 1). Either the present or the incremented values of PC can address the Program Memory. The incremented value of PC can be saved as a subroutine return address. The present PC value can address the Program Memory when waiting for a condition to become valid. PC + 1 addresses the Program Memory for sequential program flow, for unconditional instructions, and as a default for conditional instructions.

The SUBREG block consists of a six-bit, three-to-one multiplexer (S MUX) driving a six-bit register (SREG). The three possible SREG inputs are PC + 1, CREG, and SREG. SREG normally operates as a one-deep stack to save subroutine return addresses. PC + 1 is the input source when performing subroutine calls, and PC MUX is the output destination when performing return from subroutine.

The CNTR block consists of a six-bit, four-to-one multiplexer (C MUX), driving a six-bit register (CREG); a six-bit combinatorial decrementer (CREG-1); and a zero-detection circuit. The CNTR logic block is typically used for timing functions and iterative loop counting.

The SUBREG and CNTR can be considered as one logic block because of their unique interaction. Both have the other as an additional input source and output destination. The CREG can therefore be an additional stack location when not used for counting, and the SREG can be a nested-count location when not used as a stack location. Thus the SREG and CREG can operate in three different modes:

1. As a separate one-deep stack and counter
2. As a two-deep stack
3. As a two-deep nested counter

The GOTO logic block serves three functions:

1. It provides a six-bit count value from the DATA field in the pipeline register (P[21:16]) or from the TEST inputs T[5:0] masked by the DATA field P[21:16]. This is represented by T*M.

2. It provides a branch address from the DATA field in the pipeline register P[21:16] or from the TEST inputs T[5:0] masked by the DATA field P[21:16]. This is represented by T*M.

3. It compares T[5:0] masked by the MASK field P[21:16], called T*M, to the CONSTANT field from the pipeline register P[27:22]. If a match occurs, the EQ flip-flop is set. EQ remains unchanged if there is no match. Constant field bits that correspond to masked test bits must be zero.

The EQ flag can be tested by the condition code selection logic. Multiple tests of any group of T inputs in a manner analogous to sum-of-products can be performed since a no-match comparison does not reset the EQ flag. Any conditional branch on EQ will reset the EQ flag. Conditional returns on EQ will not change the EQ flag. $\overline{\text{RESET}}$ input LOW will reset the EQ flag.

NOTE: A zero in the MASK field blocks the corresponding bit in the TEST field; a one activates the corresponding bit.

The constant field bits that correspond to masked test field bits must be zero. A zero is substituted for masked test field bits. The "POL" bit is a "don't care" when using test inputs to load registers.

Note that when the inputs are internally registered (programmable option) they must meet the register setup time on the cycle preceding the one in which they are to be used.

Condition Code Selection Logic

The condition code selection logic consists of an eight-to-one multiplexer. The eight test condition inputs are the device inputs CC, T[5:0], and the EQ flag. The TEST field P[24:22] selects one of the eight conditions to test.

The polarity bit POL in the instruction allows the user to test for either a pass or fail condition. Refer to table 2 for details.

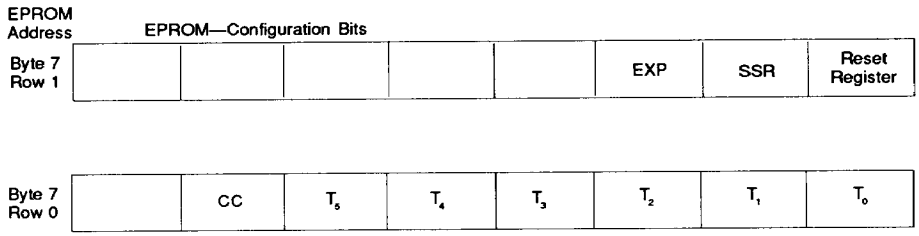
Note that when the inputs are internally registered (programmable option) they must meet the register setup time on the cycle preceding the one in which they are to be used.

Instruction Decode

The instruction decoder is a PLA that generates the control for 29 different instructions. The decoder inputs include the OPCODE field P[30:26], the zero detection output from the CNTR, and the selected test condition code from the condition code selection logic.

Operational Modes

The Am29CPL141 operates as a six-bit microcontroller in normal mode, and there are several configuration bits that can be programmed to modify this normal operation (see diagram below). The EXP bit allows the six program address lines from the PC MUX to be output on the lower six bits of the output pins (P[5:0]) so that a user can expand the width of the control lines by using external registered memories. The SSR bit allows on-chip diagnostic capabilities for in-system testing. The remaining bits serve to individually select whether the input pins will be unsynchronized or not. The default setting of these bits (unprogrrammed,1) will cause each pin to be unsynchronized, and so programming a given bit (to 0) will cause that corresponding input to become internally synchronized.



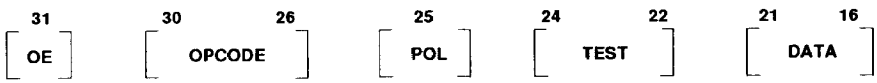
Am29CPL141 SSR Diagnostics Option

As a programmable option, the Am29CPL141 FPC may be configured to contain Serial Shadow Register (SSR) diagnostics capability. SSR diagnostics is a simple, straightforward method of in-system testing to isolate problems down to the IC level.

The SSR diagnostics configuration activates a 32-bit-wide D-type register called a "shadow" register, on the pipeline register inputs. The shadow register can be serially loaded from the SDI pin, parallel loaded from the pipeline register, or held. The pipeline register can be loaded from the Program Memory in normal mode or from the shadow register during diagnostics. A redefinition of four device pins is required to control the different diagnostics functions. CC also functions as the Serial Data Input (SDI), $\overline{ZERO}$ becomes the Serial Data Output (SDO), P[7] becomes the diagnostic clock (DCLK), and P[6] becomes the diagnostic mode control (MODE). The various diagnostic and normal modes are shown in table 1.

Serially loading a test instruction into the shadow register and parallel loading the shadow register contents into the pipeline register forces execution of the test instruction. The test result can then be clocked into the pipeline register as in normal operation mode, parallel loaded into the shadow register, and serially shifted out for system diagnostics.

Am29CPL141 General Instruction Format



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WHERE:

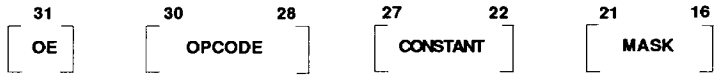
OE = Synchronous Output Enable for P[15:8]
OPCODE = A five-bit opcode field for selecting one of the 28 single-data-field instructions.
POL = A one-bit test condition polarity select (refer to table 2)
TEST = A three-bit test condition select

TEST[24:22]	UNDER TEST
000	T[0]
001	T[1]
010	T[2]
011	T[3]
100	T[4]
101	T[5]
110	CC
111	EQ

DATA = A six-bit conditional branch address, test input mask, or counter value field designated as PL in instruction mnemonics.

The special two-data-field comparison instruction format is shown below:

Am29CPL141 Comparison Instruction Format



WHERE:

OE = Synchronous Output Enable for P[15:8]
OPCODE = Compare instruction (binary 100)
CONSTANT = A six-bit constant for equal to comparison with T*M
MASK = A six-bit mask field for masking the incoming T[5:0] inputs

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Table 1

Inputs				Outputs			Operation
SDI	MODE	DCLK	CLK	SDO	Shadow Register	Pipeline Register	
D	L	↑	H,L,↓	S_0	$S_{i-1} \leftarrow S_i$ $S_{31} \leftarrow D$	Hold	Serial Right-Shift Register
CC	L	H,L,↓	↑	S_0	Hold	$P_i \leftarrow EPROM_i$	Normal Load Pipeline Register from EPROM
L	H	↑	H,L,↓	L	$S_i \leftarrow P_i$	Hold	Load Shadow Register* from Pipeline Register
X	H	H,L,↓	↑	SDI	Hold	$P_i \leftarrow S_i$	Load Pipeline Register from Shadow Register
H	H	↑	H,L,↓	H	Hold	Hold	Hold Shadow Register

*S7, S6 are undefined. S[15:8] load from the source driving pins P[15:8]. If P[31] in the microword is a ONE, S[15:8] are loaded from the pipeline register. If P[31] in the microword is a ZERO, S[15:8] are loaded from an external source.

Key:
H = HIGH
L = LOW
X = Don't Care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition

Table 2

Input Condition Being Tested	POL	Condition
0	0	Fail
0	1	Pass
1	0	Pass
1	1	Fail

Am29CPL141 INSTRUCTION SET DEFINITION

• = Other instruction

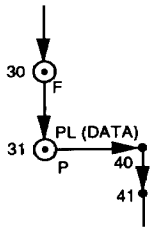
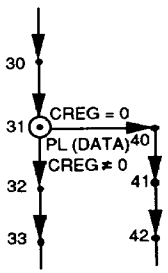
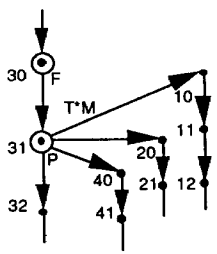
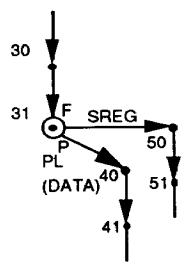
⊙ = Instruction being described

◯ = Register in part

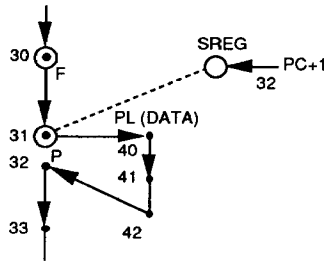
P = Test Pass

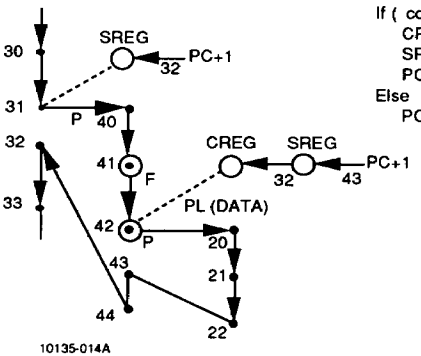
F = Test Fail

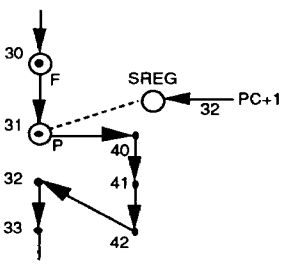
X,Y are arbitrary values in the CREG or SREG

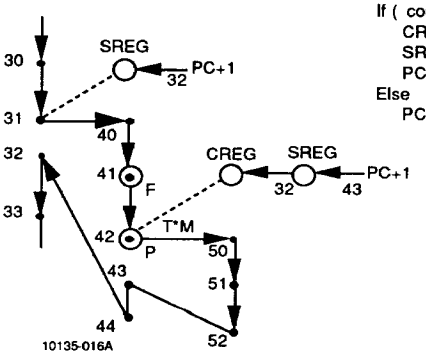
Opcode	Mnemonic	Description	Execution Example	Register Transfer Description
19	GOTOPL	**IF (cond) THEN GOTO PL (data)** Conditional branch to the address in the PL (DATA field). The EQ flag will be reset if the test field selects it and the condition passes.	 10135-009A	If (cond = true) Then PC = PL(data) Else PC = PC + 1
0B	GOTOPLZ	**IF (CREG=0) THEN GOTO PL (data)** Conditional branch to the address in the PL (DATA field) when CREG is equal to zero. This instruction does not depend on the pass/fail condition. The EQ flag will be reset if the test field selects it and the CREG is equal to zero.	 10135-010A	If (CREG = 0) Then PC = PL(data) Else PC = PC+1
0F	GOTOTM	**IF (cond) THEN GOTO TM (data)** Conditional branch to the address defined by the T*M (T[5:0] under bitwise mask from the DATA field). This instruction is intended for multiway branches. The EQ flag will be reset if the test field selects it and the condition passes.	 10135-011A	If (cond = true) Then PC = T*M Else PC = PC + 1
18	FORK	**IF (cond) THEN GOTO PL (data) ELSE GOTO (SREG)** Conditional branch to the address in the PL (DATA field) or the SREG. A branch to PL is taken if the condition is true and a branch to SREG if false. The EQ flag will be reset if the test field selects it and the condition passes.	 10135-012A	If (cond = true) Then PC = PL (data) Else PC = SREG

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

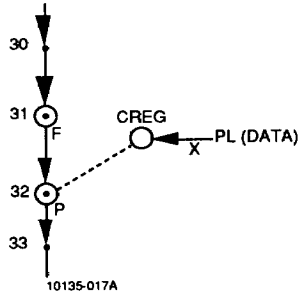
1C	CALPL	**IF (cond) THEN CALL PL (data)** Conditional jump to subroutine at the address in the PL (DATA field). The PC + 1 is pushed into the SREG as the return address. The EQ flag will be reset if the test field selects it and the condition passes.	 10135-013A	If (cond = true) Then
				SREG= PC + 1
				PC = PL(data)
				Else
				PC = PC + 1

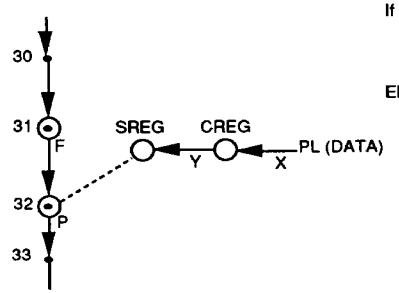
1D	CALPLN	**IF (cond) THEN CALL PL (data), NESTED** Conditional jump to subroutine at the address in the PL (DATA field) nested. The SREG and CREG are treated as a two-deep stack, the PC + 1 is pushed into the SREG as the return address, and the previous SREG value is transferred into the CREG as a nested return address. The EQ flag will be reset if the test field selects it and the condition passes.	 10135-014A	If (cond = true) Then
				CREG= SREG
				SREG= PC + 1
				PC = PL(data)
				Else
				PC = PC + 1

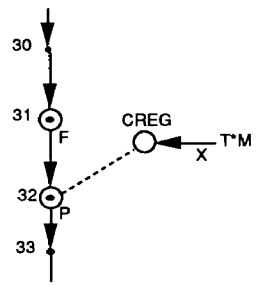
1E	CALTM	**IF (cond) THEN CALL TM (data)** Conditional jump to subroutine at the address specified by the T*M (T[5:0] under bitwise mask from the DATA field). The PC + 1 is pushed into the SREG as the return address. The EQ flag will be reset if the test field selects it and the condition passes.	 10135-015A	If (cond = true) Then
				SREG= PC + 1
				PC = T*M
				Else
				PC = PC + 1

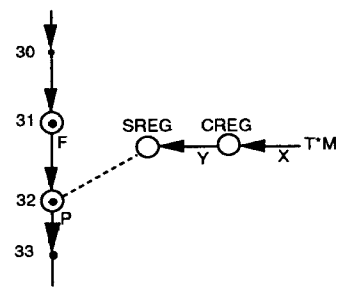
1F	CALTMN	**IF (cond) THEN CALL TM (data) NESTED** Conditional jump to subroutine at the address specified by the T*M (T[5:0] under bitwise mask from the DATA field) nested. The PC + 1 is pushed into the SREG as the return address and the previous SREG value is transferred into the CREG as a nested return address. The EQ flag will be reset if the test field selects it and the condition passes.	 10135-016A	If (cond = true) Then
				CREG= SREG
				SREG= PC + 1
				PC = T*M
				Else
				PC = PC + 1

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

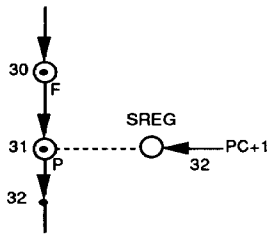
04	LDPL	**IF (cond) THEN LOAD PL (data)**
		Conditional load the CREG from the PL (DATA field).
			
			10135-017A
				If (cond = true) Then
				CREG= PL(data)
				PC = PC + 1
				Else
				PC = PC + 1

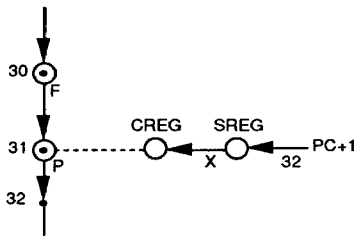
05	LDPLN	**IF (cond) THEN LOAD PL (data), NESTED**
		Conditional load the CREG from the PL (DATA field) nested. The CREG and SREG are treated as a two-deep nested count register, the previous CREG value is pushed into the SREG as a nested count, and the CREG is loaded from PL.
			
			10135-018A
				If (cond = true) Then
				SREG =CREG
				CREG =PL(data)
				PC = PC + 1
				Else
				PC = PC + 1

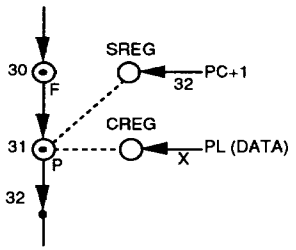
06	LDTM	**IF (cond) THEN LOAD TM (data)**
		Conditional load the CREG from the T*M (T[5:0] inputs under bitwise mask from the DATA field).
			
			10135-019A
				If (cond = true) Then
				CREG = T*M
				PC = PC + 1
				Else
				PC = PC + 1

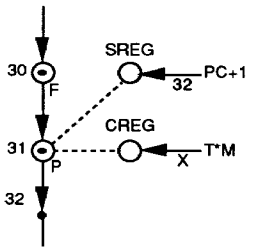
07	LDTMN	**IF (cond) THEN LOAD TM (data), NESTED** Conditional load the CREG from the T*M (T[5:0] inputs under bitwise mask from the DATA field) nested. The SREG and CREG are treated as a two-deep nested count register, the previous CREG value is transferred into the SREG, and the CREG is loaded from T*M.	 10135-020A	If (cond = true) Then SREG = CREG CREG = T*M PC = PC + 1

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

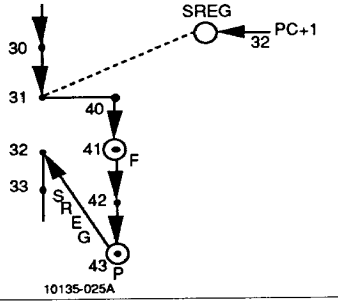
15	PSH	**IF (cond) THEN PUSH**
		Conditional push the PC + 1 into the SREG.
			
			10135-021A
				If (cond = true) Then
				SREG = PC + 1
				PC = PC + 1
				Else
				PC = PC + 1

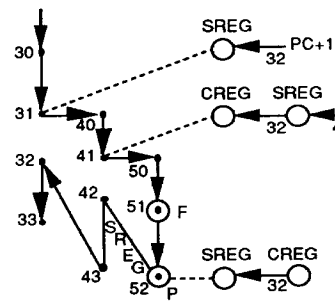
17	PSHN	**IF (cond) THEN PUSH, NESTED**
		Conditional push the PC + 1 into the SREG nested. This microinstruction treats the SREG and CREG as a two-deep stack, PC + 1 is pushed into SREG, and the previous value in SREG is transferred into the CREG.
			
			10135-022A
				If (cond = true) Then
				CREG= SREG
				SREG= PC + 1
				PC = PC + 1
				Else
				PC = PC + 1

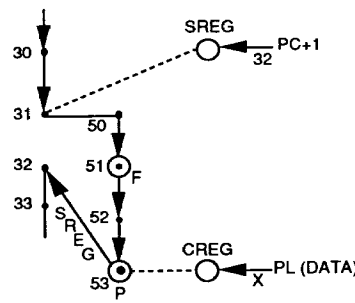
14	PSHPL	**IF (cond) THEN PUSH, LOAD PL (data)**
		Conditional push the PC + 1 into the SREG and load the CREG from the PL (DATA field).
			
			10135-023A
				If (cond = true) Then
				CREG= PL(data)
				SREG= PC + 1
				PC = PC + 1
				Else
				PC = PC + 1

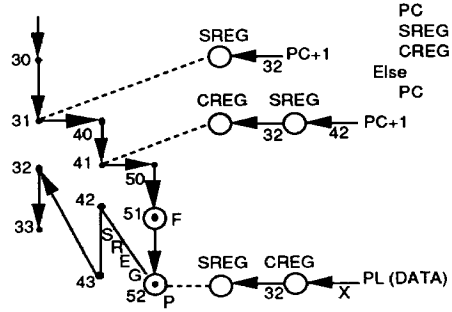
16	PSHTM	**IF (cond) THEN PUSH, LOAD TM (data)**
		Conditional push the PC + 1 into the SREG and load the CREG from the T*M (T[5:0] under bitwise mask from the DATA field).
			
			10135-024A
				If (cond = true) Then
				CREG= T*M
				SREG= PC + 1
				PC = PC + 1
				Else
				PC = PC + 1

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

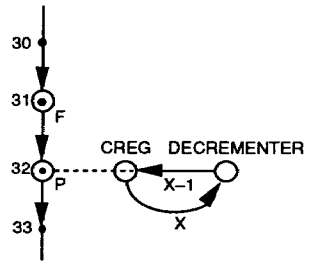
02	RET	**IF (cond) THEN RET**
		Conditional return from subroutine. The SREG provides the return from subroutine address.
			
			10135-025A
				If (cond = true) Then
				PC = SREG
				Else
				PC = PC + 1

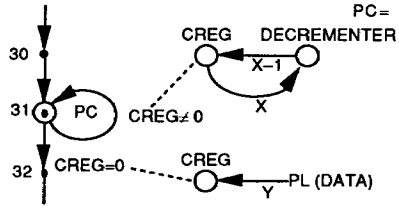
03	RETN	**IF (cond) THEN RET, NESTED**
		Conditional return from nested subroutine. This instruction treats the SREG and CREG as a two-deep stack providing the SREG value as a return address, and the CREG value as a nested return address that is transferred into the SREG.
			
			10135-026A
				If (cond = true) Then
				PC = SREG
				SREG = CREG
				Else
				PC = PC + 1

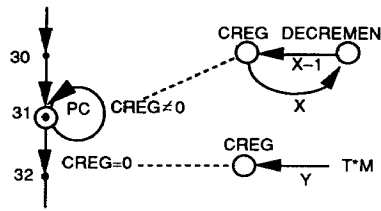
00	RETPL	**IF (cond) THEN RET, LOAD PL (data)**
		Conditional return from subroutine and load the CREG from the PL (DATA field). The SREG provides the return from subroutine address.
			
			10135-027A
				If (cond = true) Then
				CREG = PL(data)
				PC = SREG
				Else
				PC = PC + 1

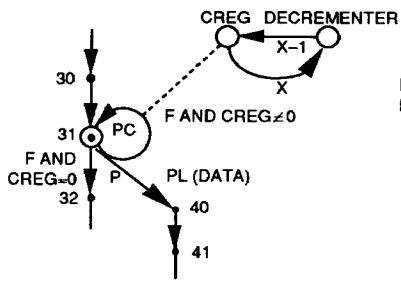
01	RETPLN	**IF (cond) THEN RET NESTED, LOAD PL (data)**
		Conditional return from nested subroutine and load the CREG from the PL (DATA field). This instruction treats the SREG and CREG as a two-deep stack providing the SREG value as a return address, and the CREG value as a nested return address that is transferred into the SREG.
			
			10135-028A
				If (cond = true) Then
				PC = SREG
				SREG = CREG
				CREG = PL(data)
				Else
				PC = PC + 1

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

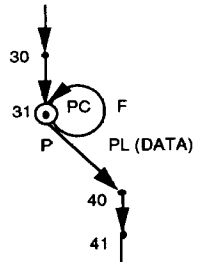
09	DEC	**IF (cond) THEN DEC**
		Conditional decrement of the CREG.
			
			10135-029A
				If (cond = true) Then
				CREG= CREG – 1
				PC = PC + 1
				Else
				PC = PC + 1

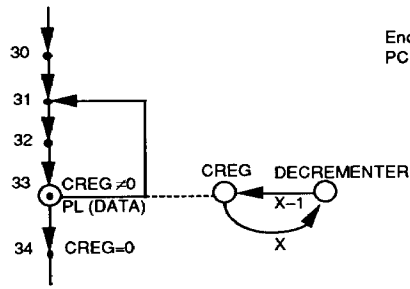
0C	DECPL	**WHILE (CREG < > 0) WAIT ELSE LOAD PL (data)**
		Conditional Hold until the counter is equal to zero, then load CREG from the PL (DATA field). This instruction is intended for timing waveform generation. If the CREG is not equal to zero, the same instruction is refetched while CREG is decremented. Timing is complete when the CREG is equal to zero, causing the next instruction to be fetched and the CREG to be reloaded from PL. This instruction does not depend on the pass/fail condition.
			
			10135-030A
				While (CREG < > 0)
				CREG= CREG – 1
				PC = PC
				End While
				CREG = PL(data)
				PC= PC + 1

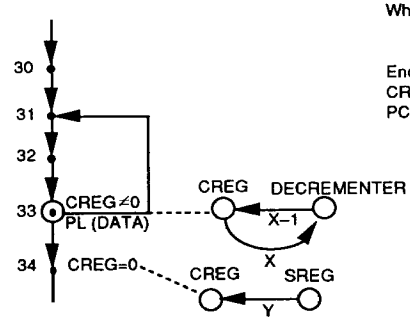
0E	DECTM	**WHILE (CREG < > 0) WAIT ELSE LOAD TM (data)**
		Conditional Hold until the counter is equal to zero, then load CREG from the T*M (T[5:0] under bitwise mask from the DATA field). This instruction is intended for timing waveform generation. If the CREG is not equal to zero, the same instruction is refetched while the CREG is decremented. Timing is complete when the CREG is equal to zero, causing the next instruction to be fetched and the CREG to be reloaded from T*M. This instruction does not depend on the pass/fail condition.
			
			10135-031A
				While (CREG < > 0)
				CREG= CREG – 1
				PC = PC
				End While
				CREG = T*M
				PC= PC + 1

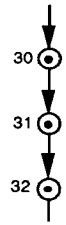
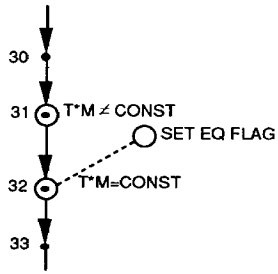
1B	DECGOPL	**If (cond) THEN GOTO PL (data) ELSE WHILE (CREG < > 0) WAIT**
		Conditional Hold/Count. The current instruction will be refetched and the CREG decremented until the condition under test becomes true or the counter is equal to zero. If the condition becomes true, a branch to the address in the PL (DATA field) is executed. If the counter becomes zero without the condition becoming true, a CONTINUE is executed. The EQ flag will be reset if the test field selects it and the condition passes.
			
			10135-032A
				While (cond = false)
				If (CREG < > 0)
				CREG = CREG – 1
				PC = PC
				Else
				PC = PC + 1
				End While
				PC = PL(data)

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description

1A	WAIT	**IF (cond) THEN GOTO PL (data) ELSE WAIT**
		Conditional Hold. The current instruction will be refetched and executed until the condition under test becomes true. When true, a branch to the address in the PL (DATA field) is executed. The EQ flag will be reset if the test field selects it and the condition passes.
			
			10135-033A
				If (cond = true) Then
				PC = PL(data)
				Else
				PC = PC

08	LPPL	**WHILE (CREG < > 0) LOOP TO PL (data)**
		Conditional loop to the address in the PL (DATA field). This instruction is intended to be placed at the bottom of an iterative loop. If the CREG is not equal to zero, it is decremented (signifying completion of an iteration), and a branch to the PL (DATA field) (top of the loop) is executed. If the CREG is equal to zero, looping is complete and the next sequential instruction is executed. This instruction does not depend on the pass/fail condition. The EQ flag will be reset if the test field selects it and CREG is not equal to zero.
			
			10135-034A
				While (CREG < > 0)
				CREG= CREG – 1
				PC = PL (data)
				End While
				PC = PC + 1

0A	LPPLN	**WHILE (CREG < > 0) LOOP TO PL (data) ELSE NEST**
		Conditional loop to the address in the PL (DATA field) nested. The SREG and CREG are treated as a two-deep nested count register, and the instruction is intended to be placed at the bottom of an "inner-nested" iterative loop. If the CREG is not equal to zero, the CREG is decremented (signifying completion of an interation), and a branch to the PL (DATA field) (top of the inner loop) is executed. If the CREG is equal to zero, the inner loop is complete, and the count value for the outer loop is transferred from the SREG into the CREG. This instruction does not depend on the pass/fail condition. The EQ flag will be reset if the test field selects it and the CREG is not equal to zero.
			
			10135-035A
				While (CREG < > 0)
				CREG= CREG – 1
				PC = PL(data)
				End While
				CREG = SREG
				PC = PC + 1

Opcode	Mnemonic	Description	Execution Example	Register Transfer Description
0D	CONT	**CONTINUE** The next sequential instruction is fetched unconditionally.	 10135-036A	PC = PC + 1
10–13 (100XX binary)	CMP	**CMP TM (mask) TO PL (constant)** This instruction performs bitwise exclusive-or of T*M (T[5 : 0] under bitwise mask from the MASK field) with CONSTANT (P[27 : 22]). If T*M equals CONSTANT, the EQ flag is set to one, which may be branched on in a following instruction. If not equal, the EQ flag is unaffected. This allows sequences of compares, in a manner analogous to sum-of-products, to be performed which can be followed by a single conditional branch if one or more of the comparisons are true. Note: The EQ flag is set to zero on reset or when EQ is selected as the test condition in a branch. Conditional returns on EQ leave the flag unchanged. Constant field bits that correspond to masked test field bits must be zero. This instruction does not depend on the pass/fail condition.	 10135-037A	Compare T*M and CONSTANT EQ = ((T [5:0] .AND. MASK). XNOR. CONSTANT) .OR. EQ

INSTRUCTIONS BASED ON TEST CONDITIONS

Opcode	Mnemonic	Assembler Statement	Condition Pass				Condition Fail				Notes
			PC MUX	STACK	CREG	EQ FLAG	PC MUX	STACK	EQ CREG	FLAG	
00	RETPL	IF (cond) THEN RET, LOAD PL (data)	SREG	Hold	Load PL	NC	PC + 1	Hold	Hold	NC	
01	RETPLN	IF (cond) THEN RET NESTED, LOAD PL (data)	SREG	Load CREG	Load PL	NC	PC + 1	Hold	Hold	NC	
02	RET	IF (cond) THEN RET	SREG	Hold	Hold	NC	PC + 1	Hold	Hold	NC	
03	RETN	IF (cond) THEN RET, NESTED	SREG	Load CREG	Hold	NC	PC + 1	Hold	Hold	NC	
04	LDPL	IF (cond) THEN LOAD PL (data)	PC + 1	Hold	Load PL	NC	PC + 1	Hold	Hold	NC	
05	LDPLN	IF (cond) THEN LOAD PL (data), NESTED	PC + 1	Load CREG	Load PL	NC	PC + 1	Hold	Hold	NC	
06	LDTM	IF (cond) THEN LOAD TM (data)	PC + 1	Hold	Load TM	NC	PC + 1	Hold	Hold	NC	
07	LDTMN	IF (cond) THEN LOAD TM (data), NESTED	PC + 1	Load CREG	Load TM	NC	PC + 1	Hold	Hold	NC	
09	DEC	IF (cond) THEN DEC	PC + 1	Hold	DEC	NC	PC + 1	Hold	Hold	NC	
0F	GOTOTM	IF (cond) THEN GOTO TM (data)	TM	Hold	Hold	Reset	PC + 1	Hold	Hold	NC	1
14	PSHPL	IF (cond) THEN PUSH, LOAD PL (data)	PC + 1	PC + 1	Load PL	NC	PC + 1	Hold	Hold	NC	
15	PSH	IF (cond) THEN PUSH	PC + 1	PC + 1	Hold	NC	PC + 1	Hold	Hold	NC	
16	PSHTM	IF (cond) THEN PUSH, LOAD TM (data)	PC + 1	PC + 1	Load TM	NC	PC + 1	Hold	Hold	NC	
17	PSHN	IF (cond) THEN PUSH, NESTED	PC + 1	PC + 1	Load SREG	NC	PC + 1	Hold	Hold	NC	
18	FORK	IF (cond) THEN GOTO PL (data) ELSE GOTO (SREG)	PL	Hold	Hold	Reset	SREG	Hold	Hold	NC	1
19	GOTOPL	IF (cond) THEN GOTO PL (data)	PL	Hold	Hold	Reset	PC + 1	Hold	Hold	NC	1
1A	WAIT	IF (cond) THEN GOTO PL (data) ELSE WAIT	PL	Hold	Hold	Reset	PC	Hold	Hold	NC	1
1C	CALPL	IF (cond) THEN CALL PL (data)	PL	PC + 1	Hold	Reset	PC + 1	Hold	Hold	NC	1
1D	CALPLN	IF (cond) THEN CALL PL (data), NESTED	PL	PC + 1	Load SREG	Reset	PC + 1	Hold	Hold	NC	1
1E	CALTM	IF (cond) THEN CALL TM (data)	TM	PC + 1	Hold	Reset	PC + 1	Hold	Hold	NC	1
1F	CALTMN	IF (cond) THEN CALL TM (data), NESTED	TM	PC + 1	Load SREG	Reset	PC + 1	Hold	Hold	NC	1

INSTRUCTIONS DEPENDENT ON CREG

Opcode	Mnemonic	Assembler Statement	CREG = 0				CREG ≠ 0				Notes
			PC MUX	STACK	CREG	EQ FLAG	PC MUX	STACK	CREG	EQ FLAG	
08	LPPL	WHILE (CREG < > 0) LOOP TO PL (data)	PC + 1	Hold	Hold	NC	PL	Hold	DEC	Reset	2
0A	LPPLN	WHILE (CREG < > 0) LOOP TO PL (data), ELSE NEST	PC + 1	Hold	Load SREG	NC	PL	Hold	DEC	Reset	2
0B	GOTOPLZ	IF (CREG = 0) THEN GOTO PL (data)	PL	Hold	Hold	Reset	PC + 1	Hold	Hold	NC	3
0C	DECPL	WHILE (CREG < > 0) WAIT ELSE LOAD PL (data)	PC + 1	Hold	Load PL	NC	PC	Hold	DEC	NC	
0E	DECTM	WHILE (CREG < > 0) WAIT ELSE LOAD TM (data)	PC + 1	Hold	Load TM	NC	PC	Hold	DEC	NC	

INSTRUCTIONS DEPENDENT ON TEST CONDITION AND CREG VALUE

Opcode	Mnemonic	Assembler Statement	CREG Content	Condition Pass				Condition Fail				Notes
				PC MUX	STACK	CREG	EQ FLAG	PC MUX	STACK	CREG	EQ FLAG	
1B	DECGOPL	IF (cond) THEN GOTO PL (data) ELSE WHILE (CREG < > 0) WAIT	≠ 0	PL	Hold	Hold	Reset	PC	Hold	DEC	NC	1
			= 0	PL	Hold	Hold	Reset	PC + 1	Hold	Hold	NC	

UNCONDITIONAL INSTRUCTIONS

Opcode	Mnemonic	Assembler Statement	PC MUX	STACK	CREG	EQ FLAG	Notes
OD	CONT	CONTINUE	PC + 1	Hold	Hold	NC	
10–13 (Binary 100XX)	CMP	CMP TM (mask) TO PL (constant)	PC + 1	Hold	Hold	Set	4

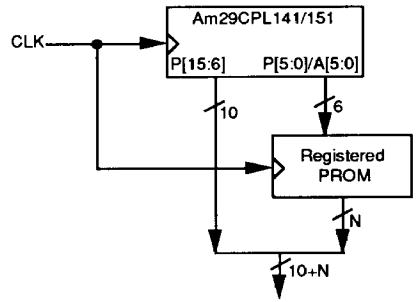
Key: PC = Program Counter
SREG = Stack Register
CREG = Counter Register
PL = Pipeline (data) Field
TM = Test Inputs Masked by MASK Field
DEC = Decrement
NC = No Change

Notes: 1. If COND = EQ and condition PASSES, reset EQ flag.
2. If COND = EQ and CREG ≠ 0, reset EQ flag.
3. If COND = EQ and CREG = 0, reset EQ flag.
4. Set EQ flag if CONST field = T*M.

APPLICATIONS

Using the Am29CPL141 to Control External PROM

By programming the EXP bit, PC MUX is output over pins P[5:0]/A[5:0]. This feature can be used to extend the width of the output control word when external registered memories are used. In the diagram below, the Am29CPL141 controls external registered PROMs to provide an output control word (10 + N) bits wide (where N is the bit width of the PROMs).



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PROGRAMMING

The Am29CPL141 FPC controller is programmed using a simple algorithm. The internal EPROM is organized as a 64-word by 32-bit array. The array is divided up into four bytes for programming. Data is written byte-wide through pins P[15:8] using a simple sequence of voltages on two pins (CLK and $\overline{\text{RESET}}$). The Am29CPL141 uses pins P[7:5] for byte addressing; the EPROM array resides in the four lower bytes (0 through 3), while the most significant byte (7) is reserved for user-configuration registers. Bytes, 4, 5, and 6 are not used on the Am29CPL141. Pins T[5:0] are used to address the word with T[5] being the MSB.

The Am29CPL141 programming cycle is shown in the Programming Waveform diagram. Each programming cycle consists of a program mode followed by a verify mode. To begin programming, the CLK pin is raised from a TTL level to VPP. The Am29CPL141 enters program mode and disables output pins P[15:5] and accepts these pins as data I/O and address inputs. Now that the chip is in program mode, the $\overline{\text{RESET}}$ pin controls the program and verify modes. With a TTL-level HIGH on $\overline{\text{RESET}}$, the data I/O is high impedance, and the program data (P[15:8]) and address (P[7:5]) can be set up. The data is written into memory by applying VPP to $\overline{\text{RESET}}$ for time $t_{w(PGMI)}$ as described in the Programming Parameter table. $\overline{\text{RESET}}$ is then switched back to a TTL-level HIGH; the program data is removed. The verify (read) cycle begins when $\overline{\text{RESET}}$ is switched to a TTL LOW level and the data resident at the addressed byte is output on the data I/O (P[15:8]). Raising $\overline{\text{RESET}}$ back to a TTL-level HIGH completes one programming cycle.

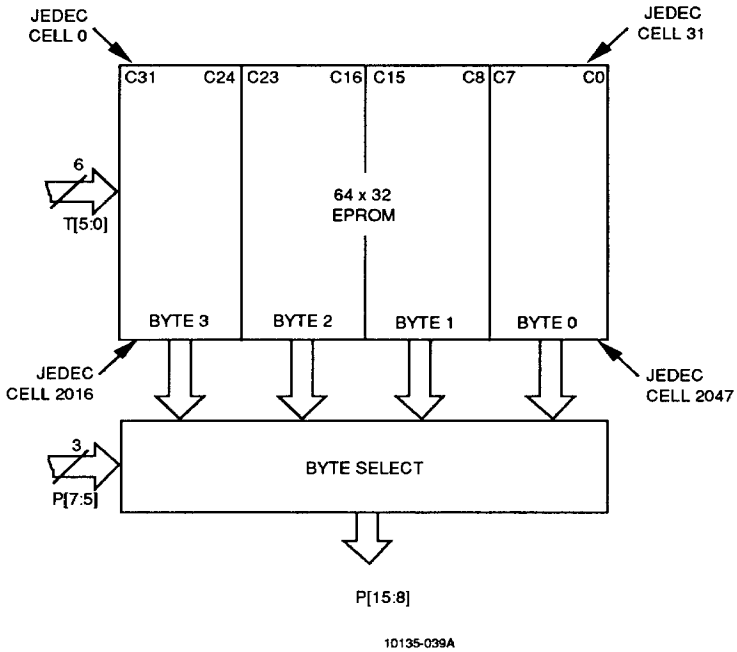
To ensure reliable programming, if the data does not verify, the programming cycle could be repeated up to a total of 25 times. After a valid verification, a final over-programming should be executed using a VCC = 5.0 V and an extended pulse width $t_{w(PGMI)}$ equal to twice the sum of initial programming pulse width. At the conclusion of programming the Am29CPL141, the EPROM memory should be reverified for correct data at all addresses using two supply voltages (V_{CC} = 5.5 V and V_{CC} = 4.5 V).

Erasure

In order to fully erase all memory locations, it is necessary to expose the memory array to an ultraviolet light source having a wavelength of 2537 angstroms. The minimum recommended dose (UV intensity × exposure time) is 15 Wsec/cm^2. For a UV lamp with a 12 mW/cm^2 power rating, the exposure time would be about 30 minutes. The device should be located one inch from the source in a direct line.

It should be noted that erasure will begin with exposure to light having wavelengths less than 4000 angstroms. To prevent exposure to sunlight or fluorescent lighting, an opaque label should be affixed over the window after programming.

OTP (One-Time Programmable) Am29CPL151 devices are available in plastic and are ideal for volume production. They can be inventoried unprogrammed and used with current software revisions; there is no window to be covered to prevent light from changing data.



JEDEC cell number definitions:

Cell no. = 32 × (Row Address) + 8 × (3 – Byte) + (7 – Bit); for Byte ≤ 3

Example computations:

Row 0, Byte 3, Bit 4 Cell no. = 32(0) + (3 –3) + (7 – 4) = 3
Row 63, Byte 0, Bit 0 Cell no. = 32(63) + 8(3 – 0) + (7 – 0) = 2047

The cell numbers for the configuration bits are as follows (Byte 7 only):

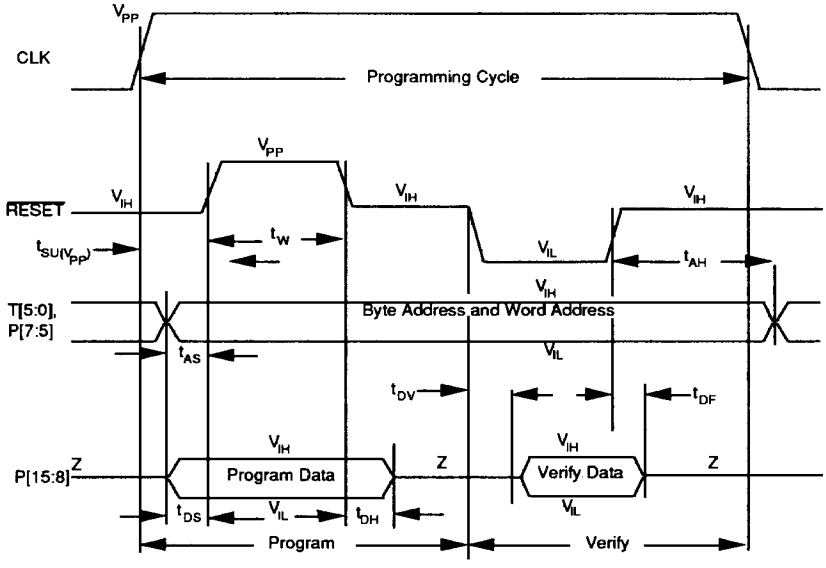
Sync. Registers for CC, T5 through T0 are cells 2048 through 2054
EXP is cell 2055
SSR is cell 2056
RESET is cell 2057

Figure 2. Programming

Byte	Byte Select			Bit Select							
	P[7]	P[6]	P[5]	P[15]	P[14]	P[13]	P[12]	P[11]	P[10]	P[9]	P[8]
0	L	L	L	C7	C6	C5	C4	C3	C2	C1	C0
1	L	L	H	C15	C14	C13	C12	C11	C10	C9	C8
2	L	H	L	C23	C22	C21	C20	C19	C18	C17	C16
3	L	H	H	C31	C30	C29	C28	C27	C26	C25	C24
4	H	L	L	-	-	-	-	-	-	-	-
5	H	L	H	-	-	-	-	-	-	-	-
6	H	H	L	-	-	-	-	-	-	-	-
7 (Row 0)	H	H	H	-	CC	T5	T4	T3	T2	T1	T0
7 (Row 1)	H	H	H	-	-	-	-	-	EXP	SSR	Reset Register

PROGRAMMING PARAMETERS (T_A + 25°C ± 5°C)

Parameter Symbol	Parameter Description		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	I_{CC} = 50 mA	5.75	6.0	6.25	V
V_{PP}	Programming Voltage	I_{PP} = 30 mA	13	13.5	14	V
V_{IH}	Input HIGH Level		2.4		5.5	V
V_{IL}	Input LOW Level		0		0.5	V
$t_{W(PGMI)}$	Program Pulse Duration (Initial)		0.95		1.05	ms
$t_{W(PGMI)}$	Program Pulse Duration (Final)		2.0		50	ms
t_{AS}	Address Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
$t_{SU(VPP)}$	VPP Setup Time		2			µs
t_{AH}	Address Hold Time		1			µs
t_{DH}	Data Hold Time		1			µs
t_{DV}	Data Valid from $\overline{RESET}$ LOW				100	vs
t_{DF}	Data Float from $\overline{RESET}$ HIGH		0		100	ns



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Programming Waveforms

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65 to +150°C
(Ambient) Temperature Under Bias ..... –55 to +125°C
Supply Voltage to Ground Potential
(Pin 28 to Pin 14) Continuous ..... –0.5 to +7.0 V
DC Voltage Applied to Outputs ..... –0.3 to +V_{CC} + 0.3 V
DC Input Voltage ..... –0.3 to +V_{CC} +0.3 V
DC Input Current ..... –10 to +10 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Military* (M) Devices
Ambient Temperature (T_A) ..... –55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Thermal Impedance Values (θ_{JA}), Typical
28-Pin Plastic DIP (PD3028) ..... 50°C/W
28-Pin Ceramic DIP (CDV028, CDE028) ..... 40°C/W
28-Pin Plastic Leaded Chip Carrier (PL028) ..... 55°C/W
28-Pin Ceramic Leadless Chip Carrier (CLV028) ... 55°C/W

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military Product 100% tested at T_A = +25°C, +125°C, and –55°C.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions				Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	COM'L	I_{OH} = -3.0 mA		2.4		V
			MIL	I_{OH} = -1.0 mA				
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IL} or V_{IH}	COM'L	I_{OL} = 16 mA			0.50	V
			MIL	I_{OL} = 12 mA				
V_{IH} (Note 1)	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs				2.0		V
V_{IL} (Note 1)	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs					0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4 V					–10	µA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.4 V					10	µA
I_{OZH}	Output Leakage Current (Note 2)	V_{CC} = Max., V_{IH} = 2.0 V			V_O = 2.4 V		10	µA
I_{OZL}					V_O = 0.5 V		–10	
I_{CC}	Power Supply Current (Note 3)	V_{CC} = Max., I_O = 0 µA	COM'L (T_A = 0 to +70°C)	CMOS	V_{IN} = V_{CC} or GND		105	mA
				TTL	V_{IN} = 0.5 V or 2.4 V		115	
			MIL (T_A = –55 to +125°C)	CMOS	V_{IN} = V_{CC} or GND		120	mA
				TTL	V_{IN} = 0.5 V or 2.4 V		130	
C_{PD}	Power Dissipation Capacitance (Note 4)	V_{CC} = Max. T_A = +25°C No Load				100 pF Typical		

Notes:
1. These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst-case of I_{OZX} or I_{IX} (where X = H or L).
3. Use CMOS I_{CC} when the device is driven by CMOS circuits and TTL I_{CC} when the device is driven by TTL circuits.
4. The dynamic current consumption is:
I_{CC} (Total) = I_{CC} (Static) + (C_{PD} + nC_L) V_{CC} (f/2), where f is the clock frequency, C_L = the output load capacitance, and n is the number of loads.

CAPACITANCE*

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C_I ($\overline{RESET}$)	Input Capacitance	f = 1 MHz T_A = –55°C to 125°C V_{CC} = 4.5 V to 5.5 V		25	pF
C_I (All others)	Input Capacitance			15	
C_O	Output Capacitance			15	

*Tested on a sample basis only.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range

No.	Parameter Symbol	Parameter Description	Test Cond.	29CPL141/ 29CPL151		29CPL141-1/ 29CPL151-1		29CPL151-2		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
1		CLK to P[15:0]			14		13		11	ns
2		CLK to A[5:0]			26		30		26	ns
3	t_{PD}	CLK to $\overline{ZERO}$			25		25		23	ns
4		DCLK to SDO			22		22		20	ns
5		Mode to SDO			20		20		17	ns
6		SDI to SDO			20		20		17	ns
7		T[2:0] to CLK, Registered Mode		8		8		8		ns
8		T[5:3] to CLK, Registered Mode		10		10		10		ns
9		T[5:0] to CLK, Async Mode (Note 1)		30		33		32		ns
10		CC to CLK, Registered Mode		8		8		8		ns
11		CC to CLK, Async Mode (Note 1)		40		33		32		ns
12	t_S	$\overline{RESET}$ to CLK, Registered Mode		12		12		12		ns
13		RESET to CLK, Async Mode (Note 1)		40		27		25		ns
14		Mode to CLK	See Test Output Load Cond.	15		12		11		ns
15		Mode to DCLK		15		12		11		ns
16		SDI to DCLK		15		12		11		ns
17		P[15:8] to CLK		15		12		11		ns
18		T[5:0] to CLK		0		0		0		ns
19		CC to CLK		0		0		0		ns
20	t_H (Note 2)	RESET to CLK		0		0		0		ns
21		Mode to CLK		6		6		6		ns
22		Mode to DCLK		0		0		0		ns
23		SDI to DCLK		0		0		0		ns
24		P[15:8] to DCLK		0		0		0		ns
25		CLK to P[15:8] Enable			40		35		33	ns
26		CLK to P[15:8] Disable			30		25		25	ns
27	t_w	CLK Pulse Width (HIGH and LOW)		12		12		11		ns
28		DCLK Pulse Width (HIGH and LOW)		12		13		12		ns
29	t_p	CLK Period (Note 1)		40		33		30		ns
30		DCLK Period		25		23		22		ns

Notes: 1. These parameters are measured indirectly on unprogrammed devices. They are determined as follows:

a. Measure delay from input (CC, T[5:0], $\overline{RESET}$, or CLK) to EPROM address out in test mode. This will measure the delay through the sequence logic.

b. Measure setup time from T[5:0] input through EPROM test columns to pipeline register in verify test column mode. This will measure the delay through the EPROM and register setup.

c. Measure delay from T[5:0] input to EPROM address out in verify test column mode. This will measure the delay through the logic and P[15:0] outputs.

To calculate the desired parameter measurement, the following formula is used:

Measurement (a) + Measurement (b) - Measurement (c)

CLK PERIOD:

CLK (a) + (b) – (c) = CLK PERIOD:

CC to CLK setup time:

CC (a) + (b) – (c) = CC to CLK setup time

T[5:0] to CLK setup time:

T[5:0] (a) + (b) – (c) = T[5:0] to CLK setup time

$\overline{RESET}$ to CLK setup time:

$\overline{RESET}$ (a) + (b) – (c) = $\overline{RESET}$ to CLK setup time

2. These hold time parameters are tested on a sample basis.

SWITCHING CHARACTERISTICS over MILITARY operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Test Conditions	29CPL141/ 29CPL151 Min.	29CPL141/ 29CPL151 Max.	29CPL141-1/ 29CPL151-1 Min.	29CPL141-1/ 29CPL151-1 Max.	Unit
1	t_{PD}	CLK to P[15:0]	See Test Output Load Conditions		20			ns
2		CLK to A[5:0]			30			ns
3		CLK to $\overline{ZERO}$			25			ns
4		DCLK to SDO			30			ns
5		Mode to SDO			30			ns
6		SDI to SDO			30			ns
7	t_S	T[2:0] to CLK, Registered Mode		10				ns
8		T[5:3] to CLK, Registered Mode		12				ns
9		T[5:0] to CLK, Async Mode (Note 1)		35				ns
10		CC to CLK, Registered Mode		10				ns
11		CC to CLK, Async Mode (Note 1)		40				ns
12		$\overline{RESET}$ to CLK, Registered Mode		16				ns
13		RESET to CLK, Async Mode (Note 1)		35				ns
14		Mode to CLK		25				ns
15		Mode to DCLK		25				ns
16		SDI to DCLK		25				ns
17	t_H	P[15:8] to DCLK		25				ns
18		T[5:0] to CLK		0				ns
19		CC to CLK		0				ns
20		RESET to CLK		0				ns
21		Mode to CLK		0				ns
22		Mode to DCLK		0				ns
23		SDI to DCLK		0				ns
24	t_{PZX}	P[15:8] to DCLK		0				ns
25	t_{PXZ}	CLK to P[15:8] Enable			35			ns
26	t_{PW}	CLK to P[15:8] Disable			35			ns
27		CLK Pulse Width (HIGH and LOW)		15				ns
28	t_P	DCLK Pulse Width (HIGH and LOW)		25				ns
29		CLK Period (Note 1)		40				ns
30		DCLK Period		60				ns

Notes: These parameters are measured indirectly on unprogrammed devices. They are determined as follows:

a. Measure delay from input (CC, T[5:0], $\overline{RESET}$, or CLK) to EPROM address out in test mode. This will measure the delay through the sequence logic.

b. Measure setup time from T[5:0] input through EPROM test columns to pipeline register in verify test column mode. This will measure the delay through the EPROM and register setup.

c. Measure delay from T[5:0] input to EPROM address out in verify test column mode. This will measure the delay through the logic and P[15:0] outputs.

To calculate the desired parameter measurement, the following formula is used:

Measurement (a) + Measurement (b) – Measurement (c)

CLK PERIOD:

CLK (a) + (b) – (c) = CLK PERIOD:

CC to CLK setup time:

CC (a) + (b) – (c) = CC to CLK setup time

T[5:0] to CLK setup time:

T[5:0] (a) + (b) – (c) = T[5:0] to CLK setup time

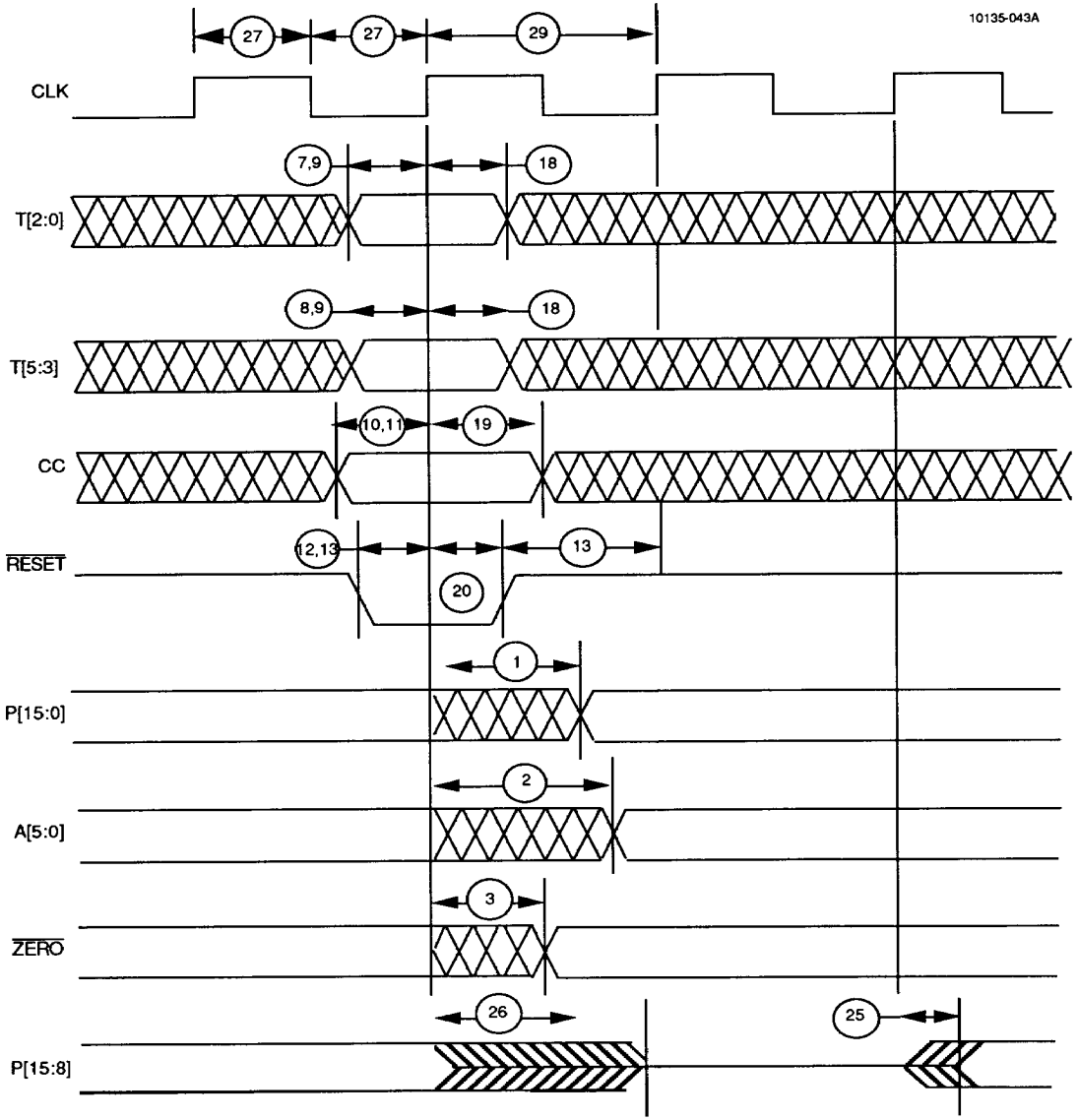
$\overline{RESET}$ to CLK setup time:

$\overline{RESET}$ (a) + (b) – (c) = $\overline{RESET}$ to CLK setup time

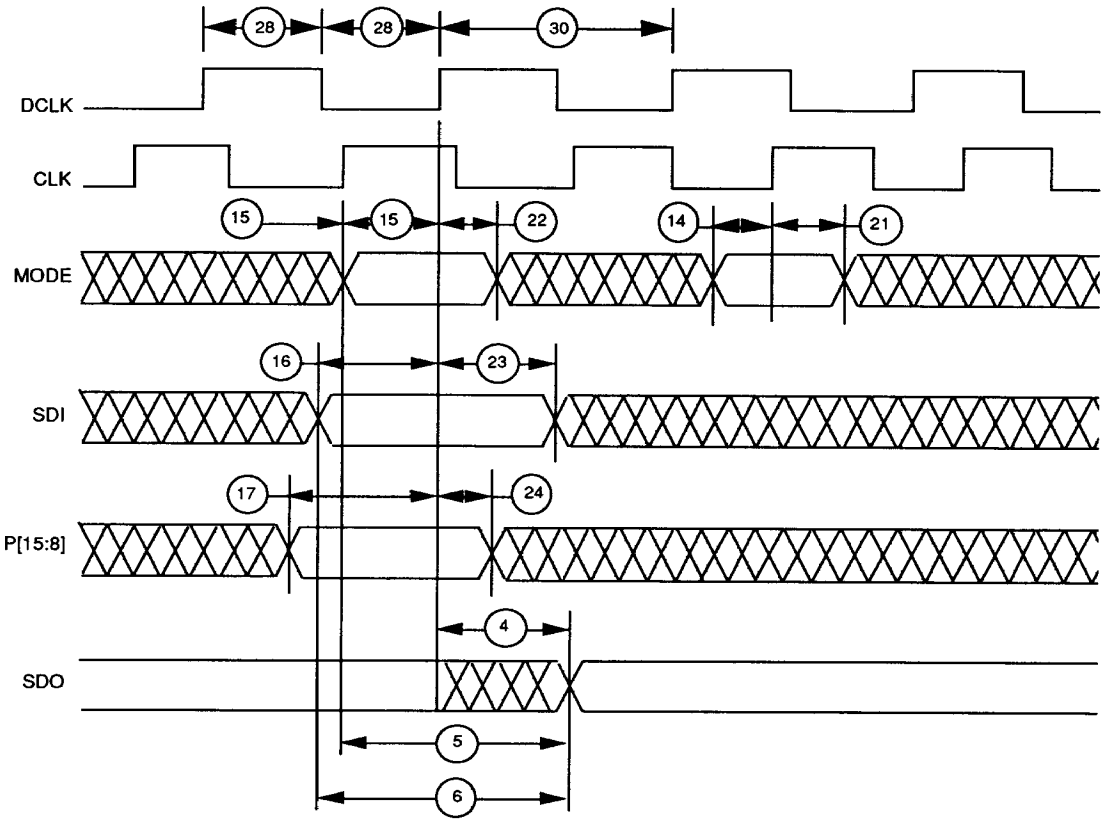
SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from H to L	Will be changing from H to L
	May change from L to H	Will be changing from L to H
	Don't care, any change permitted	Changing, state unknown
	Does not apply	Center line is high impedance "off" state



Normal Configuration



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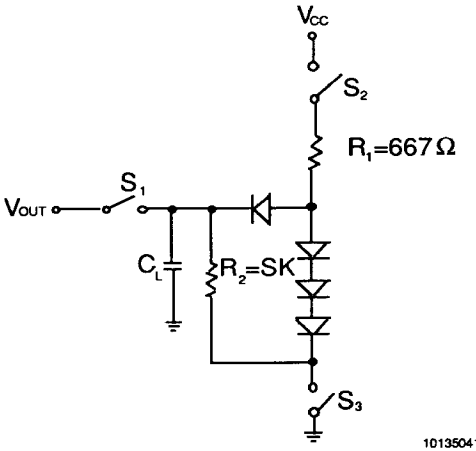
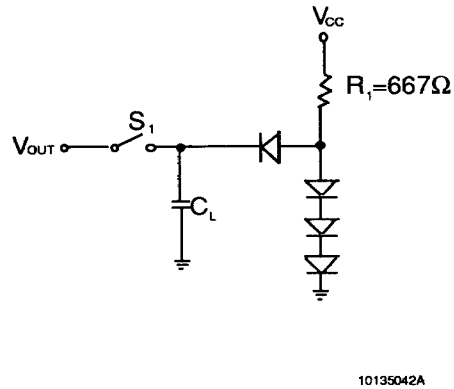
SSR Configuration

SWITCHING TEST CIRCUITS



A. Three-State Outputs

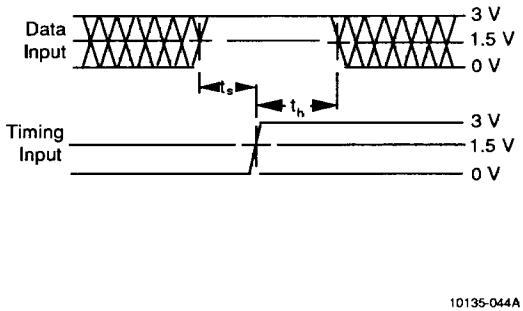


B. Normal Outputs

Notes:

1. CL= 50 pF includes scope probe, wiring, and stray capacitances without device in test fixture.
2. S_1, S_2, and S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S2 is open for t_{pZH} test.
4. C_L= 5.0 pF for output disable tests.

SWITCHING TEST WAVEFORMS



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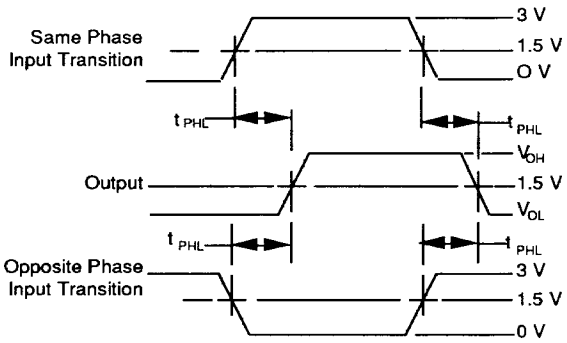
Setup, Hold, and Release Times



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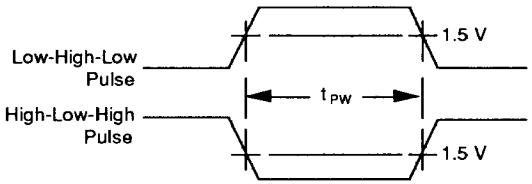
Propagation Delay

Notes:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. S_1, S_2, and S_3 of Load Circuit are closed except where shown.



10135-046A

Pulse Width

Test	V_x	Output Waveform—Measurement Level
All t_{PD}s	5.0 V	V_{OH}, V_{OL}, 1.5 V
t_{PHZ}	0.0 V	V_{OH}, 0.5 V, 0.0 V
t_{PLZ}	5.0 V	V_{OL}, 0.5 V, 3 V
t_{PZH}	0.0 V	0.0 V, 1.5 V, V_{OH}
t_{PZL}	5.0 V	3 V, 1.5 V, V_{OL}

10135-047A

Enable and Disable Times

Notes:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. S_1, S_2, and S_3 of Load Circuit are closed except where shown.

Note: Pulse generator for all pulses: Rate ≤ 1.0 MHz; Z_0 = 50 Ω; tr ≤ 2.5 ns.

Test Philosophy and Methods

The following eight points describe AMD's philosophy for high volume, high speed automatic testing.

1. Ensure that the part is adequately decoupled at the test head. Large changes in VCC current as the device switches may cause erroneous function failures due to VCC changes.

2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.

3. Do not attempt to perform threshold tests at high speed. Following an output transition, ground current may change by as much as 400 mA in 5–8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily.

4. Use extreme care in defining point input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach VIL or VIH until the noise has settled. AMD recommends using VIL≤0 and VIH≥3.0 V for AC tests.

5. To simplify failure analysis, programs should be designed to perform DC, function, and AC tests as three distinct groups of tests.

6. Capacitive Loading for AC Testing

   Automatic testers and their associated hardware have stray capacitance that varies from one type of tester to another but is generally around 50 pF. This, of course, makes it impossible to make direct measurements of parameters which call for smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays," which measure the propagation delays into the high-impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is performed at the higher load capacitance (typically 50 pF), and engineering correlations based on data taken with a bench setup are used to predict the result at the lower capacitance.

   Similarly, a product may be specified at more than one capacitive load. Since the typical automatic tester is not capable of switching loads in mid-test, it is impossible to make measurements at both capacitances even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is predicted from engineering correlations based on data taken with a bench setup and the knowledge that certain DC measurements (for example, IOH, IOL) have already been taken and are within spec. In some cases, special DC tests are performed in order to facilitate this correlation.

7. Threshold Testing

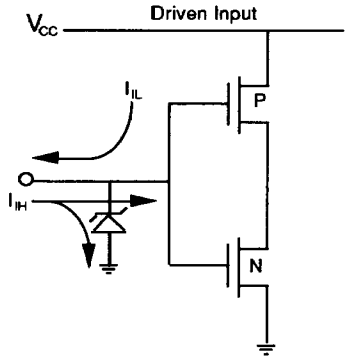
   The noise associated with automatic testing (due to the long, inductive cables) and the high gain of the tested device when in the vicinity of the actual device threshold, frequently give rise to oscillations when testing high-speed circuits. These oscillations are not indicative of a reject device but instead of an overtaxed test system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and AC testing are performed at "hard" input levels rather than at VIL Max. and VIH Min.

8. AC Testing

   Occasionally, parameters are specified that cannot be measured directly on automatic testers because of tester limitations. Data input hold times often fall into this category. In these cases, the parameter in question is guaranteed by correlating these tests with other AC tests that have been performed. These correlations are arrived at by the cognizant engineer by using precise bench measurements in conjunction with the knowledge that certain DC parameters have already been measured and are within spec.

In some cases, certain AC tests are redundant, since they can be shown to be predicted by some other tests which have already been performed. In these cases, the redundant tests are not performed.

INPUT/OUTPUT CIRCUIT DIAGRAMS



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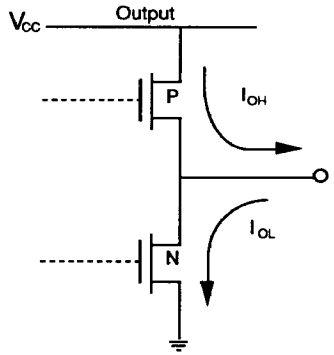

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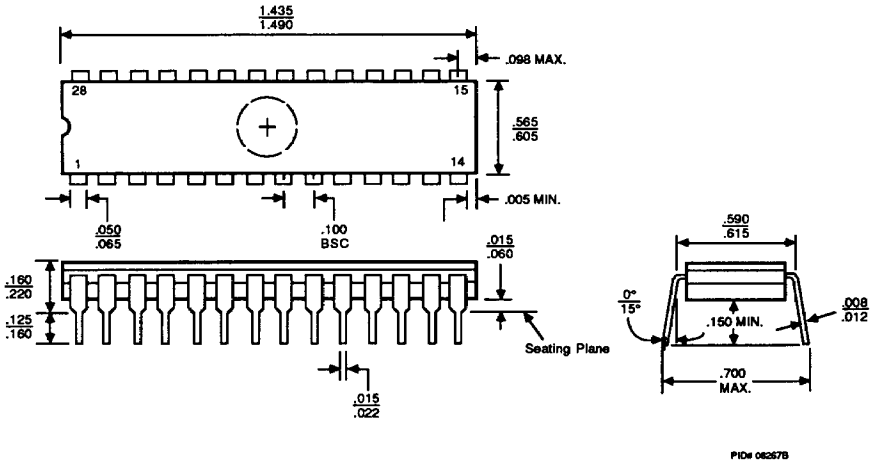

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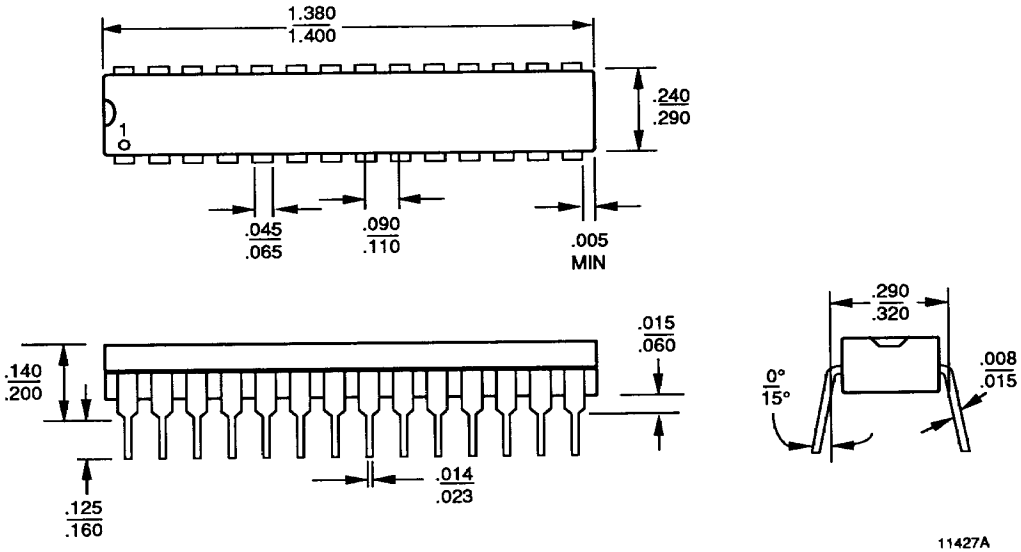
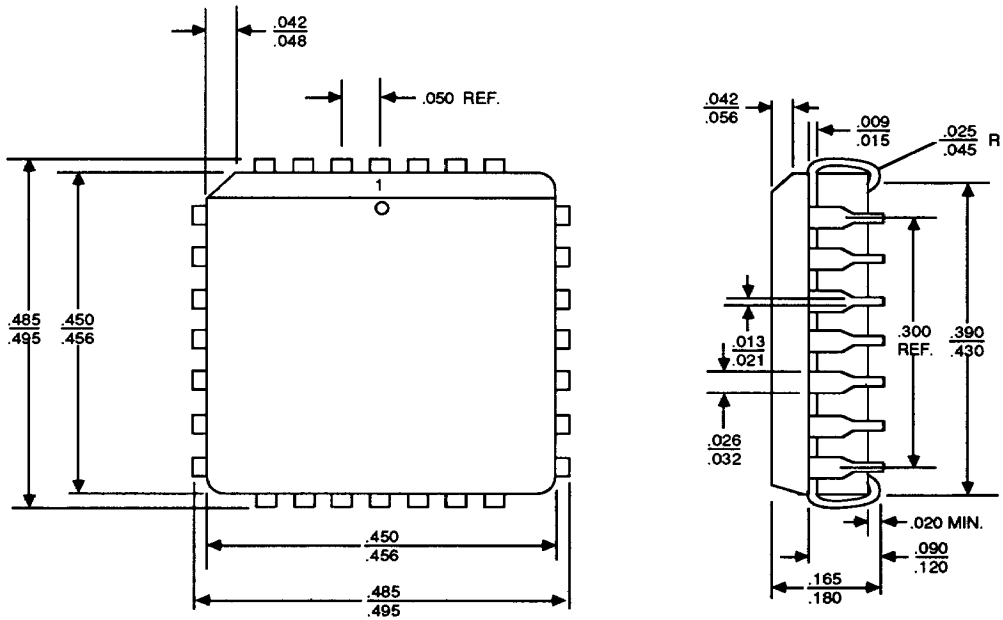


CDE028*

*Package is in development. Consult MCP Product Marketing for information.

PL028



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