Features

- Pin-for-Pin Compatible, Functional Superset of PLS105/A and PLUS405 Logic Sequencers
- Zero Standby Power of Less than 100 µA (Worst Case)
  Power Dissipation at f_{MAX} = 80 mA (Worst Case)
- CMOS and TTL Compatible
- Programmable Asynchronous Initialization and OE Functions
  Controllable from AND Array or External Source
- 17 Input Variables
- 8 Output Functions
- 68 Product Terms
  64 Transition Terms
  4 Control Terms
- 8-bit State Register
- 8-bit Output Register
- 2 Transition Complement Arrays
- Multiple Clocks
- Diagnostic Test Modes Features for Access to State and Output Registers
- Power-on Preset of all Registers to "1"
- J-K Flip-flops
  Automatic Hold States
- Security Fuse
- 3-State Outputs
- Second Source to Signetic's PLC415-16

CMOS Programmable Logic Sequencer (17 x 68 x 8)

8

Description

The ATS415 PLD is a CMOS Programmable Logic Sequencer of the Mealy type. The ATS415 is a pin-for-pin compatible, functional superset of the PLS105 and PLUS405 Bipolar Programmable Logic Sequencer devices.

The ATS415 is ideally suited for high density, power sensitive controller functions. The Power Down feature provides true CMOS standby power levels of less than 100 µA. The EPROM-based process technology supports operating frequencies of 16 to 20 MHz. The ATS415 has been designed to accept both CMOS and TTL input levels to facilitate logic integration in almost any system environment.

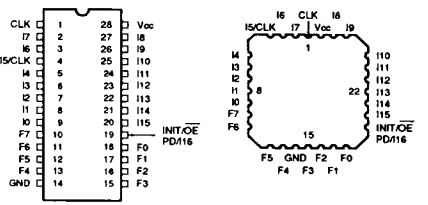
The ATS415 architecture has been tailored for state machine functions. Both arrays are programmable, thus providing full interconnectability. Any one or all of the 64 AND transition terms can be connected to any (or all) of the 8 buried state and 8 output registers.

Two clock sources enable the design of two state machines on one chip. Separate INIT functions and Output Enable functions for each are controllable either from the array or from an external pin. The J-K flip-flops provide the added flexibility of the toggle function which is indeterminate on S-R flip-flops. The programmable initialization feature supports asynchronous initialization of the state machine to any user defined pattern.

The unique Complement Array feature supports complex ELSE transition statements with a single product term. The ATS415 has 2 Complement Arrays which allows the user to design two independent complement functions. This is particularly useful if two state machines have been implemented on one chip.

Pin Configurations

Pin Name	Function
I#/CLK	Clock and Logic Input
I#	Logic Inputs
F#	Bidirectional Buffers
*	No Internal Connection
Vcc	+5V Supply



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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CLK1	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers. Pin 1 only clocks P_{0-3} and F_{0-3} if Pin 4 is also being used as a clock.	Active-High (H)
2, 3, 5–9, 26–27 20–22	$I_0 - I_4, I_7, I_6$ $I_8 - I_9$ $I_{13} - I_{15}$	**Logic Inputs:** The 12 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence. True and complement signals are generated via use of "H" and "L".	Active-High/Low (H/L)
4	I_5/CLK2	**Logic Input/Clock:** A user programmable function:	
		• **Logic Input:** A 13th external logic input to the AND array, as above.	Active-High/Low (H/L)
		• **Clock:** A 2nd clock for the State Registers P_{4-7} and Output Registers F_{4-7}, as above. Note that input buffer I_5 must be deleted from the AND array (i.e., all fuse locations "Don't Care") when using Pin 4 as a Clock.	Active-High (H)
23	I_{12}	**Logic/Diagnostic Input:** A 14th external logic input to the AND array, as above, when exercising standard TTL or CMOS levels. When I_{12} is held at +11V, device outputs $F_0 - F_7$ reflect the contents of State Register bits $P_0 - P_7$. The contents of each Output Register remains unaltered.	Active-High/Low (H/L)
24	I_{11}	**Logic/Diagnostic Input:** A 15th external logic input to the AND array, as above, when exercising standard TTL or CMOS levels. When I_{11} is held at +11V, device outputs $F_0 - F_7$ become direct inputs for State Register bits $P_0 - P_7$; a Low-to-High transition on the appropriate clock line loads the values on pins $F_0 - F_7$ into the State Register bits $P_0 - P_7$. The contents of each Output Register remains unaltered.	Active-High/Low (H/L)
25	I_{10}	**Logic/Diagnostic Input:** A 16th external logic input to the AND array, as above, when exercising standard TTL or CMOS levels. When I_{10} is held at +11V, device outputs $F_0 - F_7$ become direct inputs for Output Register bits $Q_0 - Q_7$; a Low-to-High transition on the appropriate clock line loads the values on pins $F_0 - F_7$ into the Output Register bits $Q_0 - Q_7$. The contents of each State Register remains unaltered.	Active-High/Low (H/L)
10–13 15–18	$F_0 - F_7$	**Logic Outputs/Diagnostic Outputs/Diagnostic Inputs:** Eight device outputs which normally reflect the contents of Output Register Bits $Q_0 - Q_7$, when enabled. When I_{12} is held at +11V, $F_0 - F_7 = (P_0 - P_7)$. When I_{11} is held at +11V, $F_0 - F_7$ become inputs to State Register bits $P_0 - P_7$. When I_{10} is held at +11V, $F_0 - F_7$ become inputs to Output Register bits $Q_0 - Q_7$.	Active-High (H)
19	INIT/$\overline{OE}$ I_{16}/PD	**External Initialization, External /OE, PD or I_{16}:** A user programmable function: Only one of the four options below may be selected. Note that both Initialization and /OE options are alternately available via the AND array. (P-terms INA, INB, OEA, and OEB.)	
		• **External Initialization:** Provides an asynchronous Preset to logic "1" or Reset to logic "0" of any or all State and Output Registers, determined individually on a register-by-register basis. INIT overrides the clock, and when held High, clocking is inhibited. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after the INIT pulse goes Low. See timing diagrams for t_{NVCK} and t_{VCK}. Note that if the External Initialization option is selected, I_{16} is disabled automatically via the design software and the Power Down and External OE options are not available. Internal OE is available via P-Terms OEA and/or OEB. This option can be selected for one or both banks of registers.	Active-High (H)
		• **External Output Enable:** Provides an Output Enable/Disable function for Output Registers. Note that if the External OE option is selected, I_{16} is disabled automatically via the design software and the Power Down and External INIT options are not available. Internal INIT is available via P-terms INA and/or INB. This option can be selected for one or both banks of registers.	Active-Low (L)
		• **Power Down:** When invoked, provides a Power Down (zero power) mode. The contents of all Registers is retained, despite the toggling of the Inputs or the clocks. To obtain the lowest possible power level, all Inputs should be static and at CMOS input levels. Note that if the PD options is selected, I_{16} is disabled automatically via the design software and the External INIT and External OE options are not available. Internal INIT is available via P-terms INA and/or INB and Internal OE is available via P-terms OEA and/or OEB.	Active-High (H)
		• **Logic Input:** The 17th external logic input to the AND array as above. Note that when the I_{16} option is selected, the Power Down, External /OE and External INIT are not available. Internal OE and Internal INIT are available from P-Terms OEA/OEB and INA/INB, respectively.	Active-High/Low (H/L)

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TRUTH TABLE [1, 2, 3, 4, 5]

V_{CC}	OPTION INIT	OPTION $\overline{OE}$	I_{10}	I_{11}	I_{12}	CK	J	K	Q_P	Q_F	F
	H		X	X	X	X	X	X	H/L	H/L	Q_F
	X		+11V	X	X	↑	X	X	Q_P	L	L
	X		+11V	X	X	↑	X	X	Q_P	H	H
	X		X	+11V	X	↑	X	X	L	Q_F	L
	X		X	+11V	X	↑	X	X	H	Q_F	H
	X		X	X	+11V	X	X	X	Q_P	Q_F	Q_P
	L		X	X	X	X	X	X	Q_P	Q_F	Q_F
+5V		H	X	X	X	X	X	X	Q_P	Q_F	Hi-Z
		X	+11V	X	X	↑	X	X	Q_P	L	L
		X	+11V	X	X	↑	X	X	Q_P	H	H
		X	X	+11V	X	↑	X	X	L	Q_F	L
		X	X	+11V	X	↑	X	X	H	Q_F	H
		L	X	X	+11V	X	X	X	Q_P	Q_F	Q_P
		L	X	X	X	X	X	X	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	L	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	H	L	L	L
		L	X	X	X	↑	H	L	H	H	H
		L	X	X	X	↑	H	H	$\overline{Q_P}$	$\overline{Q_F}$	$\overline{Q_F}$
↑	L	L	X	X	X	X	X	X	H	H	H

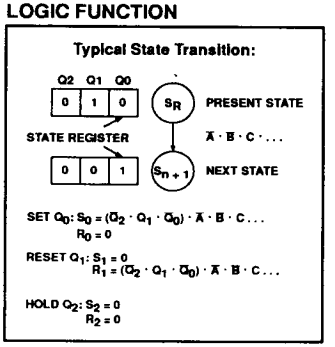
NOTES:
1. Positive Logic:
   S/R (or J/K) = $T_0 + T_1 + T_2 + \ldots T_{63}$
   $T_n = (C_0, C_1)(I_0, I_1, I_2, \ldots)(P_0, P_1 \ldots P_7)$
2. ↑ denotes transition from Low-to-High level.
3. X = Don't Care (≤5.5V)
4. H/L implies that either a High or a Low can occur, depending upon user-programmed Initialization selection (each State and Output Register individually programmable).
5. When using the F_n pins as inputs to the State and Output Registers in diagnostic mode, the F buffers are 3-Stated and the indicated levels on the output pins are forced by the user.

VIRGIN STATE

A factory-shipped virgin device contains all fusible links intact, such that:

1. INIT/$\overline{OE}$/PD/I_{16} is set to INIT. In order to use the INIT function, the user must select either the PRESET or the RESET option for each flip-flop. Note that regardless of the user-programmed initialization, or even if the INIT function is not used, all registers are preset to "1" by the power-up procedure.
2. All transition terms are inactive (0).
3. All J/K flip-flop inputs are disabled (0).
4. The Complement Arrays are inactive.
5. Clock 1 is connected to all State and Output Registers.

LOGIC FUNCTION



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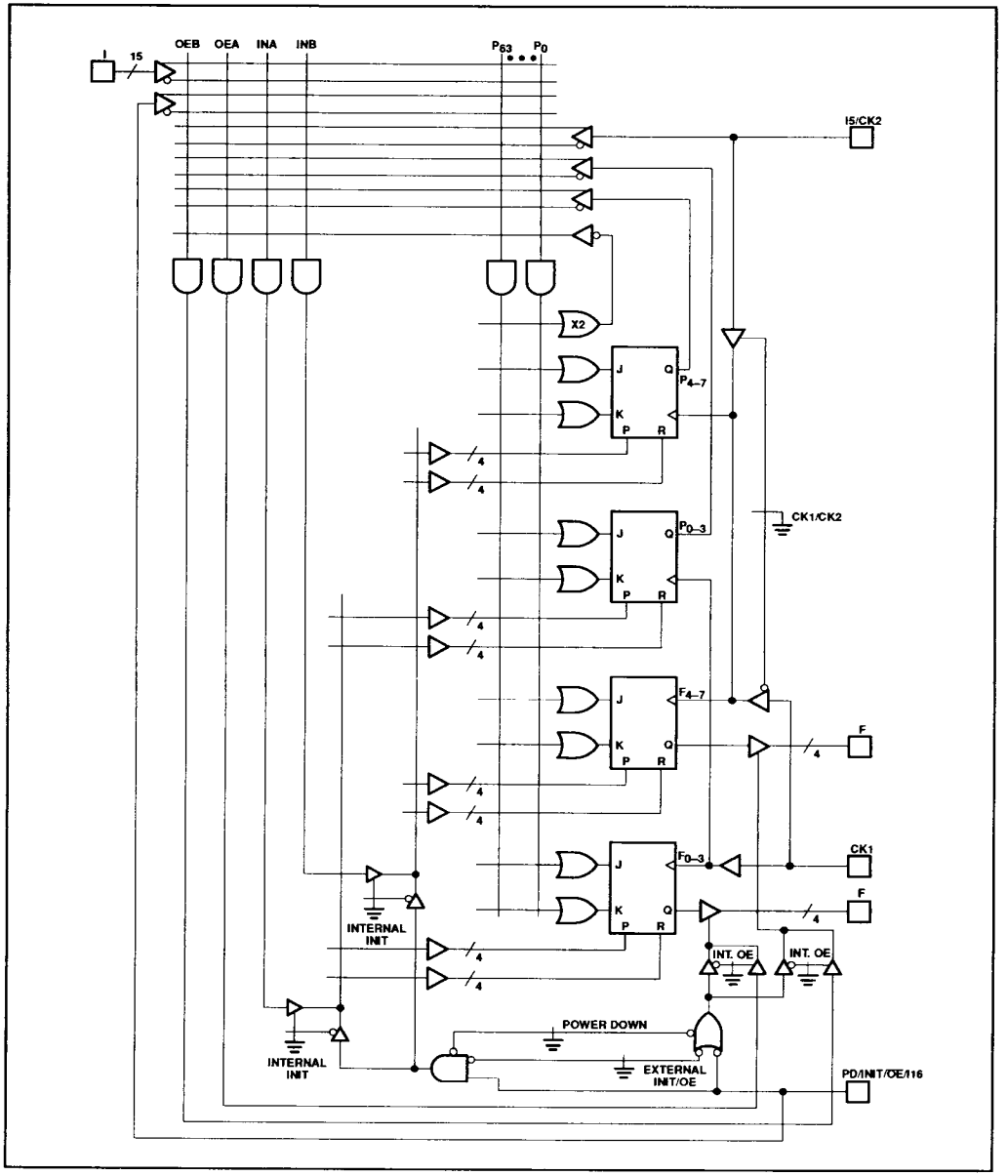
FUNCTIONAL DIAGRAM



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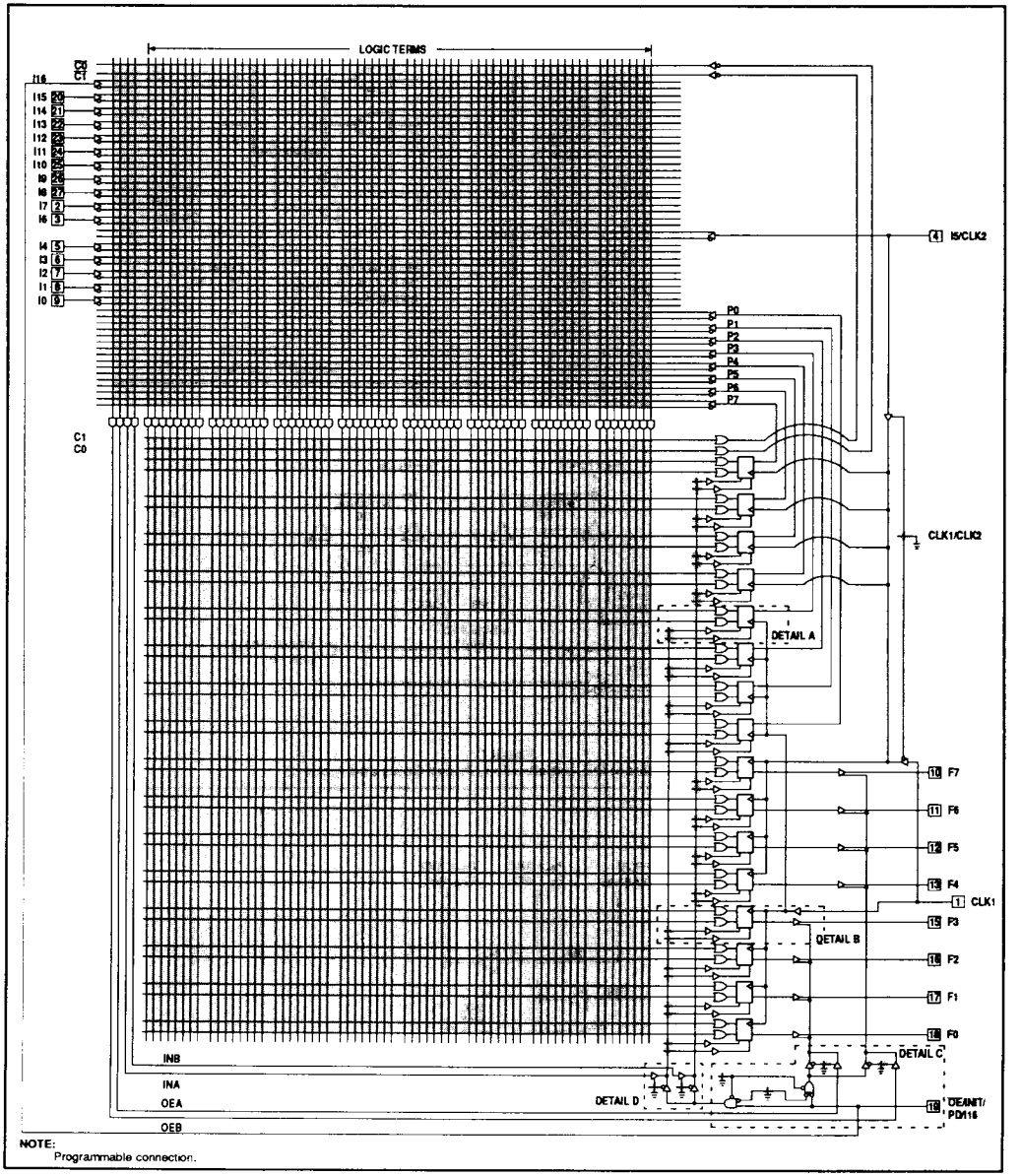
LOGIC DIAGRAM



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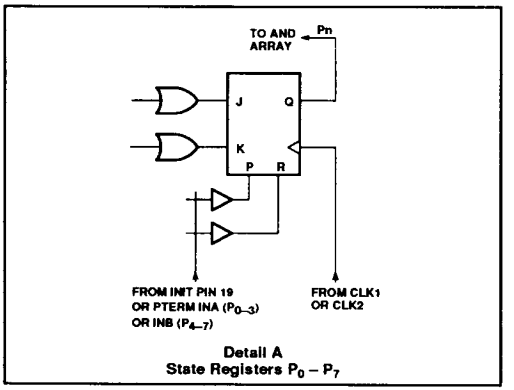
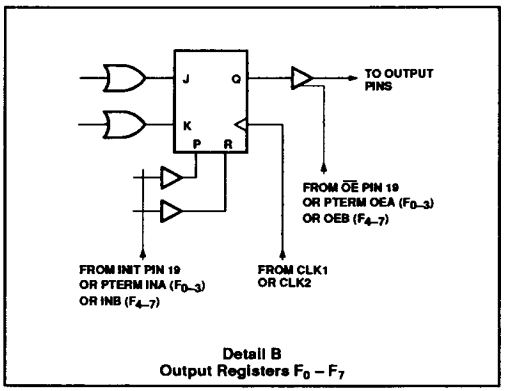
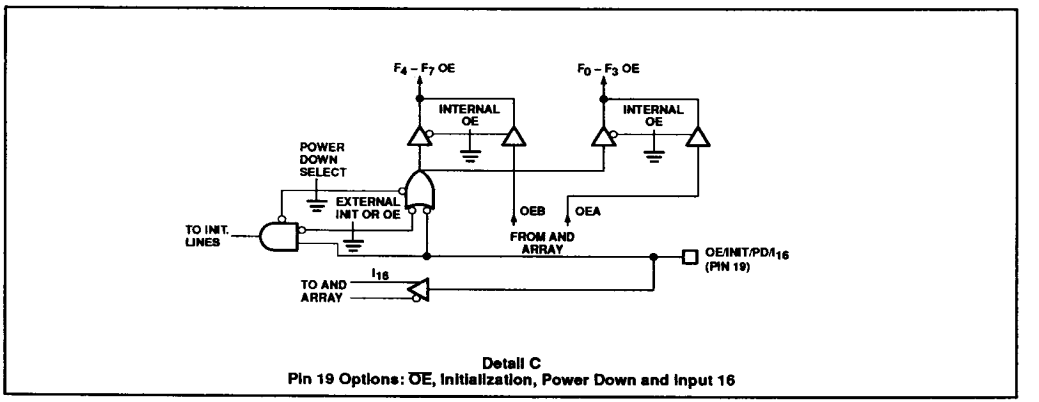
DETAILS FOR PLC415–16 LOGIC DIAGRAM



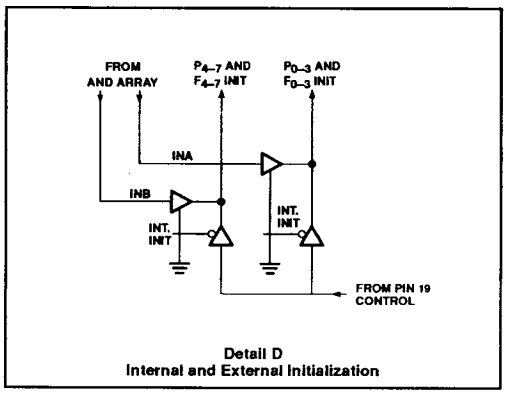
Detail A
State Registers $P_0 - P_7$



Detail B
Output Registers $F_0 - F_7$



Detail C
Pin 19 Options: $\overline{OE}$, Initialization, Power Down and Input 16



Detail D
Internal and External Initialization

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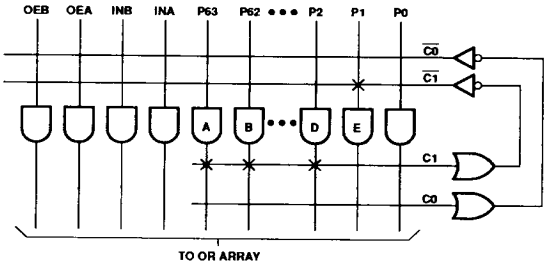
DETAILS FOR PLC415–16 LOGIC DIAGRAM (Continued)



Complement Array Detail

The Complement Array is a special sequencer feature that is often used for detecting illegal states. It is also ideal for generating IF-THEN-ELSE logic statements with a minimum number of product terms.

The concept is deceptively simple. If you subscribe to the theory that the expressions (/A • /B • /C) and ($\overline{A + B + C}$) are equivalent, you will begin to see the value of this single term NOR array.

The Complement Array is a single OR gate with inputs from the AND array. The output of the Complement Array is inverted and fed back to the AND array (NOR). The output of the array will be Low if any one or more of the AND terms connected to it are active (High). If, however, all the connected terms are inactive (Low), which is a classic unknown state, the output of the Complement Array will be High.

Consider the Product Terms A, B and D that represent defined states. They are also connected to the input of the Complement Array. When the condition (not A and not B and not D) exists, the Complement Array will detect this and propagate an Active-High signal to the AND array. This signal can be connected to Product Term E, which could be used in turn to reset the state machine to a known state. Without the Complement Array, one would have to generate product terms for all unknown or illegal states. With very complex state machines, such an approach can be prohibitive, both in terms of time and wasted resources.

Note that the PLC415–16 has 2 Complement Arrays which allow the user to design 2 independent Complement functions. This is particularly useful if 2 independent state machines have been implemented on one device.

Note that use of the Complement Array adds an additional delay path through the device. Please refer to the AC Electrical Characteristics for details.

8

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage	+5.5	V_{DC}
I_{IN}	Input currents	–30 to +30	mA
I_{OUT}	Output currents	+100	mA
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	–65 to +150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

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DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75 \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITION		LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Input voltage[2]							
V_{IL}	Low	V_{CC} = MIN		–0.3		0.8	V
V_{IH}	High	V_{CC} = MAX		2.0		V_{CC} + 0.3	V
Output voltage[2]							
V_{OL}	Low	V_{CC} = MIN I_{OL} = 16mA				0.5	V
V_{OH}	High	I_{OH} = –3.2mA		2.4			V
Input current							
I_{IL}	Low	V_{IN} = GND				–10	µA
I_{IH}	High	V_{IN} = V_{CC}				10	µA
Output current							
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = V_{CC} V_{OUT} = GND				10 –10	µA µA
I_{OS}	Short-circuit [3, 6]	V_{OUT} = GND				–130	mA
I_{CCSB}	V_{CC} supply current with PD asserted[7]	V_{CC} = MAX V_{IN} = 0 or V_{CC}			50	100	µA
I_{CC}	V_{CC} supply current Active [4, 5]	I_{OUT} = 0mA	at f = 1MHz			55	mA
	(TTL or CMOS Inputs)	V_{CC} = MAX	at f = MAX			80	mA
Capacitance							
C_I	Input	V_{CC} = 5V V_{IN} = 2.0V			12		pF
C_B	I/O	V_B = 2.0V			15		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Duration of short-circuit should not exceed one second. Test one at a time.
4. Tested with TTL input levels: V_{IL} = 0.45V, V_{IH} = 2.4V. Measured with all inputs and outputs switching.
5. Refer to Figure 1, I_{CC} vs Frequency (worst case).
6. Refer to Figure 2 for Δt_{PD} vs output capacitance loading.
7. The outputs are automatically 3-Stated when the device is in the Power Down mode. To achieve the lowest possible current, the inputs and clocks should be at CMOS static levels.

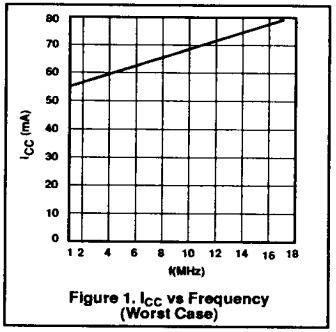

Figure 1. I_{CC} vs Frequency (Worst Case)

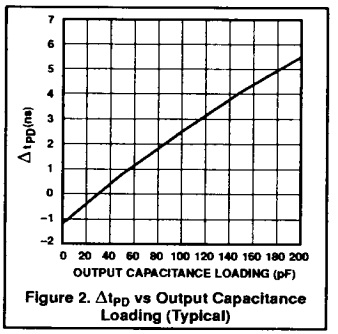

Figure 2. Δt_{PD} vs Output Capacitance Loading (Typical)

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AC ELECTRICAL CHARACTERISTICS

$R_1 = 252\Omega$, $R_2 = 178\Omega$, $0°C \leq T_{amb} \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Pulse width								
t_{CKH}	Clock High	CK+	CK–	30pF	25	10		ns
t_{CKL}	Clock Low	CK–	CK+	30pF	25	10		ns
t_{INITH}	Initialization Input pulse	INIT+	INIT–	30pF	20			ns
Set–up time								
t_{IS1}	Input	(I) +/–	CK+	30pF	38	25		ns
t_{IS2}[1]	Input through Complement array	(I) +/–	CK+	30pF	60	40		ns
t_{ISPD}	Power Down Setup (from PD pin)	PD+	CK+	30pF	38	15		ns
t_{ISPU}	Power Up Setup (from PD pin)	PD–	First Valid CK+	30pF	38	30		ns
t_{VS}[1]	Power on Preset Setup	V_{CC}+	CK–	30pF	0			ns
t_{VCK1}	Clock resume (after INIT) when using INIT pin (pin 19)	INIT–	CK–	30pF	10	–5		ns
t_{VCK2}[1]	Clock resume (after INIT) when using P-term INIT (from AND array)	(I) +/–	CK–	30pF	20	8		ns
t_{NVCK1}	Clock lockout (before INIT) when using INIT pin (pin 19)	CK–	INIT–	30pF	10	–3		ns
t_{NVCK2}[1]	Clock lockout (before INIT) when using P-term INIT (from AND array)	CK–	INIT–	30pF	0	–5		ns
Propagation delays								
t_{CKO}	Clock to Output	CK+	(F) +/–	30pF		15	22	ns
t_{PDZ}	Power Down to outputs off	PD+	Outputs Off	5pF		25	30	ns
t_{PUA1}	Power Up to outputs Active with dedicated Output Enable	PD–	Outputs Active	30pF		20	35	ns
t_{PUA2}[1]	Power Up to outputs Active with P-term Output Enable[1]	PD–	Outputs Active	30pF		37	55	ns
t_{IHPU}	Last valid clock to Power Down delay (Hold)	Last Valid Clock	PD+	30pF	25	15		ns
t_{IHPD}	First valid clock cycle before Power Up	Beginning of First Valid Clock Cycle	PD–	30pF	0	–25		ns
t_{OE1}[3]	Output Enable: from /OE pin	OE–	Output Enabled	30pF		15	30	ns
t_{OE2}[1]	Output Enable; from P–term	(I) +/–	Output Enabled	30pF		25	40	ns
t_{OD1}[3]	Output Disable; from /OE pin	OE+	Output Disabled	5pF		20	30	ns
t_{OD2}[3]	Output Disable; from P-term	(I) +/–	Output Disabled	5pF		30	40	ns
t_{INIT1}	INIT to output when using INIT pin	INIT+	(F) +/–	30pF		22	35	ns
t_{INIT2}	INIT to output when using P-term INIT	(I) +/–	(F) +/–	30pF		35	45	ns
t_{PPR}[1]	Power-on Preset (F_n = 1)	V_{CC} +	(F) +	30pF			15	ns
t_{RP1}	Registered operating period; ($t_{IS1} + t_{CKO1}$)	(I) +/–	(F) +/–	30pF		40	60	ns
t_{RP2}[1]	Registered operating period with Complement Array ($t_{IS2} + t_{CKO1}$)	(I) +/–	(F) +/–	30pF		55	75	ns

Notes on following page

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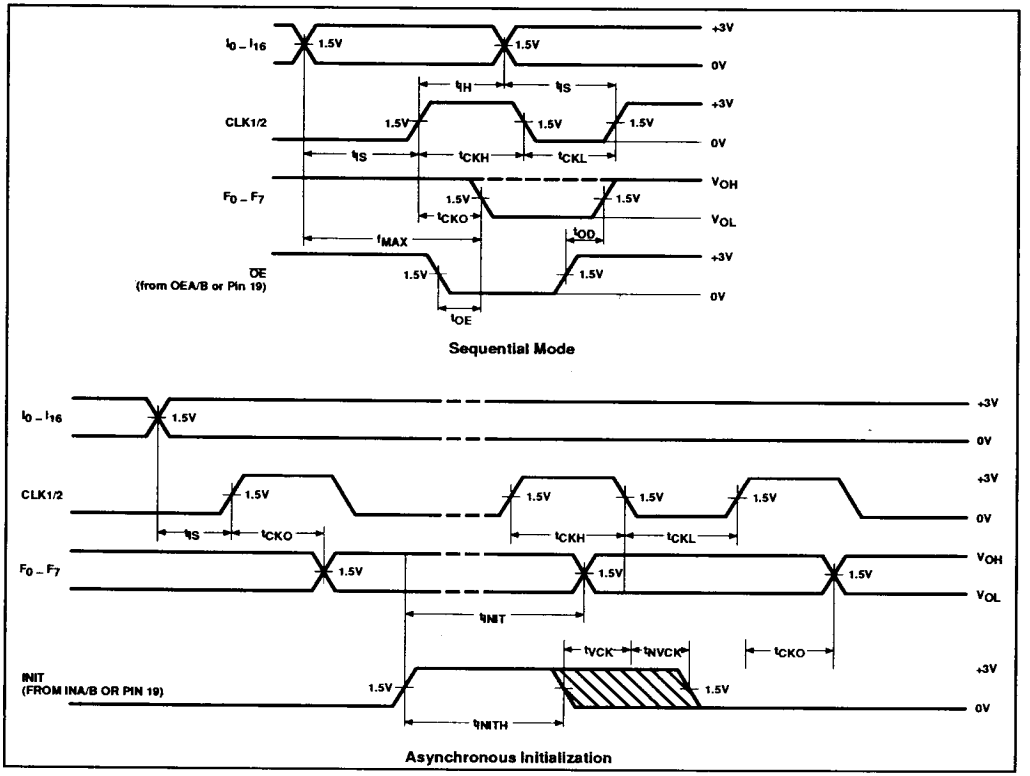
AC ELECTRICAL CHARACTERISTICS (Continued)

$R_1 = 252\Omega$, $R_2 = 178\Omega$, $0°C \le T_{amb} \le +75°C$, $4.75 \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Hold time								
t_{IH}	Input Hold	CK+	(F) +/–	30pF		–10	0	ns
Frequency of operation								
f_{CLK}[1]	Clock (toggle) frequency	C+	C+	30pF	20	50		MHz
f_{MAX1}	Registered operating frequency ($t_{IS1} + t_{CKO1}$)	(I) +/–	(F) +/–	30pF	16.7	25		MHz
f_{MAX2}	Registered operating frequency with Complement Array ($t_{IS2} + t_{CKO1}$)	(I) +/–	(F) +/–	30pF	13.3	18.2		MHz

NOTE:
1. Not 100% tested, but guaranteed by design/characterization.
2. All propagation delays and setup times are measured and specified under worst case conditions.
3. For 3-State output; output enable times are tested with $C_L = 30pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.

TIMING DIAGRAMS



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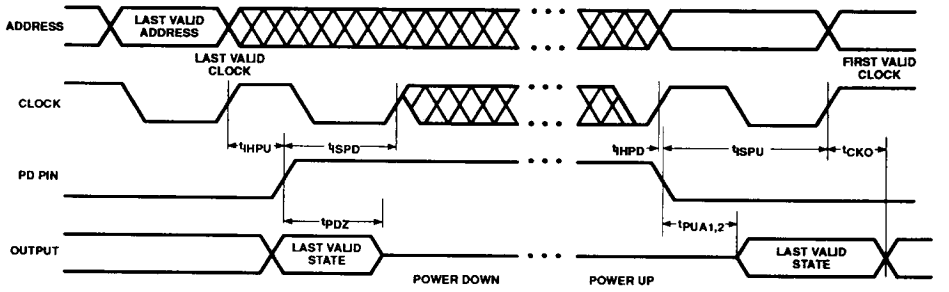
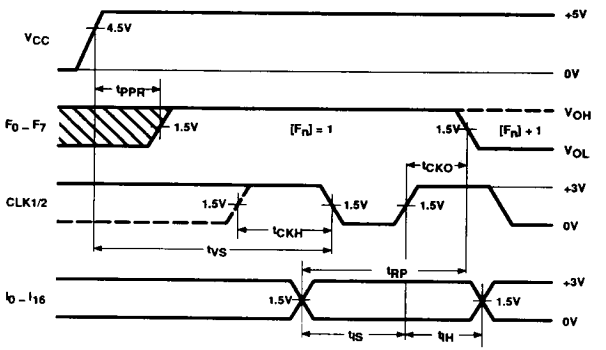
The PLC415–16 has a unique power down feature that is ideal for power sensitive controller and state machine applications. During idle periods, the PLC415 can be powered down to a near zero power consumption level of less than 100 micro Amps. Externally controlled from Pin 19, the power down sequence first saves the data in all the State and Output registers. In order to insure that the last valid states are saved, there are certain hold times associated with the first and last valid clock edges and the Power Down input pulse. The Outputs are then automatically 3-Stated and power consumption is reduced to a minimum.

Once in the power down mode, any or all of the inputs, including the clocks, may be toggled without the loss of data. To obtain the lowest possible power level, the inputs should be at static CMOS input levels during the power down period.

TIMING DIAGRAMS (Continued)



Power Down Enable and Disable



Power-On Preset

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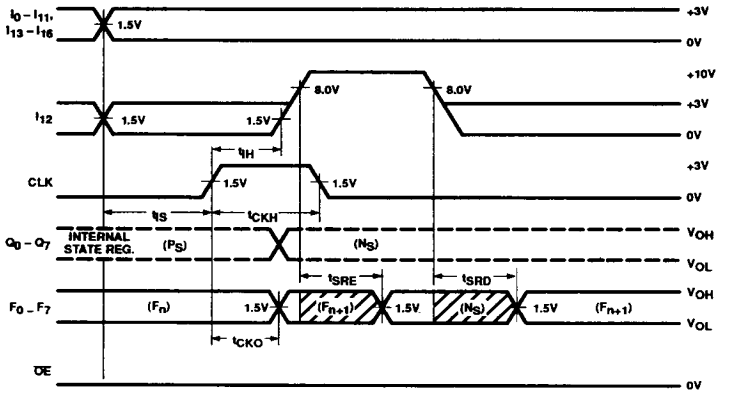
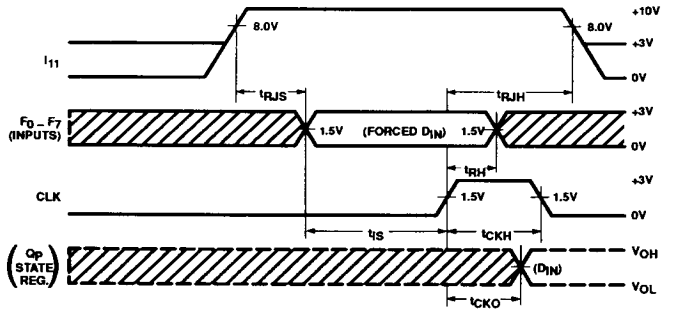
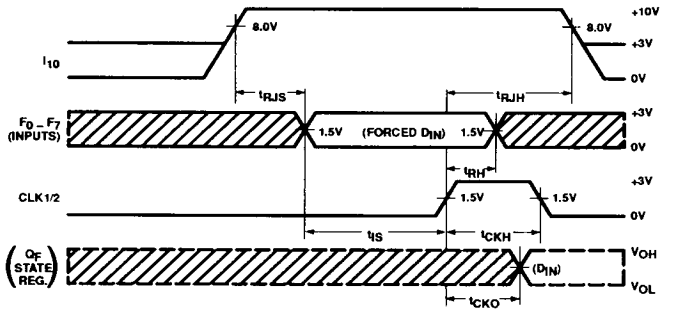
TIMING DIAGRAMS (Continued)



Diagnostic Mode—State Register Outputs



Diagnostic Mode—State Register Input Jam



Diagnostic Mode—Output Register Input Jam

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TIMING DEFINITIONS

SYMBOL	PARAMETER
f_{CLK}	Minimum guaranteed toggle frequency of the clock (from Clock HIGH to Clock HIGH).
$f_{MAX1,2}$	Minimum guaranteed operating frequency.
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{RP1}	Minimum guaranteed operating period – when not using Complement Array.
t_{RP2}	Minimum guaranteed operating period – when using Complement Array.
t_{CKO}	Delay between positive transition of Clock and when Outputs become valid (with outputs enabled).
t_{IH}	Required delay between positive transition of Clock and end of valid Input data.
t_{IHPD}	Required delay between the positive transition of the beginning of the first valid clock cycle to the beginning of Power Down LOW to insure that the last valid states are intact and that the next positive transition of the clock is valid.
t_{IHPU}	Required delay between the positive transition of the last valid clock and the beginning of Power Down HIGH to insure that last valid states are saved.
t_{INITH}	Width of initialization input pulse.
t_{INIT1}	Delay between positive transition of Initialization and when Outputs become valid when using external INIT control (from pin 19).
t_{INIT2}	Delay between positive transition of Initialization and when outputs become valid when using internal INIT control (from P-terms INA and INB).
t_{ISPD}	Required delay between the beginning of Power Down HIGH (from pin 19) and the positive transition of the next clock to insure that the clock edge is not detected as a valid Clock and that the last valid states are saved.

SYMBOL	PARAMETER
t_{ISPU}	Required delay between the beginning of Power Down LOW and the positive transition of the first valid clock.
t_{IS1}	Required delay between beginning of valid input and positive transition of Clock.
t_{IS2}	Required delay between beginning of valid input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND Array).
t_{NVCK1}	Required delay between the negative transition of the clock and the negative transition of the Asynchronous Initialization when using external INIT control (from pin 19) to guarantee that the clock edge is not detected as a valid negative transition.
t_{NVCK2}	Required delay between the negative transition of the clock and the negative transition of the Asynchronous Initialization, when using the internal INIT control (from P-terms INA and INB), to guarantee that the clock edge is not detected as a valid negative transition.
t_{OD1}	Delay between beginning of Output Enable High and when Outputs are in the OFF-State, when using external OE control (from pin 19).
t_{OD2}	Delay between beginning of Output Enable High and when outputs are in the OFF-State when using internal OE control (from P-terms OEA and OEB).
t_{OE1}	Delay between beginning of Output Enable Low and when Outputs become valid when using external OE control from pin 19.
t_{OE2}	Delay between beginning of Output Enable Low and when outputs become valid when using internal OE control (from P-terms OEA and OEB).
t_{PDZ}	Delay between beginning of Power Down HIGH and when outputs are in OFF–State and the circuit is "powered down".

SYMBOL	PARAMETER
t_{PPR}	Delay between V_{CC} (after power-on) and when Outputs become preset at "1".
$t_{PUA1,2}$	Delay between beginning of Power Down LOW and when outputs become Active (valid) and the circuit is "powered up". See AC Specifications.
t_{RH}	Required delay between positive transition of Clock and end of valid Input data when jamming data into State or Output Registers in diagnostic mode.
t_{RJH}	Required delay between positive transition of Clock and end of inputs I_{11} or I_{10} transition to State and Output Register Input Jam Diagnostic Modes, respectively.
t_{RJS}	Required delay between when inputs I_{11} or I_{10} transition to State and Output Register Input Jam Diagnostic Modes, respectively, and when the output pins become available as inputs.
t_{SRD}	Delay between input I_{12} transition to Logic mode and when the Outputs reflect the contents of the Output Register.
t_{SRE}	Delay between input I_{12} transition to Diagnostic Mode and when the Outputs reflect the contents of the State Register.
t_{VCK1}	Required delay between negative transition of Asynchronous Initialization and negative transition of Clock preceding the first valid clock pulse when using external INIT control (pin 19).
t_{VCK2}	Required delay between the negative transition of the Asynchronous Initialization and the negative transition of the clock preceding the first valid clock pulse when using internal INIT control (from P–terms INA and INB).
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of Clock preceding first reliable clock pulse.

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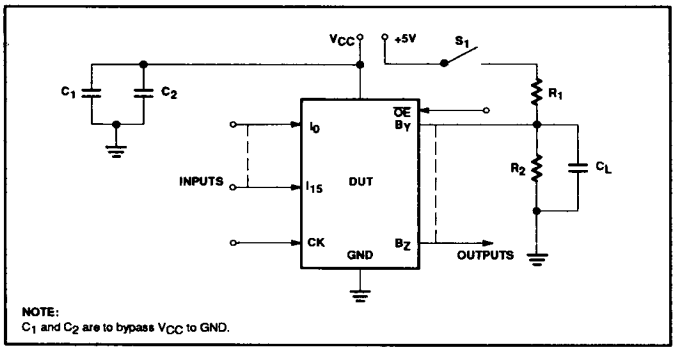
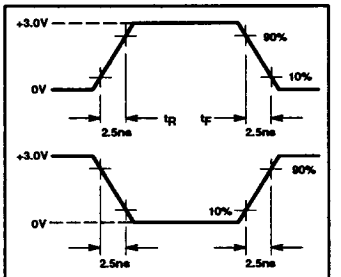
TEST LOAD CIRCUIT



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

LOGIC PROGRAMMING

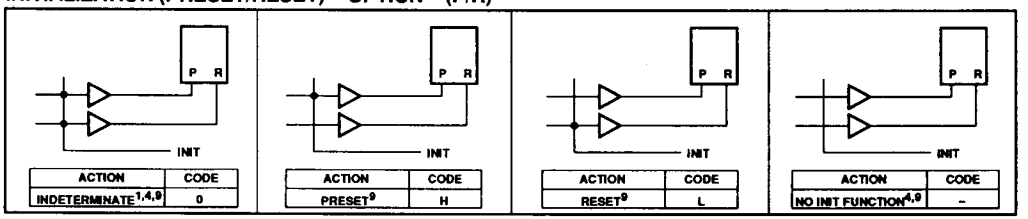
The PLC415–16 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics AMAZE, SLICE and SNAP design software packages. ABEL™ and CUPL™ design software packages also support the PLC415–16 architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLC415–16 logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by AMAZE and SLICE only. Both AMAZE and SLICE design packages are available, free of charge, to qualified users.

To implement the desired logic functions, each logic variable (I, B, P, S, T, etc.) from the logic equations if assigned a symbol. TRUE, COMPLEMENT, PRESET, RESET, OUTPUT ENABLE, INACTIVE, etc., symbols are defined below.

INITIALIZATION (PRESET/RESET)[11] OPTION – (P/R)



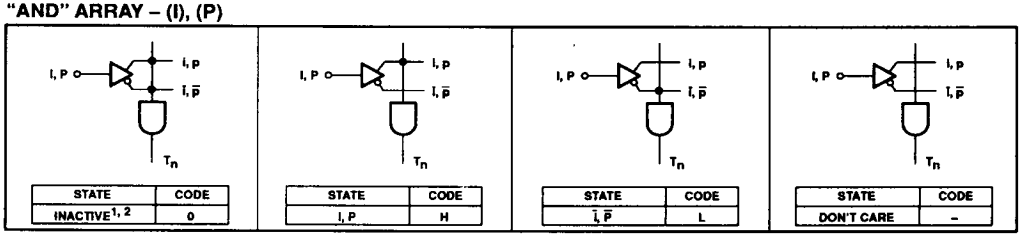
ACTION	CODE
INDETERMINATE[1,4,9]	0

ACTION	CODE
PRESET[9]	H

ACTION	CODE
RESET[9]	L

ACTION	CODE
NO INIT FUNCTION[4,9]	–

"AND" ARRAY – (I), (P)



STATE	CODE
INACTIVE[1, 2]	0

STATE	CODE
I, P	H

STATE	CODE
$\overline{I}$, $\overline{P}$	L

STATE	CODE
DON'T CARE	–

Notes on page 8-138

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

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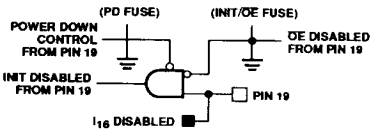
LOGIC PROGRAMMING (Continued)

PIN 19 FUNCTION: POWER DOWN, INIITALIZATION, $\overline{OE}$, OR INPUT

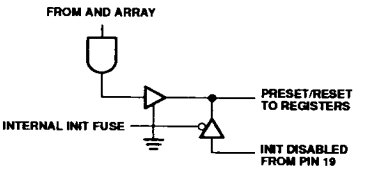
Power Down Mode



POWER DOWN FUSE	CODE
PIN 19 AS POWER DOWN	H[6]

EXTERNAL INIT/OE FUSE	CODE
EXTERNAL INIT/OE DISABLED	L

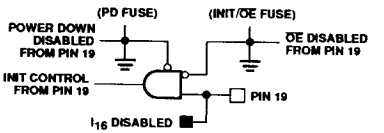
P-Term Initialization Control



INTERNAL INIT FUSES	CODE
P-TERM INIT CONTROL	H[7, 8]

POWER DOWN FUSE	CODE
POWER DOWN ENABLED OR DISABLED	H OR L

External Initialization Control

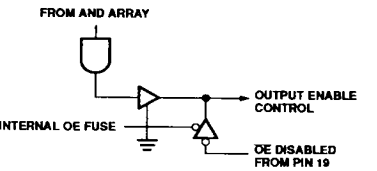


PD FUSE	CODE
POWER DOWN DISABLED	L[1]

EXTERNAL INIT/OE FUSE	CODE
PIN 19 AS EXTERNAL INIT	L[1]

INTERNAL INIT FUSES	CODE
P-TERM INIT ACTIVE OR INACTIVE	H OR L[7, 8]

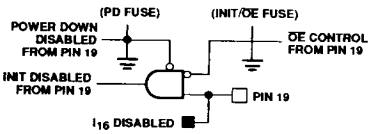
P-Term OE Control



INTERNAL OE FUSES	CODE
P-TERM OE CONTROL	H[7, 8]

POWER DOWN FUSE	CODE
POWER DOWN ENABLED OR DISABLED	H OR L

External Output Enable Control



PD FUSE	CODE
POWER DOWN DISABLED	L

EXTERNAL INIT/OE FUSE	CODE
PIN 19 AS EXTERNAL OE	H

INTERNAL INIT FUSES	CODE
P-TERM OE ACTIVE OR INACTIVE	H OR L[7, 8]

Notes are on page 17.

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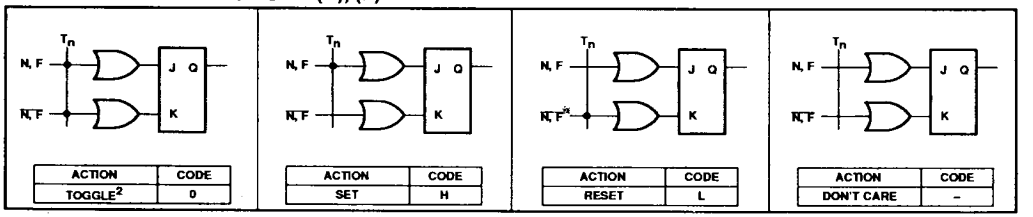
LOGIC PROGRAMMING (Continued)

"OR" ARRAY – J-K FUNCTION – (N), (F)



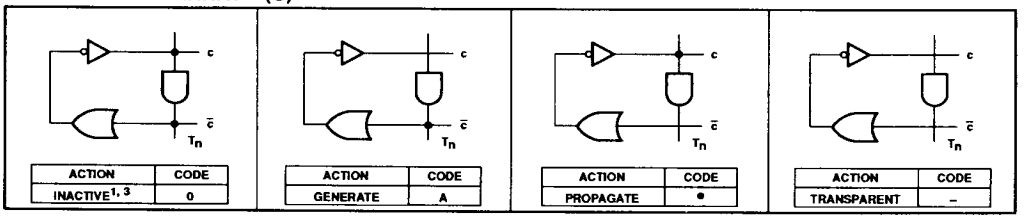
ACTION	CODE
TOGGLE[2]	0

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
DON'T CARE	–

"COMPLEMENT" ARRAY – (C)



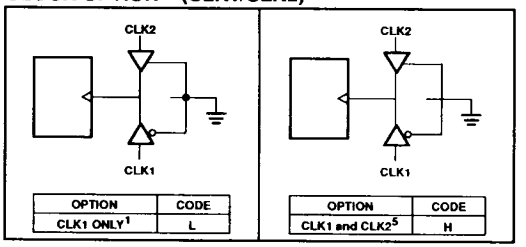
ACTION	CODE
INACTIVE[1, 3]	0

ACTION	CODE
GENERATE	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

CLOCK OPTION – (CLK1/CLK2)



OPTION	CODE
CLK1 ONLY[1]	L

OPTION	CODE
CLK1 and CLK2[5]	H

NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate T_n will be unconditionally inhibited if any one of its I or P link pairs is left intact.
3. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.
4. These states are not allowed when using PRESET/RESET option.
5. Input buffer I_5 must be deleted from the AND array (i.e., all fuse locations "Don't Care") when using second clock option.
6. When using Power Down feature, INPUT 16 is automatically disabled via the design software.
7. If the internal (P–term) control fuse for INIT and/or OE is programmed as Active High, the associated External Control function will be permanently disabled, regardless of the state of the External INIT/OE fuse.
8. One internal control fuse exists for each group of 8 registers. P_{0-3} and F_{0-3} are banked together in one group, as are P_{4-7} and F_{4-7}. Control can be split between the INIT/OE pin (Pin 19) and P–terms INA, INB, OEA and OEB.
9. The PLC415–16 also has a power–up preset feature. This feature insures that the device will power–up in a known state with all register elements (State and Output Register) at a logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.
10. L = cell unprogrammed.
    H = cell programmed.
11. Inputs 10, 11 and 12 (pins 25, 24, & 23) can be used for supervoltage diagnostic mode tests. It is recommended that these inputs not be connected to product terms INA, INB, OEA or OEB if you intend to make use of the diagnostic modes due to the fact that the patterns associated with the internal INIT and OE control product terms may interfere with the diagnostic mode data loading and reading.

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PROGRAM TABLE

AND

(Im, Ps)		(Cn)	
INACTIVE	O	INACTIVE	O
I, P	H	GENERATE	A
$\overline{I}$, $\overline{P}$	L	PROPAGATE	•
DON'T CARE	–	TRANSPARENT	–

OR (Ns, Fn)

TOGGLE	O
SET	H
RESET	L
NO CHANGE	–

OPTIONS

EXTERNAL INIT	L
EXTERNAL OE	H
INTERNAL INIT/OE ENABLED	H
INTERNAL INIT/OE DISABLED	L
POWER DOWN ENABLED	H
POWER DOWN DISABLED	L
CLOCK 1 ONLY	L
CLOCK 1 AND 2	H

INITIALIZATION	
PRESET	H
RESET	L
NO INIT	–
INDETERMINATE	O

PROJECT NAME _____ DATE _____ REVISION _____

CUSTOMER NAME _____ SIGNETICS PART # _____ CUSTOMER PART # _____

ITEMS	COMP. ARRAY	INTERNAL INIT INB	INTERNAL INIT INA	INTERNAL OE OEB	INTERNAL OE OEA	EXTERNAL INIT/OE	CLK 1/1&2	PD	INITIALIZATION
	NOR	AND							OR
	Cn	INPUT (Im)							PRESENT STATE (Ps)	NEXT STATE (Ns)	OUTPUT (Fn)
	C1	C0	I16	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0	P7	P6	P5	P4	P3	P2	P1	P0	N7	N6	N5	N4	N3	N2	N1	N0	F7	F6	F5	F4	F3	F2	F1	F0
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OEB																																										
INA																																										
OEA																																										
PIN NO.		19	20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9										10	11	12	13	15	16	17	18								
PIN LABELS																																										

NOTES:
1. In the unprogrammed state all cells are conducting. Thus, the program table for an unprogrammed device would contain "0"s for all product terms (inactive) and initialization states (indeterminate). The default or unprogrammed state of all other options is "L".
2. Unused Cn, Im and Ps cells are normally programmed as Don't Care (–).
3. Unused product terms can be left blank (inactive) for future code modification.

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ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the PLC415 Series devices are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps has wavelengths in the 3000 – 4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical PLC415 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the PLC415 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the PLC415 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000μW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2 (1 week @ 12000μW/cm^2). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

The maximum number of guaranteed erase/write cycles is 50. Data retention exceeds 20 years.

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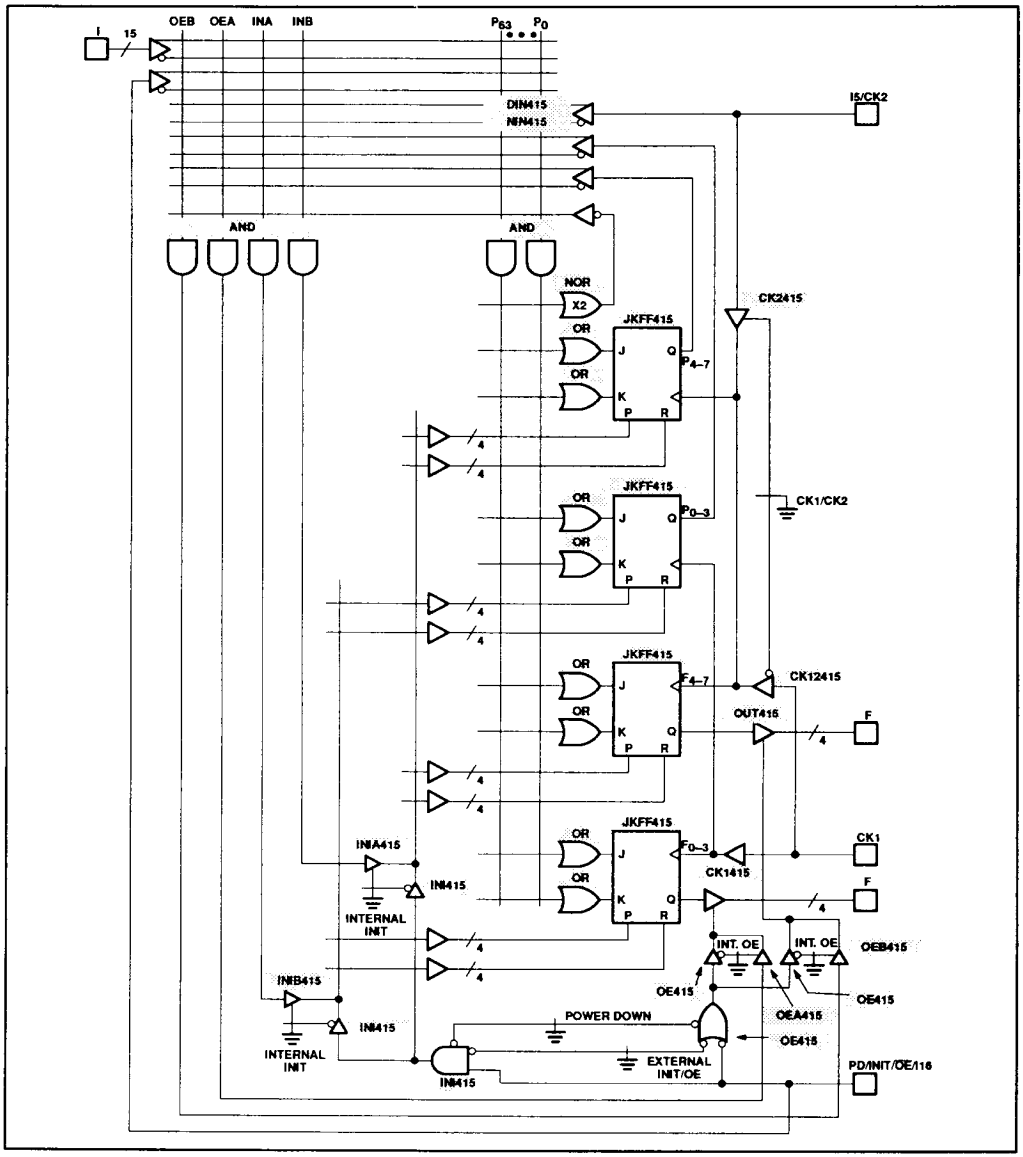
SNAP RESOURCE SUMMARY DESIGNATIONS



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t_{PD} (MHz)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
16	38	22	ATS415-16DC ATS415-16JC ATS415-16PC	28DW6 28J 28P6	Commercial (0°C to 70°C)

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

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