Automotive Body Power Management LSI

Voltage Tracker

BD3925FP-C,BD3925HFP-C

No.11039EBT06

●Description

BD3925FP-C and BD3925HFP-C are voltage trackers for automotive use which feature high withstand-voltage to 50V. They offer the output current loading to 500mA while limiting the quiescent current to 45μA (typ.), so that they suit to apply for systems which are permanently connected to the car battery and requiring low-current-consumption. The offset is ±15mV (for 5V output. 6V < Vcc < 36V, 5mA < Io < 200mA). They integrate folded–type of over-current protection to minimize heat dissipation while accidentally shorted, thus lead to most robust power-supply design under the harsh automotive environment.

●Features

1) Ultra-low quiescent current: 45μA (TYP.)
2) Low-saturation voltage type P-channel DMOS output transistors
3) Low offset voltage: ± 15mV(for 5V output, 6V< Vcc <36V, 5mA<Io<200mA)
4) Vcc power supply voltage = 50 V
5) Integrated over-current protection circuit and thermal shutdown circuit
6) TO252-5/HRP5 Package

●Applications

Onboard vehicle devices (body-control, car stereos, satellite navigation systems, etc.)

●Product line

Part No.	Package
BD3925FP-C	TO252-5
BD3925HFP-C	HRP5

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit
Supply Voltage	Vcc	50 ※1	V
Switch Supply Voltage	VSW	50	V
VADJ Terminal Supply Voltage	VADJ	28	V
Vo Terminal Voltage	Vout	28	V
Output Current	Io	500	mA
Power Dissipation	Pd	1.3 (TO252-5) ※2	W
		1.6 (HRP5) ※3	
Operating Temperature Range	Topr	-40 ~ +125	℃
Storage Temperature Range	Tstg	-55 ~ +150	℃
Maximum Junction Temperature	Tjmax	150	℃

※1 Not to exceed Pd and ASO.
※2 TO252-5: Reduced by 10.4 mW/°C over 25 °C, when mount on a glass epoxy board : 70 mm × 70 mm × 1.6 mm.
※3 HRP5: Reduced by 12.8 mW/°C over 25 °C, when mount on a glass epoxy board : 70 mm × 70 mm × 1.6 mm).
NOTE: This product is not designed for protection against radioactive rays.

●**Operating Conditions**

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	Vcc	4.5 ※4	36.0	V
Input Voltage ※5	VADJ	2.5	14	V
Output Current	Io	—	500	mA

※4 Please consider that the Output voltage would be dropped (Dropout voltage) according to the output current.
※5 Not to exceed Vcc - 0.5V.
NOTE: This product is not designed for protection against radioactive rays.

●**Electrical Characteristics** (Unless otherwise specified, Ta=-40 ~ 125°C, VCC=13.2 V, SW=3V, ADJ=5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Shut Down Current	Ishut	—	—	10	μA	SW=GND
Bias Current	Ib	—	45	90	μA	Io=0mA
Offset Voltage	△Vo	-15	—	15	mV	6V<Vcc<36V, 5mA<IO<200mA
Output Current	Io	0.5	—	—	A	
Dropout Voltage	△Vd	—	0.25	0.48	V	Vcc=5V, VADJ=5V, Io=200mA
Ripple Rejection	R.R.	45	55	—	dB	f=120Hz, ein=1Vrms, Io=100mA
Switch Threshold Voltage H	SWH	2.0	—	—	V	ACTIVE MODE
Switch Threshold Voltage L	SWL	—	—	0.5	V	OFF MODE
Switch Bias Current	SWI	—	22	60	μA	SW=5V
ADJ Bias Voltage	ADJI	—	5	12	μA	ADJ=5V

●**Reference Data (BD3925FP-C)**

Unless otherwise specified, Vcc=13.2V, ADJ=5V, SW=3V, Ta=25°C

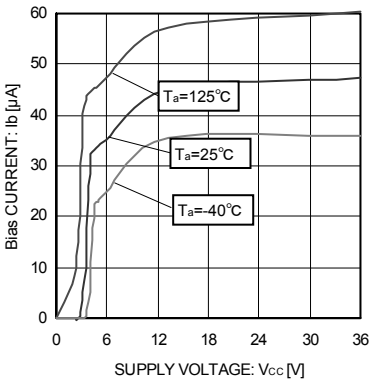


Fig.1 Bias current

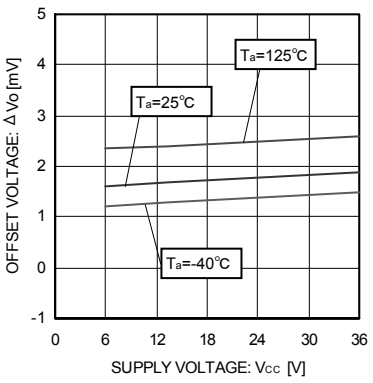


Fig.2 Output voltage vs power supply voltage 1 (Io=5mA)

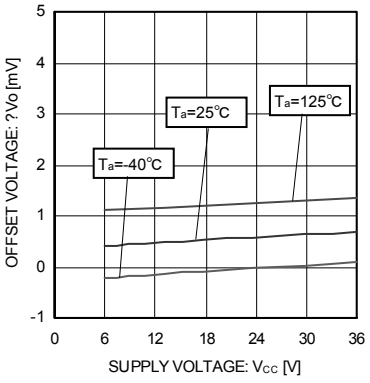


Fig.3 Output voltage vs power supply voltage 2 (Io=200mA)

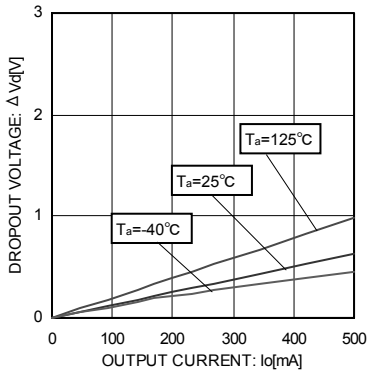


Fig.4 Dropout voltage

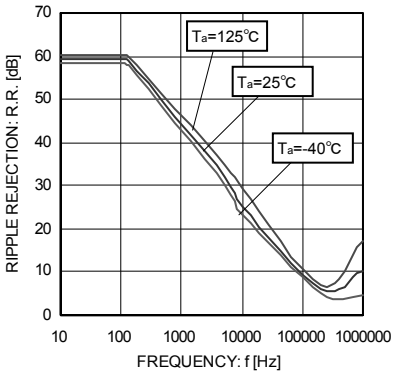


Fig.5 Ripple rejection

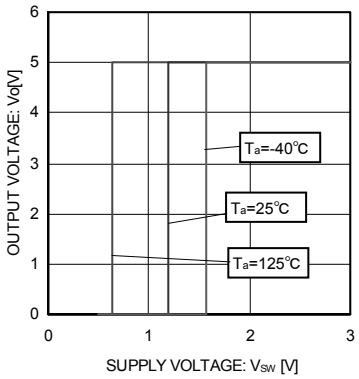


Fig.6 Output voltage vs SW input voltage

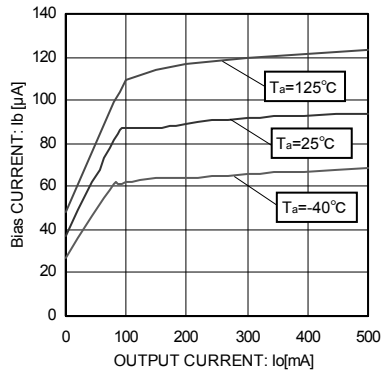


Fig.7 Bias current classified by load

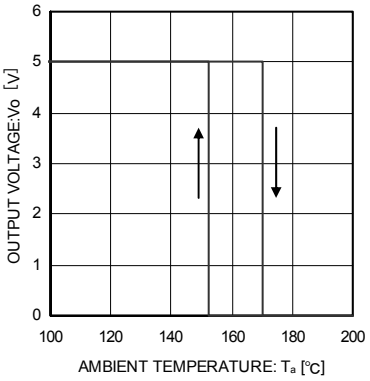


Fig.8. Thermal shutdown circuit

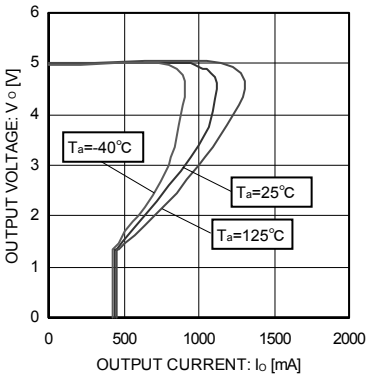


Fig.9 Output voltage vs load

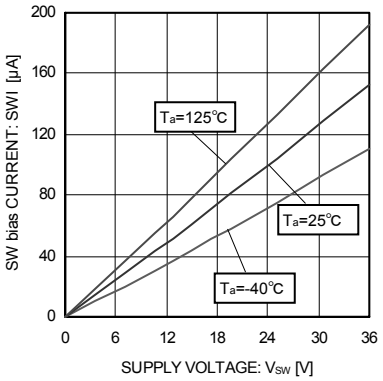


Fig.10 SW bias current

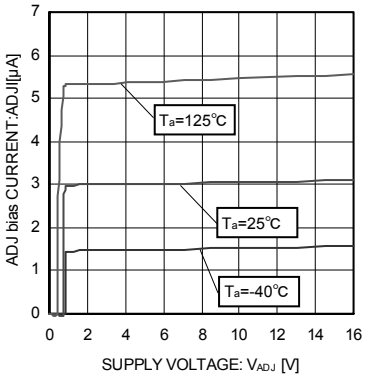


Fig.11 ADJ bias current

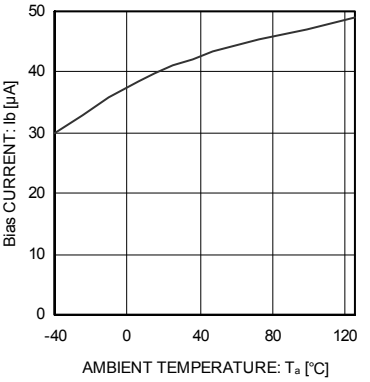


Fig.12 Bias current vs temperature

●**Block Diagram**

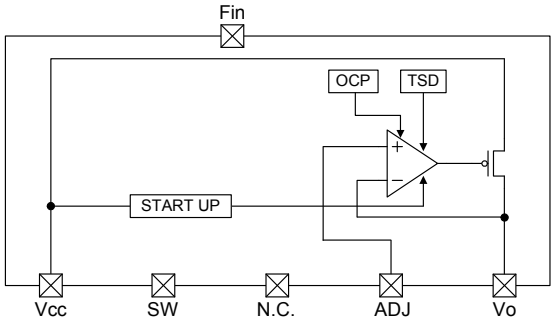


Fig.13 (FP)

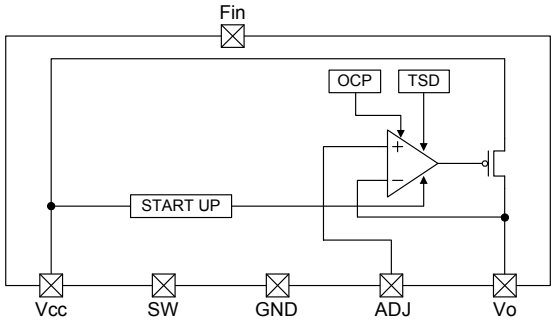


Fig.14 (HFP)

TO252-5

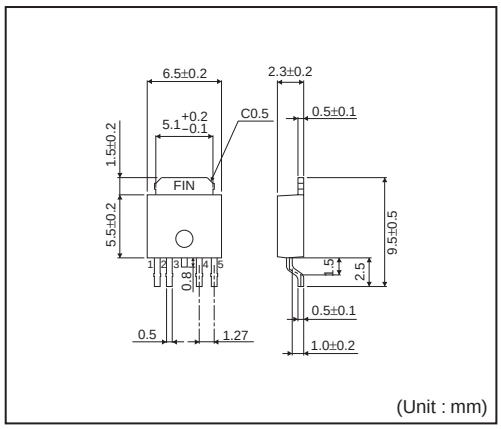
Pin No.	Pin Name	Function
1	Vcc	Power supply pin
2	SW	Vo on/off function pin
3	N.C.	No Connection
4	ADJ	Input voltage
5	Vo	Output Voltage
Fin	GND	Grand

HRP5

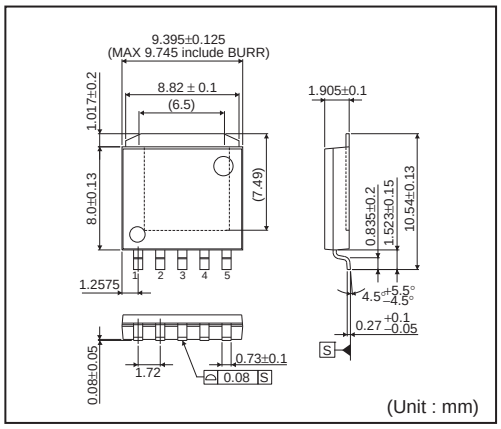
Pin No.	Pin Name	Function
1	Vcc	Power supply pin
2	SW	Vo on/off function pin
3	GND	Grand
4	ADJ	Input voltage
5	Vo	Output Voltage
Fin	GND	Grand

●**Top View** (Package dimension)

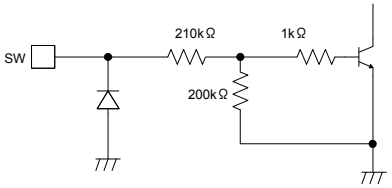
TO252-5



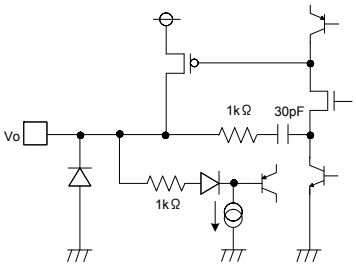
HRP5



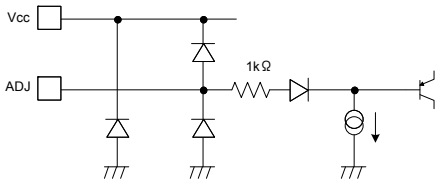
●**I/O equivalence circuit** (All resistance values are typical.)



2PIN[SW]



5PIN[Vo]



1.4PIN[Vcc、ADJ]

●Thermal Dissipation Curve

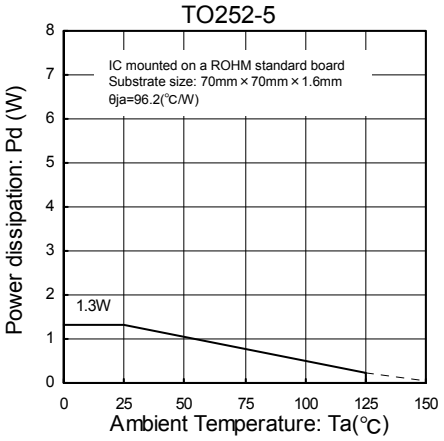


Fig.15

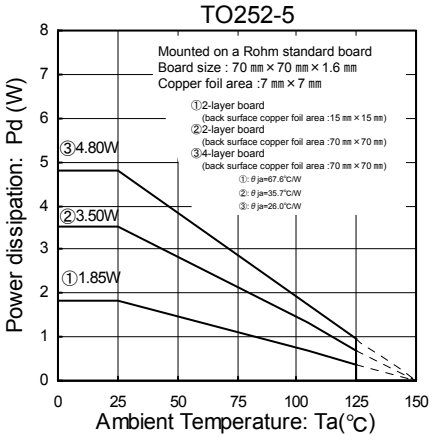


Fig.16

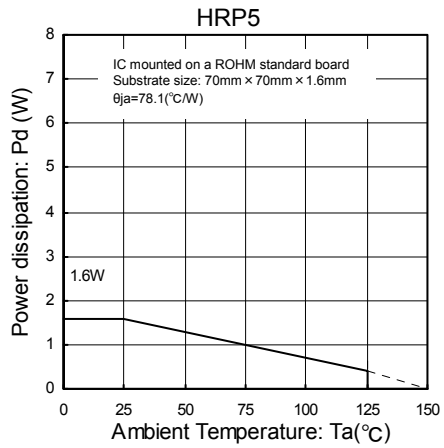


Fig.17

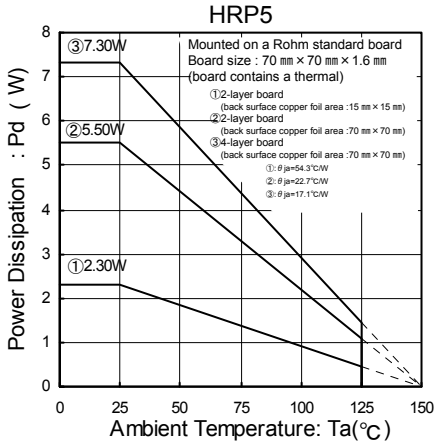


Fig.18

Refer to the heat mitigation characteristics illustrated in Figs. 15 ~ 18 when using the IC in an environment where Ta≧25°C. The characteristics of the IC are greatly influenced by the operating temperature. If the temperature is in excess of the maximum junction temperature Tjmax, the elements of the IC may be deteriorated or damaged. It is necessary to give sufficient consideration to the heat of the IC in view of two points, i.e., the protection of the IC from instantaneous damage and the maintenance of the reliability of the IC in long-time operation.
In order to protect the IC from thermal destruction, it is necessary to operate the IC not in excess of the maximum junction temperature Tjmax. Fig. 15,16 illustrates the power dissipation/heat mitigation characteristics for the TO252 package. Operate the IC within the power dissipation Pd. The following method is used to calculate the power consumption Pc (W).

$Pc=(Vcc-Vo)\times Io+Vcc\times Ib$

Power dissipation $Pd \geqq Pc$

Vcc : Input voltage
Vo : Output voltage
Io : Load current
Ib : Total supply current

The load current IO is obtained to operate the IC within the power dissipation.

$$Io \leqq \frac{Pd - Vcc \times Ib}{Vcc - Vo}$$

(Please refer to Fig.7 and Fig.12 for Ib.)

The maximum load current IOMax for the applied voltage Vcc can be calculated during the thermal design process.

Example)BD3925FP-C Vcc = 12V and Vo=5V(ADJ=5)at Ta = 85°C

$$Io \leqq \frac{0.624 - 12 \times Ib}{12 - 5}$$

(θja=96.2℃/W→-10.4mAW/℃
25℃=1.3W→85℃=0.624W)

Io≦89mA (Ib=100μA)

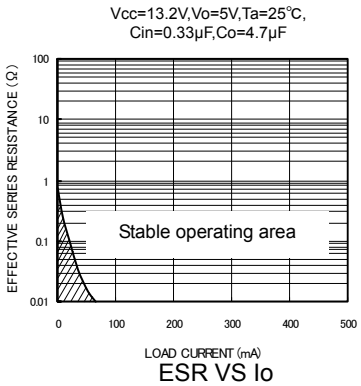
Make a thermal calculation in consideration of the above so that the whole operating temperature range will be within the power dissipation.
The power consumption Pc of the IC in the event of shorting (i.e., if the Vo and GND pins are shorted) will be obtained from the following equation.

$Pc=Vcc\times(Icc+Ishort)$ Ishort = Short current (Please refer to Fig.9 for Ishort.)

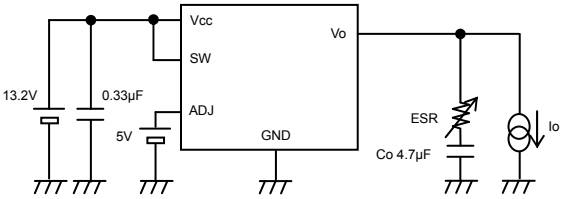
●Pin Settings / Precautions

1. Vcc pins
   Insert capacitors with a capacitance of 0.33μF to 1000μF between the Vcc and GND pins.
   The capacitance varies with the application. Be sure to design the capacitance with a sufficient margin.

2. Output pin
   It is necessary to place capacitors between each output pin and GND to prevent oscillation on the output. Usable capacitance values range from 4.7μF to 1000μF. Ceramic capacitors can be used as long as their ESR value is low enough to prevent oscillation. Abrupt fluctuations in input voltage and load conditions may affect the output voltage. Output capacitance values should be determined only through sufficient testing of the actual application.



ESR VS Io



※Pin Settings / Precautions 2 Measurement circuit

●Notes for use

1. Absolute maximum ratings
   Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2. GND potential
   Ensure a minimum GND pin potential in all operating conditions.

3. Thermal design
   The Power dissipation indicated on this specification is the value without heat sink. Use a thermal design that allows for a sufficient margin by attaching with heat sink in light of the power dissipation (Pd) in actual operating conditions.

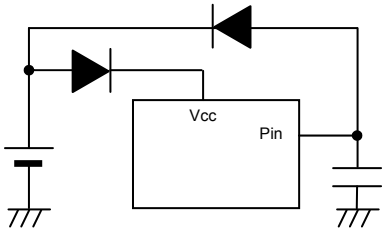
4. Pin short and mistake mounting
   Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC. Ensure a minimum GND pin potential in all operating conditions.

5. Actions in strong magnetic field
   Keep in mind that the IC may malfunction in strong magnetic fields

6. Testing on application boards
   When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC

7. Ground patterns
   When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external parts, either.

8. Applications or inspection processes where the potentials of the Vcc pin and other pins may be reversed from their normal states may cause damage to the IC's internal circuitry or elements. Use an output pin capacitance of 470μF or lower in case Vcc is shorted with the GND pin while the external capacitor is charged. It is recommended to insert a diode for preventing back current flow in series with Vcc or bypass diodes between Vcc and each pin.

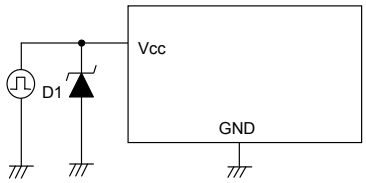


9. SW Pin, ADJ Pin
   Do not apply the voltage to SW pin and ADJ pin when the Vcc is not applied.
   And when the Vcc is applied, the voltage of SW pin and ADJ pin must not exceed Vcc.

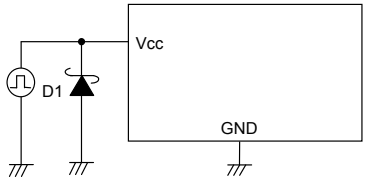
10. Thermal shutdown circuit (TSD)
    This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the junction temperature (Tj) will trigger the TSD circuit to turn off all output power elements(175℃:Typ). The circuit automatically resets once the junction temperature (Tj) drops (150℃:Typ). Operation of the TSD circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.

11. Overcurrent protection circuit (OCP)
    The IC incorporates a built-in overcurrent protection circuit that operates according to the output current capacity.
    This circuit serves to protect the IC from damage when the load is shorted. The protection circuit is designed to limit current flow by not latching in the event of a large and instantaneous current flow originating from a large capacitor or other component. This protection circuits is effective in preventing damage due to sudden and unexpected accidents.
    However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capacity has negative characteristics to temperatures.

12. About positive surge voltage
To protect against a surge voltage that exceeds 50V between Vcc and GND please insert a power zener diode between Vcc terminal and GND.

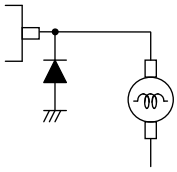


13. About negative surge voltage
To protect against a negative surge voltage, please insert a Schottky diode between the Vcc terminal and GND.



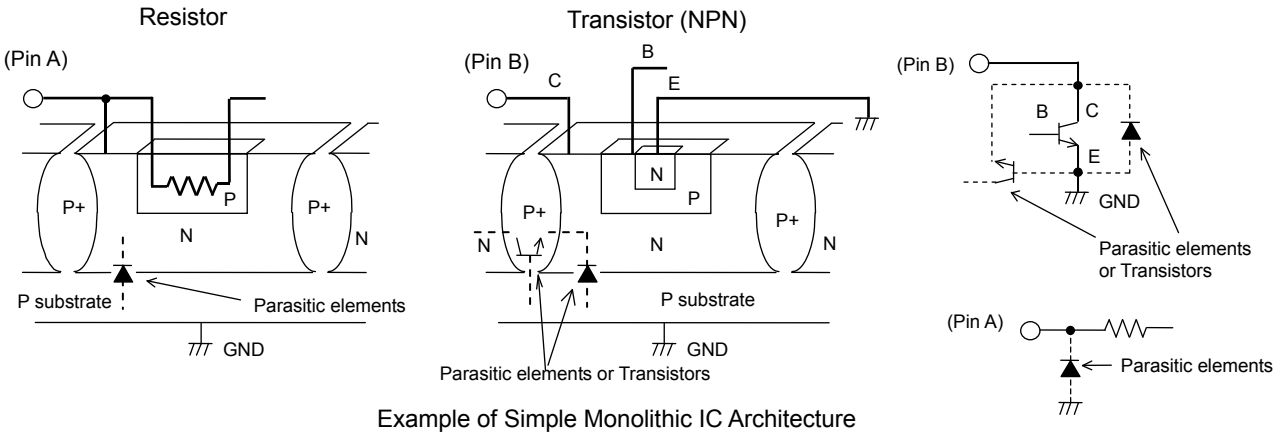
14. For an infinitesimal fluctuations of output voltage
At the use of the application that infinitesimal fluctuations of output voltage caused by some factors (e.g. disturbance noise, input voltage fluctuations, load fluctuations, etc.), please take enough measures to avoid some influence (e.g. insert the filter, etc.).

15. We recommend using Diode for protection purpose when the temperature so output voltage is off.
This is to prevent against large loads of impedance or reverse current during initial stages or output off stage



16. This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements. For example, when the resistors and transistors are connected to the pins as shown in the following figure,
    - ○The P/N junction functions as a parasitic diode when GND > Pin A for the resistor or GND > Pin B for the transistor (NPN).
    - ○Similarly, when GND > Pin B for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (P substrate) voltage to input pins. Keep in mind that the IC may malfunction in strong magnetic fields.,



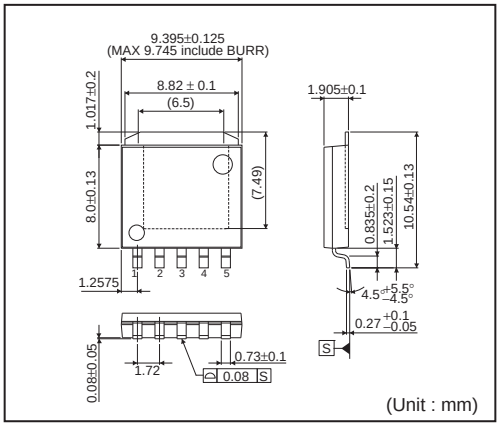
Example of Simple Monolithic IC Architecture

●Part Number Selection

B	D	3	9	2	5	H	F	P	-	C	T	R

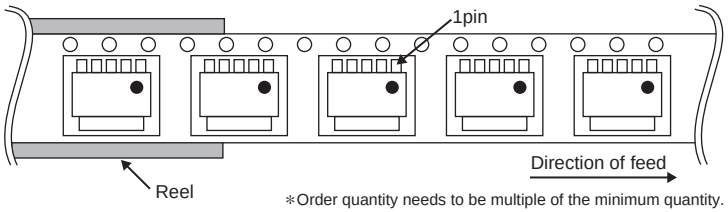
- Part No.
- Part No.
- Package
  HFP :HRP5
  FP :TO252-5
- Packaging and forming specification
  TR: Embossed tape and reel (HRP5)
  E2: Embossed tape and reel (TO252-5)

HRP5



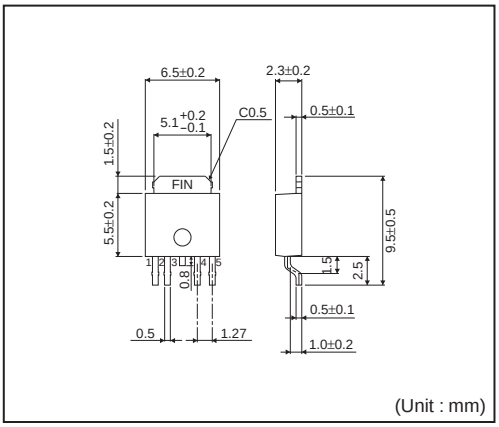
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



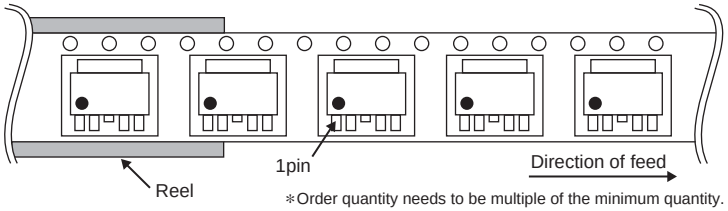
∗Order quantity needs to be multiple of the minimum quantity.

TO252-5



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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