CIRRUS LOGIC

CL-GD6340

Preliminary Data Sheet

FEATURES

- **100% IBM® VGA compatible at the display level**
- **Supports SimulSCAN™ — displays on CRT and LCD simultaneously**
- **Provides full-color VGA on 8- or 512-color TFT (Thin Film Transistor) and other active-matrix or color STN (Super Twist Nematic) LCD panels:**
  - 256 display colors in Mode 13
  - 16 display colors in Mode 12
- **Enhanced color palette**
- **Supports VGA color modes on monochrome LCD panels:**
  - 64 shade grayscale in Mode 13 (direct-multiplexed panels)
  - 16 shade grayscale in Mode 12 (direct-multiplexed panels)
  - Supports Automap™, color-to-grayscale mapping in text and graphics modes
- **Support for monochrome, color TFT active matrix, and color STN LCD panels**
- **On-chip buffers and logic to support monochrome and color active matrix and direct-multiplexed (Passive) LCDs, of both single- and dual-panel construction**
- **Fully integrated and compatible with the existing CL-GD610/620 and CL-GD6410 VGA chipsets, as well as future Cirrus Logic flat panel controllers**

(cont. next page)

Color LCD Interface Controller

OVERVIEW

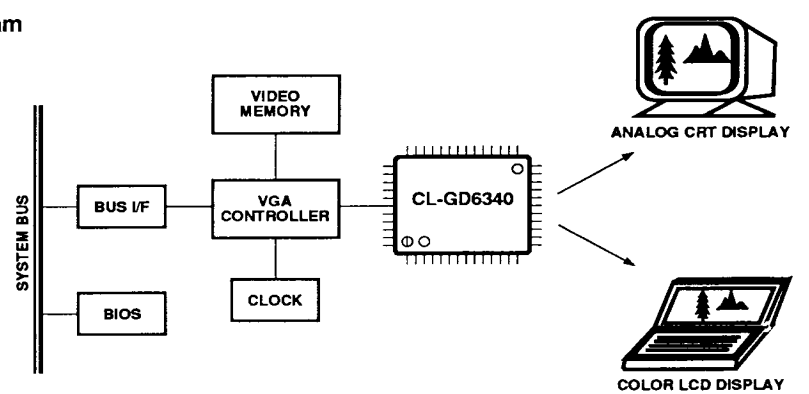
The CL-GD6340 color LCD (Liquid Crystal Display) interface controller provides full-color VGA graphics on LCD panels. By using proprietary techniques for color shading, the CL-GD6340 is able to increase the number of colors that the LCD panel can display. On an eight-color active-matrix LCD panel, a palette of over 4,000 display colors can be generated, from which up to 256 colors can be displayed at one time in VGA Mode 13. On a 512-color active-matrix LCD panel, the number of available colors is over 185,000. The CL-GD6340 also provides a palette of over 226,000-color palette on eight-color STN panels, as well as up to 64 shades of gray on monochrome panels.

The CL-GD6340 integrates the following major functions:

- Shading logic for generating grayscale and color on LCDs,

(cont. next page)

Functional Block Diagram



October 1991

FEATURES (cont.)

- **32 MHz operation for compatibility with high-performance VGA chips**
- **Support for flat panels includes buffers to the panels, STN LCDs with monochrome (single and dual panels) and color (single and dual panels)**
- **Packaged in EIAJ-standard 100-pin plastic Quad Flat Pack (QFP) package**
- **Low-power CMOS construction**
- **Enhanced power management features**
- **Provides power-up/down sequence control to flat panel displays**
- **Programmable grayscale circuits**
- **Integrated CRT RAMDAC compatible with IMS® 171/174 or Brooktree® 471/475**
- **Low chip count solution**

ADVANTAGES

- **Expands the number of display colors**
- **Flexible architecture includes a programmable panel interface with buffers, timing, and power sequencing logic**
- **Provides simultaneous display on analog CRT and digital LCD (SimulSCAN)**
  - CL-GD6340-based portable computers, driving internal and external displays simultaneously, can be used for live presentations
- **Integrates VGA RAMDAC**
- **Provides LCD image quality comparable with that of a CRT in all VGA modes**
- **Thousands of display colors provide subtlety of shading necessary for real-life and three-dimensional images**
- **Supports multiple panels and types; color, monochrome, passive, and active-matrix panels**
- **Provides a highly integrated solution for minimum-form-factor designs**

OVERVIEW (cont.)

- Highly programmable flat-panel interface with buffers, timing, and power sequencing output that enables the use of many different panels from various manufacturers, and
- RAMDAC with RGB color lookup table and digital-to-analog converter

The CL-GD6340 is optimized to provide full VGA graphics on monochrome or color LCD panels. The programmable architecture allows the flexibility to support LCD panels from a large variety of vendors, as well as other display technologies including gas plasma, electro-luminescent, and CRT.

The CL-GD6340 handles subtle gradations of shade and hue, expands the total color (or grayscale) capability of an LCD, and provides a display quality that compares to an analog CRT. With a complete Cirrus Logic color LCD VGA solution, even eight-color panels can support all VGA modes (including Mode 13), displaying 256 colors simultaneously from a palette of thousands. This color range is critical to lifelike, three-dimensional images, and is increasingly important for graphical user interfaces.

The CL-GD6340 can simultaneously drive analog CRTs and digital outputs to LCD panels. Its integrated RAMDAC enables the design of a minimum-size VGA solution, providing unequaled color capacity for the portable and flat panel markets.

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SimulSCAN Operation

SimulSCAN operation, a Cirrus Logic technique for allowing simultaneous CRT and LCD operation, is a feature unique to the Cirrus Logic controllers. SimulSCAN allows the portable computer to become a key part of presentation environments for sales force automation, field service, and educational organizations.

SimulSCAN Functions

- Simultaneous display on internal LCD and external CRT
- Compatible with VGA modes
- Compatible with VGA applications software

SimulSCAN Features

- An external display for audience presentations – fixed frequency or multi-frequency analog CRT
- An internal display for computer operation – single-scan or dual-scan LCD (6.3 MHz panel speed required for dual-scan LCD)
- Reverse intensity (optional) on the internal monochrome display; simultaneous with normal operation of the external display

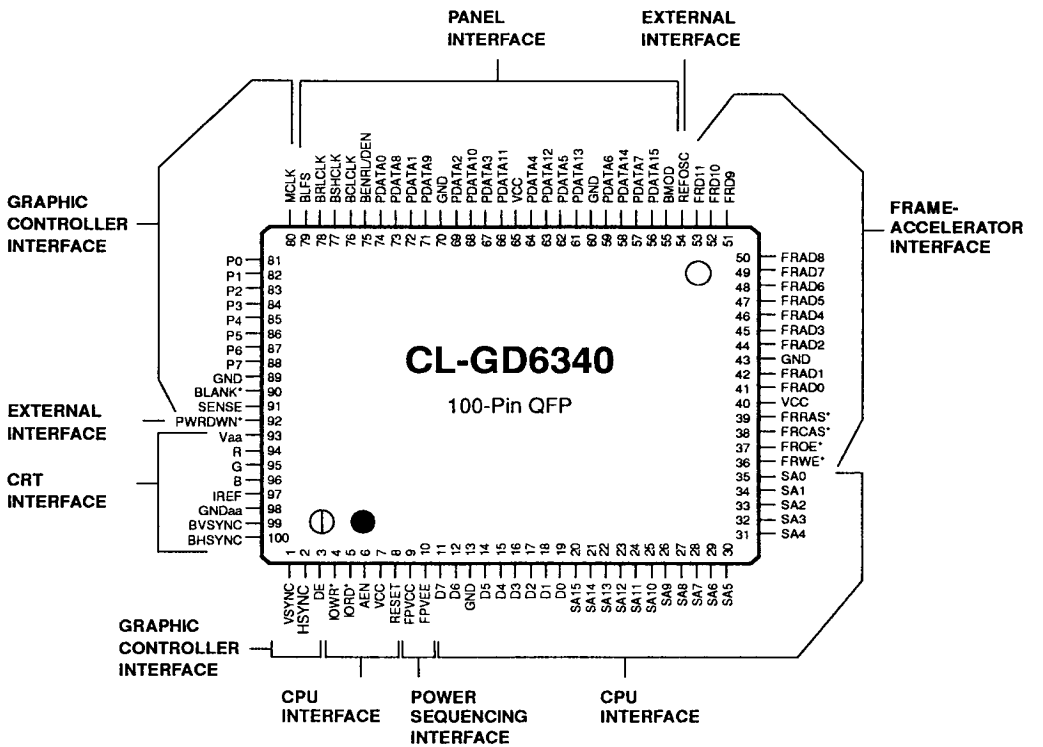
SimulSCAN allows the portable computer to be used in large audience presentation/demonstration environments. With SimulSCAN, the computer provides an analog RGB video signal for overhead projection systems, standard CRTs, or large-screen CRTs, for the audience to view while maintaining operation of the computer's internal LCD display for the computer operator to view.

To achieve SimulSCAN operation, the CL-GD6340 provides separate CRT and LCD display data output paths. Resolution-mapping logic converts the various CRT resolutions to the fixed resolution of the LCD. Clock management logic converts the CRT timing to LCD timing, and CL-GD6340 is able to provide clock signals at different rates to two displays simultaneously. The Frame-Accelerator stores half of the screen image, and effectively re-formats the data path to dual-scan LCDs.

1. PIN INFORMATION

The CL-GD6340 is available in a 100-pin Quad Flat Pack (QFP). The diagram below shows the pinout of this package.

1.1 Pin Diagram



(*) Denotes negative true signal

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Figure 1–1. CL-GD6340 Pin Diagram

1.2 Pin Assignment Table

Symbol	Pin	Type	Description
CPU INTERFACE (28 PINS)			
RESET	8	I	System Reset
SA[15:0]	20-35	I	Latched CPU Address Bus
D[7:0]	11, 12, 14-19	I/O	CPU Data Bus
AEN	6	I	Address Enable for DMA usage only
IORD*	5	I	Read Enable to internal registers
IOWR*	4	I	Write Enable to internal register
EXTERNAL INTERFACE (2 PINS)			
REFOSC	54	I	Oscillator Input must be connected to a clock, usually the 14 MHz system oscillator.
PWRDWN*	92	I	Power-Down Input
GRAPHIC CONTROLLER INTERFACE (14 PINS)			
P[7:0]	81-88	IC	Pixel Data Bits [7:0]
MCLK	80	IC	Master Clock
BLANK*	90	IC	Video Blanking Signal
DE	3	IC	Display Enable
HSYNC	2	IC	Horizontal Sync
VSYNC	1	IC	Vertical Sync
SENSE	91	O	Monitor Sense Output
CRT INTERFACE (8 PINS)			
IREF	97	OA	Current Reference Input. An external current reference must sink 6.7 mA.
Vaa	93	P	Analog Power
GNDaa	98	G	Analog Ground
R, G, B	94-96	OA	Output, high-impedance current source to directly drive a doubly terminated 75 ohm coaxial cable.
BHSYNC	100	TO	Buffered HSYNC for direct connection to an analog monitor.
BVSYNC	99	TO	Buffered VSYNC for direct connection to an analog monitor.
PANEL INTERFACE (24 PINS)			
BLFS	79	TO	Buffered LCD Frame Start
BMOD	55	TO	Buffered MODulation
PDATA[15:0]	56-59, 61-64 66-69, 71-74	TO	Panel Data
BCLCLK	76	TO	Buffered Column Line Clock for TFT/STN Panels
BRLCLK	78	TO	Buffered Row Line Clock for TFT Panels
BENRL/DEN	75	TO	Enable Row Line Clock for TFT or Display Enable
BSHCLK	77	TO	Buffered Shift Clock to Panel Shift Register
FPVCC	9	O	Power Sequence Control Bit 1 (Vcc on)
FPVEE	10	O	Power Sequence Control Bit 0 (Vee on)

1.2 Pin Assignment Table *(cont.)*

Symbol	Pin	Type	Description
FRAME-ACCELERATOR MEMORY INTERFACE (16 PINS)			
FROE*	37	O	Frame-Accelerator Output Enable
FRCAS*	38	O	Frame-Accelerator CAS*
FRRAS*	39	O	Frame-Accelerator RAS*
FRWE*	36	O	Frame-Accelerator Write Enable
FR-AD[8:0]	41, 42,44-50	I/O	Frame-Accelerator Multiplexed Address/Data
FR-D[11:9]	51,52,53	I/O	Frame-Accelerator Upper 3 bits of data for dual-scan color panels
POWER (8 PINS)			
VCC	7, 40, 65	P	3 VCC pads total
GND	13, 43, 60 70, 89	G	5 GND pads total

NOTE:

The following conventions are used in the pin assignment tables:

(*) indicates that a signal is asserted low

(G) = Ground

(IA) = Analog Input

(I/O) = CMOS-Level Input/Output

(O) = CMOS-Level Output

(P) = Power

(TO) = CMOS Output

(I) = TTL-Level Input

(IC) = CMOS-Level Input

(OA) = Analog Output

2. DETAILED PIN DESCRIPTION

The following conventions are used in the pin assignment tables: (*) indicates that a signal is asserted low; (03) indicates Tri-state; (G) indicates Ground; (I) indicates TTL-Level Input; (IA) indicates Analog Input; (IC) indicates CMOS-Level Input; (I/O) indicates TTL-Level Input/Output; (O) indicates CMOS-Level Output; (OA) indicates Analog Output; (O) indicates TTL-Level Output and (P) indicates Power.

2.1 CPU Interface (28 pins)

Symbol	Pin	Type	Description
RESET	8	I	**System Reset:** This input is normally connected to the System Reset Bus Signal and is used as a hardware reset.
SA[15:0]	20-35	I	**Latched CPU System Address Bus:** Demultiplexed address bus for direct connection between the CPU and the CL-GD6340 for video RAM addresses and I/O register addresses.
D[7:0]	11, 12, 14-19	I/O	**CPU Data Bus:** Data Bus between the CPU and the chip for video RAM addresses, I/O register addresses, and data. In CL-GD610/620-controller-based systems, these pins are connected to the controller side of the Multiplexed Address/Data Bus buffers. In CL-GD6410-based systems, these pins are either connected to the controller side of the data buffers (if any) or directly to the system data bus. (if there are less than four ISA Bus slots)
AEN	6	I	**Address Enable for DMA Usage Only:** Host CPU bus signal that distinguishes between DMA and non-DMA bus cycles. The signal is high for a DMA Cycle.
IORD*	5	I	**Input/Output Read Enable to Internal Registers:** When low, this signal indicates that an IORD* Cycle is taking place. The CL-GD6340 will respond only if proper I/O port addresses have been decoded, and AEN is low.
IOWR*	4	I	**Input/Output Write Enable to Internal Register:** When low, this signal indicates that an IOWR* Cycle is taking place. The CL-GD6340 will respond only if proper I/O port addresses have been decoded, and AEN is low.

2.2 External Interface (2 pins)

Symbol	Pin	Type	Description
REFOSC	54	I	**Oscillator Input:** This signal is used to control the timing of the CL-GD6340 power sequencing circuitry. This input must be connected to a continuously running clock, usually the 14 MHz system oscillator. (MIN = 5 MHz, MAX = 14.318 MHz)
PWRDWN*	92	I	**Power-Down Input:** When this pin is asserted low, the CL-GD6340 goes into Suspend Mode.

2.3 Graphic Controller Interface (14 pins)

Symbol	Pin	Type	Description
P[7:0]	81-88	IC	**Pixel Data Bits [7:0]:** Input from the VGA controller.
MCLK	80	IC	**Master Clock:** This is the display (pixel) clock from the VGA controller.
BLANK*	90	IC	**Video Blanking Signal:** When this signal is high, display on screen is enabled. When low, screen is blanked.
DE	3	IC	**Display Enable:** When this signal is high, it indicates valid display data. This signal is low during overscan or retrace and pulses high for each line of non-displayed data.
HSYNC	2	IC	**Horizontal Sync:** Horizontal Sync Input.
VSYNC	1	IC	**Vertical Sync:** Vertical Sync Input.
SENSE	91	O	**Monitor Sense Output:** IBM-standard analog SENSE output to the VGA controller. This signal is used for detecting monitor type and presence.

2.4 CRT Interface (8 pins)

Symbol	Pin	Type	Description
IREF	97	OA	**RAMDAC Current Reference Input:** An external current reference must sink 6.7 mA.
Vaa	93	P	**RAMDAC Analog Power Input**
GNDaa	98	G	**RAMDAC Analog Ground Input**
R,G,B	94-96	OA	**Analog Red, Analog Green, and Analog Blue:** High-impedance PS/2-compatible current source to directly drive a doubly terminated 75 ohm coaxial cable.
BHSYNC	100	TO	**Buffered Horizontal Sync:** For direct connection to an analog monitor. The active polarity of this signal can be selected by Bit 6 of the Miscellaneous Output Register (I/O address 3C2H), or Bit 6 of the Timing Control Register (ER85).
BVSYNC	99	TO	**Buffered Vertical Sync:** For direct connection to an analog monitor. The active polarity of this signal can be selected by Bit 7 of the Miscellaneous Output Register (I/O address 3C2H), or Bit 7 of the Timing Control Register (ER85).

2.5 Panel Interface (24 pins)

Symbol	Pin	Type	Description
BLFS	79	TO	**Buffered LCD Frame Start:** LCD frame start pulse indicates the start of a new frame, reset of horizontal and vertical logic to the first nibble of the first (of top and bottom panel) scanline.
BMOD	55	TO	**Buffered MOD:** Buffered Modulation (AC Inversion) is used to prevent DC polarization of LCD panels. The BMOD period is programmable. See ERD9 for details.
PDATA[15:0]	56-59, 61-64, 66-69, 71-74	TO	**Panel Data:** Video data output for direct connection to LCD panels.
BCLCLK	76	TO	**Buffered Column Line Clock for TFT and STN panels:** LCD column clock used to load column drivers with horizontal shift register data.
BRLCLK	78	TO	**Buffered Row Line Clock for TFT panels**
BENRL/DEN	75	TO	**Enable Row Line Clock for TFT panels or Display Enable**
BSHCLK	77	TO	**Buffered Shift Clock to Panel Shift Register:** LCD line clock used to latch column segment data into the horizontal shift registers.
FPVCC	9	O	**Power Sequence Control Bit 1 (Vcc on):** TTL-level output to control flat panel logic voltage.
FPVEE	10	O	**Power Sequence Control Bit 0 (Vee on):** TTL-level output to control flat panel back-light power and contrast voltage.

2.6 Frame-Accelerator Memory Interface (16 pins)

Symbol	Pin	Type	Description
FROE*	37	OC	**Frame-Accelerator Output Enable**
FRCAS*	38	OC	**Frame-Accelerator CAS***
FRRAS*	39	OC	**Frame-Accelerator RAS***
FRWE*	36	OC	**Frame-Accelerator Write Enable**
FRAD[8:0]	41, 42, 44-50	I/O	**Multiplexed Frame-Accelerator Address/Data**
FRD[11:9]	51-53	I/O	Upper three bits of data for color modes.

2.7 Power (8 pins)

Symbol	Pin	Type	Description
VCC	7, 40, 65	P	Three VCC pads, total.
GND	13, 43, 60, 70, 89	G	Five GND pads, total.

3. FUNCTIONAL DESCRIPTION

The data path in the CL-GD6340 operates as follows:

1) **The Input P[7:0] is used to address the RAMDAC,**
2) **RAMDAC color values are modified by Stippling and Sum-to-Gray Logic, and**
3) **Output is then either stored into the Frame-Accelerator or sent to the Panel Interface Logic, which bit shuffles the data according to panel type.**

The following sections discuss each item in detail.

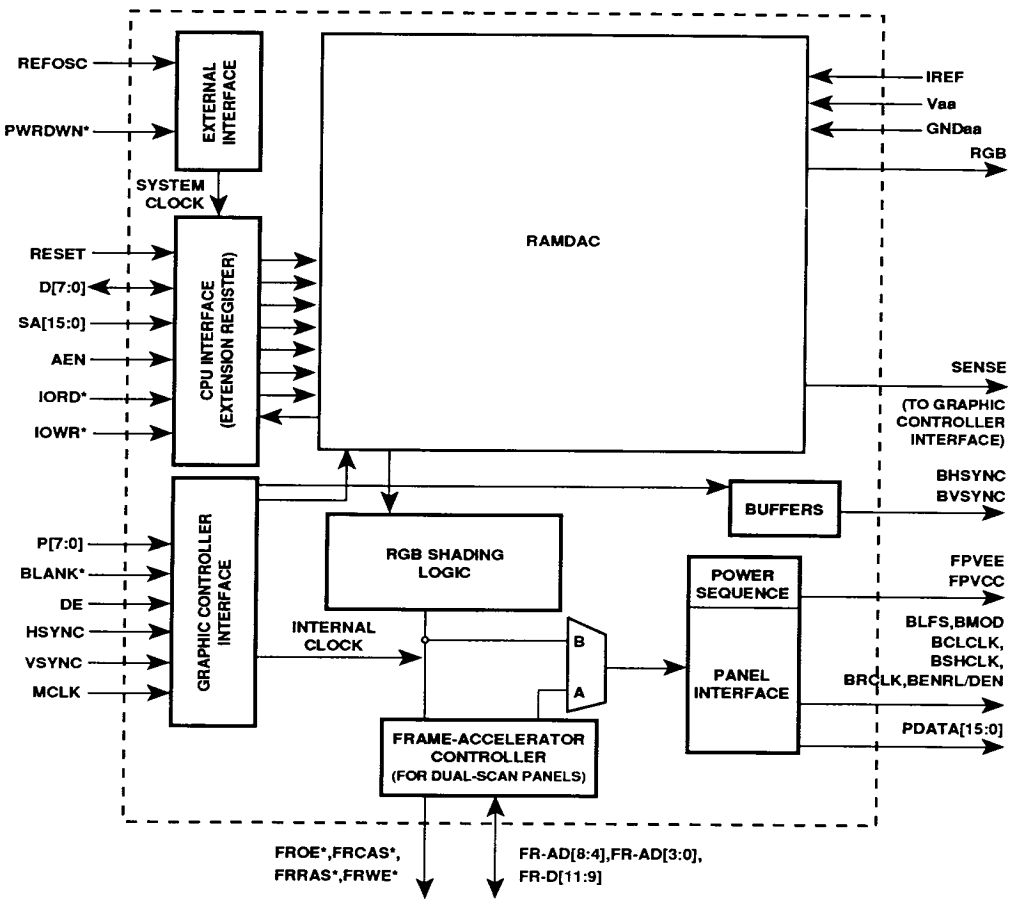

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Figure 3–1. CL-GD6340 Block Diagram

3.1 CPU Interface

The CPU Interface connects the CL-GD6340 to the PC AT bus. The CPU Interface contains the signals (IORD*, IOWR*, AEN, SA[15:0], and Reset) required to latch information from the bus and ignore DMA transfers. The Reset Signal resets all the registers, except scratch registers, to a known default state. In addition to the above signals, a multiplexed Address/Data Bus is also needed.

There are two types of registers in the CL-GD6340: indexed and non-indexed. To read or write a non-indexed register, an I/O Read or I/O Write is sufficient. The CL-GD6340 decodes the address bits A[15:0] along with the IORD* or IOWR* to determine which register is to be accessed, and the direction of the data transfer.

An indexed addressing scheme is used to control access to the CL-GD6340 extension registers. In order to read or write an extension register, the desired register's index must first be written to the Extensions Index Register (ERX) with an I/O Write. Upon the next I/O Operation, the CL-GD6340 decodes the address bits A[15:0] along with IORD* and IOWR* to determine which register is to be accessed and which operation will be performed. If the selected register is an Extension Register, the Extensions Index Register (ERX) is used as an index into the Extension Register set.

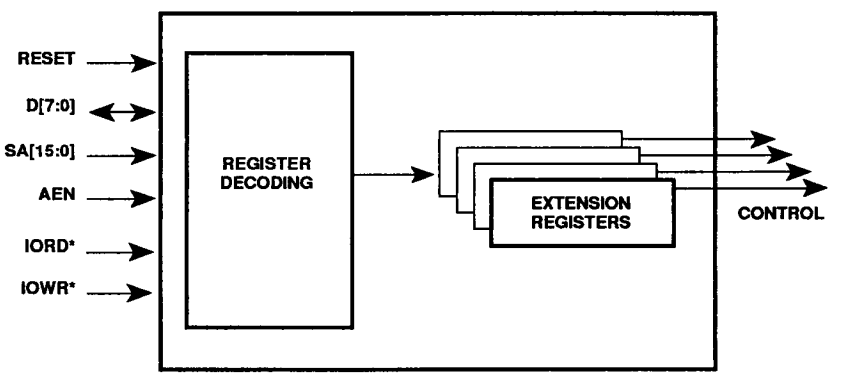

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Figure 3–2. CPU Interface

3.2 Graphic Controller Interface

The data path is from P[7:0] through the 256 x 18 RAM. This RAM Output is then passed through the DAC (to generate RGB signals) as well as the grayscale logic. During PWRDN* by External Pin, the R, G, and B signals become 'black', and BHSYNC and BVSYNC become tri-stated.

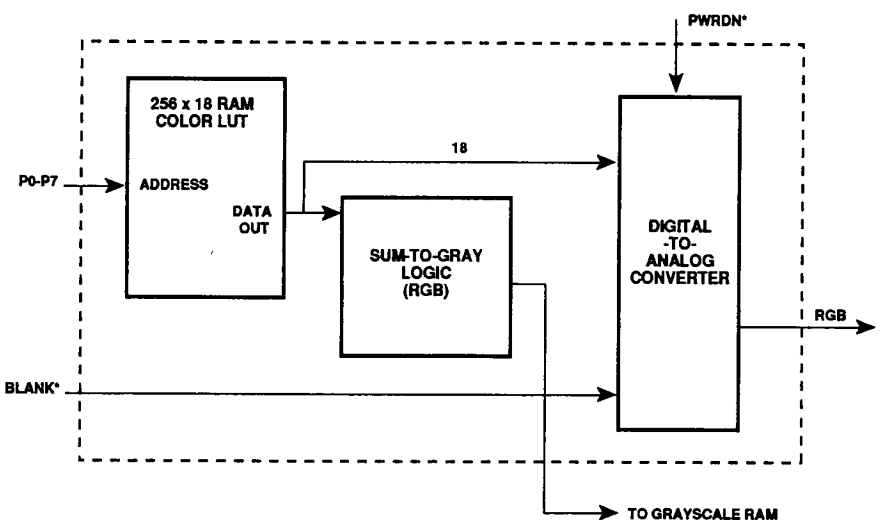

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Figure 3–3. Graphics Controller Interface

3.3 Frame-Accelerator Controller

The CL-GD6340 includes a proprietary Frame-Accelerator to allow the VGA controller to function at half the clock rate of other controllers for a given refresh rate. The Frame-Accelerator allows the CL-GD6340 to take advantage of a dual-panel LCD configuration to refresh the entire display in half the time a screen refresh would normally take. The CL-GD6340 sends frame data to one half of the display and to Frame-Accelerator. As new data is stored in the Frame-Accelerator, the previous data is used to update the other half of the display. The Frame-Accelerator and the CL-GD6340 then switch display and accelerator responsibilities. This occurs continuously and allows faster screen refresh with power dissipated by the system.

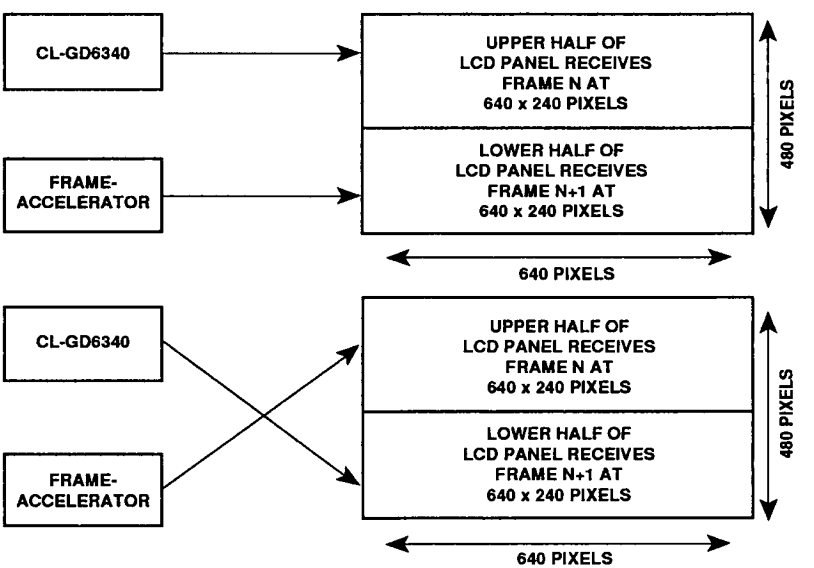

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Figure 3–4. Frame-Accelerator Block Diagram

The Frame-Accelerator memory must have 64K addressable locations with a width equal to four times the number of data bits associated with each pixel write cycle. Most monochrome applications require 4-bit-wide memory: one bit per pixel multiplied by four write cycles. In 8-color applications, 12 bits are needed to support four pixel writes of three data bits each (Red, Green, and Blue). Using one 64K x 16 DRAM (64K x 4 is sufficient if only monochrome dual-scan panels are to be supported) is one way to achieve a versatile solution.

The Frame-Accelerator DRAM(s) must be the same speed as Video Memory and is connected directly to the CL-GD6340 with no intervening circuitry. The Frame-Accelerator memory must support the following:

- **Page Mode**
- **CAS precharge time of 25 ns or less**
- **CAS-before-RAS refresh**
- **RAS low time greater than the horizontal display period (see example, below)**

Worst-Case Example: Three MHz pixel clock (BSHCLK), where the RAS (FFRAS*) will be low for a period of 67 µsec, which is the entire LCD line display time.

RAS-low required = (Shift Clock Period)* [(Pixels per line/Pixels per clock) +1]
= 333 ns * [(800/4) +1]
= 333 ns * 201
= 67 µs

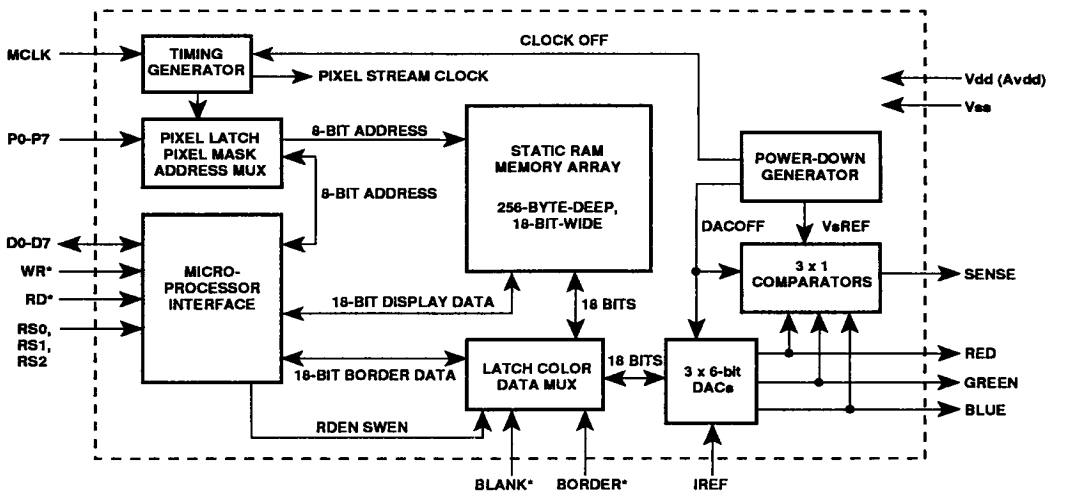
3.3.1 VGA/Panel Frame-Accelerator DRAM Combinations

Panel Type	Panel Operation	Number of DRAMs
Monochrome	– Dual-Panel, Dual-Drive*	One 64K x 4
	– Single-Panel, Single-Drive	NONE
Color (Non-active)	– Dual-Panel, Dual-Drive	One 64K x 16 or three 64K x 4
	– Single-Panel, Single-Drive*	NONE
Color (Active matrix)	– Single-Panel, Single-Drive*	NONE

NOTE: (*) indicates that the majority of system integrators use this panel.

3.4 RAMDAC

The CL-GD6340 internal RAMDAC consists of a 256 x 18 RAM with three 6-bit DAC output channels. The read and write operations involving the RAMDAC are compatible with IBM VGA Palette Memory. The registers are accessed by the CPU through I/O Read/Write instructions. The RAM Register is the data register that is also accessed by I/O Read/Write instructions.



NOTE: This diagram shows the RAMDAC as an external device. Not all signals shown are available externally in the CL-GD6340.

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Figure 3–5. RAMDAC Block Diagram

The CL-GD6340 includes an on-chip, high-speed memory with a Digital-to-Analog Converter (RAMDAC). The RAMDAC circuitry processes the video data from the VGA controller and converts it into PS/2-compatible analog signals.

An 8-bit address value applied on the Pixel Address input defines the memory location for reading an 18-bit color data word from the color lookup table. This data is partitioned as three fields of six bits each, which is applied to the individual DAC inputs.

A pixel word mask is incorporated to allow the incoming Pixel Address to be altered or masked, permitting changes to the color lookup table contents to be made immediately. This feature allows special display operations such as flashing objects and overlays to be created.

The color lookup table contents are accessed via its 8-bit-wide host interface. An internal synchronizing circuit allows the RAMDAC memory contents to be accessed during active video time without flicker.

RAMDAC Video Operation

In video operation, pixel addresses P0 through P7, and BLANK* are sampled on the rising edge of the pixel clock (MCLK). Their effect appears at the DAC outputs after three further rising edges of MCLK.

BLANK* is an active-low signal. When the BLANK* input is low, a binary '0' is applied to the DAC inputs, producing a zero-volt DAC output.

To put the DAC into a power-down state, any one of the following conditions must be true:

Suspend	= ERA7[4]	= 1
Standby	= ER8A[7]	= 1
CRT (off)	= ERF6[3]	= 0
PWRDWN*	= External Pin	= 0

When any of the above conditions is true, the DACs in the RAMDAC are totally inoperative. During this time, the three DAC channels output zero volts, which results in the power dissipation being reduced to the Standby Mode minimum. When the above conditions become false, several MCLK cycles are required before the DACs in the RAMDAC will function properly.

Analog Outputs

The DAC outputs are designed to produce 0.7 volt peak amplitude with a reference current (I_{REF}) of 6.7 mA when driving a doubly terminated 75 ohm load, which corresponds to an effective DAC output load of 37.5 ohms ($R_{effective}$).

Writing to the Color Lookup Table

To write a color definition to the lookup table, a value specifying an address location in the lookup table is first written to PELWR. The color values for the red, green, and blue intensities are then written in succession to PELDATA. After the blue data is latched, and to cause PELWR to automatically increment, this new color data is then written into the lookup table at the defined address.

Since PELWR increments after each transfer of data to the lookup table, it is best to write a set of consecutive locations with new color data. The start address of the set of locations is first written to the Write Address Mode Register. When the write is complete, the color data for each address location is then sequentially written to PELDATA. The RAMDAC automatically writes data to the lookup table and increments PELWR after each host transfer of three bytes of color data.

Reading from the Color Lookup Table

To read color data from the lookup table, a value specifying the address location of the data is written to PELRD. After the address is latched, the data from this location is automatically read out to the PELDATA, and PELRD automatically increments.

Color intensity values can then be read from the PELDATA by a sequence of three I/O Read (IORD*) commands: in sequence, Red, Green, then Blue. After the Blue value is transferred out, PELRD is automatically incremented and new data is read from the lookup table from the new address and placed in PELDATA.

Resetting Color Lookup Table Reads and Writes

If the PELWR is loaded with a new starting address while an unfinished read or write sequence is in progress, the RAMDAC aborts the current sequence and starts a new one.

3.5 Analog Monitor Sense

The CL-GD6340 contains an onboard comparator that detects the voltages of the Red, Green, and Blue outputs. This comparator takes the RGB voltages from the internal DAC and compares them to a reference voltage. The result of this comparison is then placed on the SENSE output pin.

NOTE: SENSE is output only when reading address 3C2 and ERF6[5]*(Disable Sense)* = 0 and the DAC is not in Power-down Mode.

3.6 Panel Power Sequencing

To power-up any panel, certain signals must be presented in a specific order. The Panel Active Sequence is as follows:

a. **Logic power**
b. **Signals**
c. **Panel drivers and backlight**

NOTE: The Panel Inactive Sequence is the reverse.

Two pins are assigned to facilitate power management: FPVCC and FPVEE. These output pins from the CL-GD6340 are TTL-level outputs that are sequenced properly for LCD panels. They are intended to be used to control panel logic power, backlight and contrast voltages.

NOTE: Because the CL-GD6340 is unable to provide the high current and various voltages necessary to drive LCD panels, these outputs are intended to be used as control signals for power circuitry.

The signal FPVCC is intended to be used to activate circuitry that supplies power to the desired panel logic. The signal FPVEE is used to activate circuitry that supplies the desired contrast voltage to the panel. The following diagram shows how FPVCC is always high before and after FPVEE changes state.

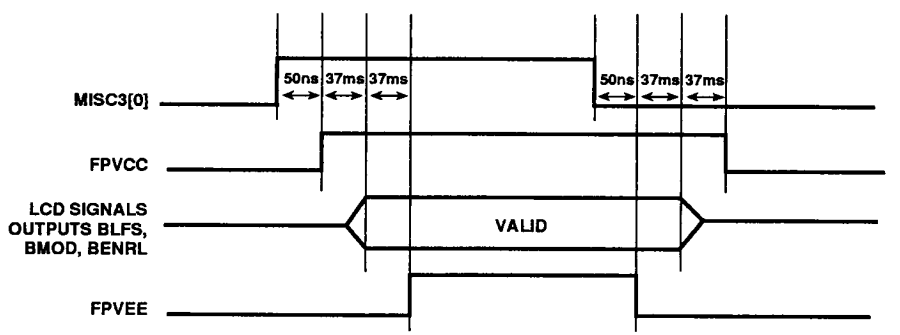

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Figure 3–6. Sequencing for Power and Signals

3.6.1 Panel Inactive Sequence

To shut the panel off, write '0' to MISC3[0].

The CL-GD6340 then performs the following operations:

a. Approximately 50 ns delay
b. FPVEE transitions to a '0'
c. Approximately 37 ms delay
d. LCD signals become tri-state
e. Approximately 37 ms delay
f. FPVCC transitions to a '0'

3.6.2 Panel Active Sequence

The power-on sequence is the reverse order of the Panel Inactive Sequence shown above.

To turn the panel on, write '1' to MISC3[0].

The CL-GD6340 then performs the following operations:

a. Approximately 50 ns delay
b. FPVCC transitions to a '1'
c. Approximately 37 ms delay
d. LCD signals become active
e. Approximately 37 ms delay
f. FPVEE transitions to a '1'

3.7 CRT Sequence Control

MISC3[1] is used to directly control the CRT. When MISC3[1] is a '0', BHSYNC and BVSYNC are tri-stated and RGB is blanked. When MISC3[1] is a '1', BHSYNC, BVSYNC, and RGB are output.

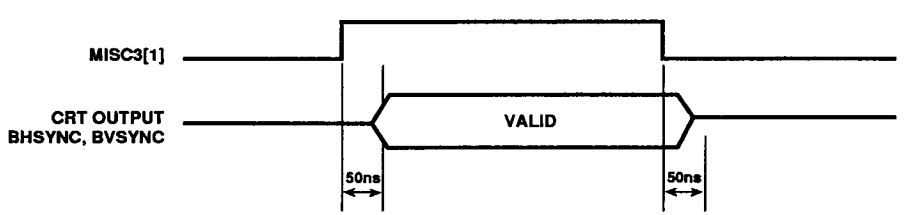

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Figure 3–7. Sequencing for Power and Signals *(cont.)*

3.8 Power-Down Modes

The CL-GD6340 has multiple modes for enhanced power management. Following is a description of the various modes and their effect on the graphics subsystem.

Table 3–1. Power-Down Modes

MODES	Internal Clocks	RAMDAC Palette R/W	DAC	CPU I/F	Panel I/F	Frame Accel.	CRT I/F
Standby Mode ER8A[7]	OFF 1*	ON	ON 1*	ON	3*	4*	3*
Suspend Mode ERA7[4]	OFF	OFF	OFF	OFF	3*	4*	3*
PWRDWN* External Pin = '0'	OFF	OFF	OFF	OFF	OFF 2*	OFF 2*	OFF 2*

NOTES:

This table shows conditions of the CL-GD6340 in each mode only, not in multiple modes.

1) MCLK is shut off internally and is supplied to RAMDAC only during RAMDAC I/O reads and writes.
2) The outputs are driven to zeroes.
3) Remains in previous state, determined by, ERF6[3:2] and ERA7[1:0].
4) If ERF2[6] (dual-scan panel) is set, this remains in previous state, determined by ERF6[2], otherwise off.

To insure the panel is not damaged and minimum power consumption in all of the above modes, the panel and CRT must be sequenced off with ERA7[1:0], SENSE must be disabled with ERF6[5], and the display type select bits ERF6[3:2] should be set to zero PRIOR to entering any power-down modes.

Entering power-down modes is accomplished by writing the correct values into Power-down Register Bits ER8A[7] or ERA7[4] or pulling the PWRDWN* pin down.

Exiting power down modes is accomplished by writing the appropriate values into the register bits ER8A[7] or ERA7[4] or pulling the PWRDWN* pin up. The states of ERA7[1:0] and ERF6[3:2] should be restored upon exit from power-down modes.

3.8.0.1 External Pin Power-Down Sequence

This mode is activated by forcing the PWRDWN* Pin to '0'. This causes the CL-GD6340 to ignore any CPU access and internally forces MCLK = 1 in less than 100 ns.

NOTE: To prevent panel damage, the LCD panel MUST have been power-sequenced 'off' prior to 'PWRDWN* = 0'.

Upon forcing the PWRDWN* Pin to '0', the CL-GD6340 then causes the following to occur:

- **Panel Interface outputs are forced to '0'**
- **Frame-Accelerator outputs are forced to '0'**
- **FPVEE, FPVCC stays in previously programmed state until ERA7[0] changes state from '1' to '0'**
- **CRT Interface outputs BHSYNC, BVSYNC, R, G, B = '0'**
- **SENSE outputs a '0'**

NOTE: Holding the Frame-Accelerator outputs low will allow the Accelerator DRAM to be totally powered-off with no resultant latchup problems or leakage current conducting through the forward-biased CMOS input protection diodes.

3.8.0.2 External Power-Up Sequence

This causes the CL-GD6340 to resume operation in less than 100 ns. Activated by PWRDWN* = '1'.

The CL-GD6340 then performs the following operations:

- **MCLK Input into the CL-GD6340 is enabled**
- **Enables Frame-Accelerator**
- **Enables CRT Interface**
- **Enables Sense**

NOTE: Power Sequencing is unaffected by the PWRDWN* Pin. The display MUST be sequenced-off before power-down and sequenced-on after power-up.

For more details as to the function of specific display control bits, see ERF6[3:2] and ERA7[1:0].

For more details as to the function of specific power-down bits, see ER8A[7] or ERA7[4].

3.9 Sleep Mode

The CL-GD6340 responds to the sleep port at I/O location 3C3 or 46E8 depending on ERF6[7]. In either case, ER87[6] (Arm Video Subsystem) must be a '1' for the CL-GD6340 to go into Sleep Mode via the selected sleep port.

Sleep Mode shuts off CPU access (IORD and IOWR) to the CL-GD6340 registers. However, the active sleep register itself can always be written to. During reading of the sleep registers, only the selected sleep register can be read back.

The selection between the two above is determined by ERF6[7]. If set then 46E8 Register is selected as the sleep register. If reset, then 3C3 is selected as the sleep register.

Table 3–2. Sleep Mode

Modes ERF6 3: 2		LCD Display	CRT Display	MCLK	Panel Clock	RAMDAC Palette R/W	DAC	CPU I/F	Frame Accelerator
0	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
0	1	ON	OFF	ON	ON	OFF	OFF	OFF	1
1	0	OFF	ON	ON	OFF	OFF	ON	OFF	1
1	1	ON	ON	ON	ON	OFF	ON	OFF	1

NOTES:

1) On only if ERF2[6] = 1 and ERF6[2] output zeroes if ERF2[6] = 0.

2) If On (ERF2[6] = '1', dual-scan panel) then it is not toggling due to no MCLK; otherwise, Off.

4. VGA/EGA REGISTER TABLE

The CL-GD6340 maintains a copy of the following bits contained within standard IBM VGA registers. These bits are needed by the CL-GD6340, therefore the BIOS keeps them updated. For the function of these specific bits, please refer to the *CL-GD610/620-C Technical Reference Manual.*

Abbreviations	Register Name	Port	Index	Bits
AR10	Attribute Controller Mode Control (Pixel Doubling Clock Select)	3C0 (3C1)	10	6 and 0
CR9	CRTC Character Cell Height Register (Scanline Doubling)	3?5	09	7 and 4-0
SR1 MODE	Sequencer Clocking Mode Register CMGA Mode Register	3C5 3?8	01	3 and 0 4
GR5	Graphics Controller Mode Register Motherboard Sleep Register Adapter Sleep Register	3CF 3C3 46E8	05	6 0 3
MISC	Miscellaneous Output Register	3C2(W) 3CC(R)		7, 6, and 0

NOTE: ? = 'D' hex for color and 'B' for monochrome.

5. RAMDAC I/O PORT SUMMARY TABLE

The CL-GD6340 contains an on-chip, high-speed, VGA-compatible RAMDAC. The following table provides a summary of each register associated with RAMDAC operation and function; see the referenced pages for complete register descriptions. See Section 3.4 for a more complete description of RAMDAC functions.

Port Address	Abbreviation	VGA/EGA Port	ERF6[6]	Access	Page
03C6	PELMSK	RAMDAC Pixel Mask	0	R/W	28
		RESERVED	1		
03C7	PELRD	RAMDAC Pixel Read Address	0	W	29
		RESERVED	1		
03C8	PELWR	RAMDAC Pixel Write Address	0	R/W	30
	BDRCOL	Border Color	1	R/W	31
03C9	PELDATA	RAMDAC Pixel Data	0	R/W	32
		RESERVED	1		

5.1 RAMDAC Pixel Mask: PELMSK

I/O Port Address: 3C6 (R/W)
ERF6[6] = '0'
Read Protection Bit: EREC[3]

Bit	Description	Access	Reset State
7(MSB)	Pixel Mask Bit 7	R/W	x
6	Pixel Mask Bit 6	R/W	x
5	Pixel Mask Bit 5	R/W	x
4	Pixel Mask Bit 4	R/W	x
3	Pixel Mask Bit 3	R/W	x
2	Pixel Mask Bit 2	R/W	x
1	Pixel Mask Bit 1	R/W	x
0	Pixel Mask Bit 0	R/W	x

Bit 7-0 **Pixel Mask Bits:** This register is initialized to FFh by the BIOS when a new video mode is selected. The Pixel Mask Register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs P[7:0]. A '1' in any position in the Pixel Mask Register leaves that corresponding bit in the Pixel Address unaltered. A '0' in any position in the Pixel Mask Register sets that bit to zero. The Pixel Mask Register does not affect the address generated by the microprocessor interface when the LUT is being read.

NOTE: ERF6[6] must be '1' to access this register. When ERF6[6] = '0', this register is RESERVED.

5.2 RAMDAC Pixel Read Address: PELRD

I/O Port Address: 3C7 (W)

ERF6[6] = '0'

Bit	Description	Access	Reset State
7(MSB)	Pixel Data Register Read Address Bit 7	W	x
6	Pixel Data Register Read Address Bit 6	W	x
5	Pixel Data Register Read Address Bit 5	W	x
4	Pixel Data Register Read Address Bit 4	W	x
3	Pixel Data Register Read Address Bit 3	W	x
2	Pixel Data Register Read Address Bit 2	W	x
1	Pixel Data Register Read Address Bit 1	W	x
0	Pixel Data Register Read Address Bit 0	W	x

Bit 7-0 **Pixel Data Register Read Address Bits:** The address written to this register is actually the index (00H-FFH decimal) that selects one of 256 data registers in the LUT. After an address is written to this register, three consecutive reads should be performed at the 3C9 PELDATA port. Each read will yield a color value in the six LSBs of the 8-bit PELDATA Register. The first read value being R(Red), the next G(Green), and finally B(Blue). After reading three successive color values, the PELRD register will automatically increment to the next index.

The read cycle should not be interrupted by writing to the PELDATA Register as this may affect palette RAM contents. The PELRD Register may be written at any time. If the read cycle is interrupted by another read or write request (i.e., loading either the PELRD or PELWR Registers with data), the current cycle will be aborted.

NOTES:

1) Interrupts should be disabled during RAMDAC access.
2) ERF6[6] must be '1' to access this register. When ERF6[6] = '0', this register is RESERVED.
3) Writing a value to this register specifies an address within the color LUT, and loads the data register with the contents of the location in the color LUT addressed. Then the Address Read Register increments. This normally precedes reading one or more color values from the color LUT.

5.3 RAMDAC Pixel Write Address: PELWR

I/O Port Address: 3C8 (R/W)
ERF6[6] = '0'
Read Protection Bit: EREC[3]

Bit	Description	Access	Reset State
7(MSB)	Pixel Data Register Write Address Bit 7	R/W	x
6	Pixel Data Register Write Address Bit 6	R/W	x
5	Pixel Data Register Write Address Bit 5	R/W	x
4	Pixel Data Register Write Address Bit 4	R/W	x
3	Pixel Data Register Write Address Bit 3	R/W	x
2	Pixel Data Register Write Address Bit 2	R/W	x
1	Pixel Data Register Write Address Bit 1	R/W	x
0	Pixel Data Register Write Address Bit 0	R/W	x

Bit 7-0 **Pixel Data Register Write Address Bits:** The address written to this register is actually the index (00H-FFH) that selects one of 256 data registers in the LUT. After an address is written to this register, three consecutive writes should be performed at the 3C9 PELDATA port. Each 8-bit write to the PELDATA port should contain valid data in the six LSBs. The first write being R(Red), the next G(Green), and the third B(Blue). After writing three successive color values, this register will automatically increment to the next index.

The write cycle should not be interrupted by reading the PELDATA Register as this may affect palette RAM contents. The PELWR Register may be written at any time.

If the write cycle is interrupted by another read or write request (loading either the PELRD or PELWR Registers with data), the current cycle will be aborted and will not affect the contents of the RAMDAC palette.

NOTES:

1) Interrupts should be disabled during RAMDAC access.
2) Writing a value to this register specifies an address within the color LUT and initializes the RAM Data Register.
3) These operations would normally precede writing one or more color values to the color LUT.

5.4 RAMDAC Border Color Register: BDRCOL

I/O Port Address: 3C8 (R/W)
ERF6[6] = '1'
Read Protection Bit: EREC[3]

Bit	Description	Access	Reset State
7(MSB)	Border Color Data Bit 7	R/W	x
6	Border Color Data Bit 6	R/W	x
5	Border Color Data Bit 5	R/W	x
4	Border Color Data Bit 4	R/W	x
3	Border Color Data Bit 3	R/W	x
2	Border Color Data Bit 2	R/W	x
1	Border Color Data Bit 1	R/W	x
0	Border Color Data Bit 0	R/W	x

Bit 7-0 **Border Color Data Bits:** This register controls the RAMDAC border color to the LCD panel. To modify this border color, three consecutive writes should be performed to this register. Each 8-bit write should contain valid data in the six LSBs; the first write being B(Blue), the next G(Green), and the third R(Red). Displaying the border color on the LCD panel is accomplished by setting EREB[7-4] = 6.

NOTES:

1) Interrupts should be disabled during RAMDAC access.
2) This register should be written to three consecutive times to change the contents of the Border Color Register; this register should *always* be written to in multiples of three.

5.5 RAMDAC Pixel Data Register: PELDATA

I/O Port Address: 3C9 (R/W)
ERF6[6] = '0'
Read Protection Bit: EREC[3]

Bit	Description	Access	Reset State
7(MSB)	RESERVED	R/W	x
6	RESERVED	R/W	x
5	Pixel Data Register Bit 5	R/W	x
4	Pixel Data Register Bit 4	R/W	x
3	Pixel Data Register Bit 3	R/W	x
2	Pixel Data Register Bit 2	R/W	x
1	Pixel Data Register Bit 1	R/W	x
0	Pixel Data Register Bit 0	R/W	x

Bit 7-6 RESERVED

Bit 5-0 **Pixel Data Register Bits:** This register contains a 6-bit value used to read/write the current RAMDAC color table entry pointed to by the address in PELRD or PELWR Address Register.

For a correct loading sequence operation, an 8-bit write containing valid data in the six LSBs must be written to the PELDATA Register three consecutive times. For a correct reading sequence operation, the PELDATA Register is read three consecutive times. The valid data is contained in the six LSBs of this register. Each value corresponds to the respective Red, Green, and Blue color components of the lookup table entry at the address pointed to by the corresponding address register.

NOTE: If consecutive locations of the RAMDAC palette need to be accessed, only the first one needs to be specified by loading its address in either PELWR or PELRD. At the end of an Red, Green, and Blue sequence, the value in PELWR or PELRD will be automatically incremented. The read or write sequence should not be mixed with write or read operations to the PELDATA Register. Such interruption may affect palette RAM contents.

The PELRD or PELWR Register may be written at any time. The read or write sequence to PELDATA is interrupted by another read or write request (loading enter the PELWR on PELRD Registers with data). The current cycle will be aborted and will not affect the content of the RAMDAC palette. The next read or write to PELDATA will affect the Red value of the new index.

NOTE: Successive reading or writing operations on PELDATA must be separated by at least 240 ns.

6. CL-GD6340 EXTENSION REGISTERS

The extension registers provide additional functions to the CL-GD6340 beyond the standard EGA and VGA.

Register	Abbreviations	Register Name	Port	Index	Access	Page
ERX	–	Extensions Index Register	3C4	–	R/W	34
ER87	MISC2	Miscellaneous Control Register 2	3C5	87	R/W	35
ER8A	LCDCNTLI	LCD Control Register 1	3C5	8A	R/W	36
ERA7	MISC3	Miscellaneous Register 3	3C5	A7	R/W	37
ERC2	LCDCNTLII	LCD Control Register 2	3C5	C2	R/W	38
ERCD	RFRCLR	Red Frame Color Register	3C5	CD	R/W	39
ERCE	GFRCLR	Green Frame Color Register	3C5	CE	R/W	40
ERCF	BFRCLR	Blue Frame Color Register	3C5	CF	R/W	41
ERD0	COLOFF	Column Offset Register	3C5	D0	R/W	42
ERD1	PHDIS	Panel Horizontal Displayed Register	3C5	D1	R/W	43
ERD2	ROWOFF	Row Offset Register	3C5	D2	R/W	44
ERD3	PRST	Panel Row Segment Total Register	3C5	D3	R/W	45
ERD4	PNLCTLI	Panel Control Register 1	3C5	D4	R/W	46
ERD5	PNLCTLII	Panel Control Register 2	3C5	D5	R/W	47
ERD6	GSCNTL1	Grayscale Control Register 1	3C5	D6	R/W	48
ERD7	PRLLCLK	Programmable Retrace LLCLK Register	3C5	D7	R/W	49
ERD9	MOD	Modulation (AC Inversion) Register	3C5	D9	R/W	50
ERE0	ENRDBK	Enable Readback Register	3C5	E0	R/W	51
ERE1-E8	VSCR0-7	Scratch Pad Registers	3C5	E1-E8	R/W	52
ERE9	VIPREV	VIPAC Chip Revision Level Register	3C5	E9	R	53
EREA	PRGCL1	Programmable CL1 Delay Register	3C5	EA	R/W	54
EREB	BDRCTRL	Border Control Register	3C5	EB	R/W	55
EREC	GSCF1	Grayscale and Color Functions Register 1	3C5	EC	R/W	56
ERED	GSCF2	Grayscale and Color Functions Register 2	3C5	ED	R/W	57
EREE	PNCTRL3	Panel Control Register 3	3C5	EE	R/W	58
EREF	PNCTRL4	Panel Control Register 4	3C5	EF	R/W	59
ERF0	VSDY	VSYNC Delay Register	3C5	F0	R/W	60
ERF1	NGRAY	Number of Grayscales Register	3C5	F1	R/W	61
ERF2	PNCTRL1	Panel Interface Control Register 1	3C5	F2	R/W	62
ERF3	FRDC1	Frame Rate Duty Control Register 1	3C5	F3	R/W	64
ERF4	FRDC2	Frame Rate Duty Control Register 2	3C5	F4	R/W	65
ERF5	PNCTRL2	Panel Interface Control Register 2	3C5	F5	R/W	66
ERF6	VGAI	VGA Interface Register	3C5	F6	R/W	67
ERF7-FF		RESERVED	3C5	F7-FF	R/W	–

NOTE: Extensions Index Register 3C4 is also read and write enabled by EXTSEL or ALLSEL, and is read and write protected by 'sleep'.

6.1 Extensions Index Register: ERX

I/O Port Address: 3C4

Read/Write Protection Bit: EXTSEL or ALLSEL

Bit	Description	Access	Reset State
7 (MSB)	Extensions Index Bit 7	R/W	0
6	Extensions Index Bit 6	R/W	0
5	Extensions Index Bit 5	R/W	0
4	Extensions Index Bit 4	R/W	0
3	Extensions Index Bit 3	R/W	0
2	Sequencer/Extensions Index Bit 2	R/W	0
1	Sequencer/Extensions Index Bit 1	R/W	0
0 (LSB)	Sequencer/Extensions Index Bit 0	R/W	0

Bits 7-0 **Extensions Index Bits:** The Sequencer/Extensions Index Register defines which registers, Sequencer Registers or CL-GD6340 Extensions Registers are accessible through 3C5. In standard IBM EGA/VGA, the three least significant bits determine the Sequencer Register to be accessed at 3C5. In the CL-GD6340, Bits 3-7 were added to allow more registers to be accessed through 3C5. In order to access the standard Sequencer Registers, Bits 3-7 should be programmed to '0'. When accessing extended registers, all eight bits are used to specify which extension register will be accessed.

6.2 Miscellaneous Control Register 2: MISC2

I/O Port Address: 3C5

Index: 87

Read/Write Protection Bit: EXTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	Unused		x
6	Arm Video Subsystem	R/W	0
5	Unused		x
4	Unused		x
3	Unused		x
2	Unused		x
1	Unused		x
0	Unused		x

Bits 7, 5-0	Unused
Bit 6	**Arm Video Subsystem:** When this bit is '1', the active Sleep Address Register, determined by ERF6[7], is made visible. The CL-GD6340 can be put to sleep (disable memory and I/O) by writing '1' to the active sleep port. While system is asleep, only the active sleep port will be recognized. Writing a '0' to this port will reawaken the video subsystem. Typically, an adapter video BIOS will recognize the presence of a motherboard video BIOS, put it to sleep and perform the display switch BIOS function call.

6.3 LCD Control Register 1: LCDCNTLI

I/O Port Address: 3C5

Index: 8A

Read/Write Protection Bit: EXTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	Enable Standby Mode	R/W	0
6	Force 8-dot Text Mode		0
5	RESERVED		x
4	RESERVED		x
3	RESERVED		x
2	RESERVED		x
1	RESERVED		x
0	RESERVED		x

Bit 7 **Enable Standby Mode:** In Standby Mode, the data paths for video signal processing are disabled.

NOTE: See Section 3.7 for details.

Bit 6 **Force 8-dot Text Mode:** VGA and MGA text modes are normally 9-dot modes. This bit will force VGA and MGA text modes to run with eight dots per character. This bit will take effect in CRT modes as well as LCD modes. Normally this bit should be set.

NOTE: This bit is used to force 8-dot Mode and causes the 8-dot/9-dot bit in SR1[0] to be ignored.

Bit 5-0 RESERVED

6.4 Miscellaneous Register 3: MISC3

I/O Port Address: 3C5

Index: A7

Read/Write Protection Bit: EXTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	RESERVED		x
6	RESERVED		x
5	RESERVED		x
4	Suspend	R/W	0
3	RESERVED		x
2	RESERVED		x
1	CRT Control	R/W	0
0	LCD Control	R/W	0

Bits 7-5	RESERVED
Bit 4	**Suspend:** When this bit is set, the internal MCLK signal is disabled and the RAMDAC is turned off. **NOTE:** See Section 3.8 for details.
Bits 3-2	RESERVED
Bit 1	**CRT Control:** Set to 1 = CRT output pads on Set to 0 = CRT output pads off (SYNCs are tri-stated and RGB are blanked) **NOTE:** See Section 3.8 for details.
Bit 0	**LCD Control:** This bit is used to control LCD power sequencing. Set to 1 = Initiates ON Power Sequencing Set to 0 = Initiates OFF Power Sequencing **NOTE:** See Sections 3.6 and 3.8 for details.

6.5 LCD Control Register 2: LCDCNTLII

I/O Port Address: 3C5

Index: C2

Read/Write Protection Bit: stingsec or allsec

Bit#	Description	Access	Reset State
7(MSB)	RESERVED	R/W	0
6	RESERVED	R/W	0
5	RESERVED	R/W	0
4	RESERVED	R/W	0
3	RESERVED	R/W	0
2	RESERVED	R/W	0
1	Enable LCD Expanded Graphics Mode	R/W	0
0	RESERVED	R/W	0

Bit 7:2	RESERVED
Bit 1	**Enable LCD Expanded Graphics Mode**: When this bit is set to 1, a predetermined set of scanlines will be replicated in graphics modes. This to fill the LCD panel with as many lines as possible. When reset, no lines are replicated.
Bit 0	RESERVED

NOTE: In Expanded Mode, 400-line Mode converts to 475 lines, 350-line Mode converts to 472 lines, 200 lines converts to 400 lines by scanline doubling, which converts to 475 lines. However, the Vertical Total Register should be programmed to 525 lines so that blank lines fill in the remaining LCD screen.

6.6 Red Frame Color Register: RFRCLR

I/O Port Address: 3C5

Index: CD

Read/Write Protection Bit: EXTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	RESERVED		x
6	RESERVED		x
5	RESERVED		x
4	RESERVED		x
3	Red Frame Color Bit 3	R/W	0
2	Red Frame Color Bit 2	R/W	0
1	Red Frame Color Bit 1	R/W	0
0	Red Frame Color Bit 0	R/W	0

Bit 7-4 RESERVED

Bit 3-0 **Red Frame Color Bits:** These bits control the red shade of the non-displayed portion of the LCD screen. Up to 16 shades can be selected (0h = darkest shade, Fh = brightest shade). It will automatically track the settings of the reverse video in text and graphics modes.

NOTE: The shade programmed into this register will be reversed if Bit 3 or Bit 6 of ERD5 (PNCNTLII Register) is set.

6.7 Green Frame Color Register: GFRCLR

I/O Port Address: 3C5

Index: CE

Read/Write Protection Bit: EXTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	RESERVED		x
6	RESERVED		x
5	RESERVED		x
4	RESERVED		x
3	Green Frame Color Bit 3	R/W	0
2	Green Frame Color Bit 2	R/W	0
1	Green Frame Color Bit 1	R/W	0
0	Green Frame Color Bit 0	R/W	0

Bit 7-4	RESERVED
Bit 3-0	**Green Frame Color Bits:** These bits control the green shade of the non-displayed portion of the LCD screen. Up to 16 shades can be selected (0 = darkest shade, Fh = brightest shade). It will automatically track the settings of the reverse video in text and graphics modes.

NOTE: The shade programmed into this register will be reversed if Bit 3 or Bit 6 of ERD5 (PNCNTLII Register) is set.

6.8 Blue Frame Color Register: BFRCLR

I/O Port Address: 3C5

Index: CF

Read/Write Protection Bit: EXTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	RESERVED		x
6	RESERVED		x
5	RESERVED		x
4	RESERVED		x
3	Blue Frame Color Bit 3	R/W	0
2	Blue Frame Color Bit 2	R/W	0
1	Blue Frame Color Bit 1	R/W	0
0	Blue Frame Color Bit 0	R/W	0

Bit 7-4	RESERVED
Bit 3-0	**Blue Frame Color Bits:** These bits control the blue shade of the non-displayed portion of the LCD screen. Up to 16 shades can be selected (0 = darkest shade, F = brightest shade). It will automatically track the settings of the reverse video in text and graphics modes.

NOTE: The shade programmed into this register will be reversed if Bit 3 or Bit 6 of ERD5 (PNCNTLII Register) is set.

6.9 Column Offset Register: COLOFF

I/O Port Address: 3C5
Index: D0 (and D4[4])
Read/Write Protection Bit: EXTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	Column Offset Bit 7	R/W	0
6	Column Offset Bit 6	R/W	0
5	Column Offset Bit 5	R/W	0
4	Column Offset Bit 4	R/W	0
3	Column Offset Bit 3	R/W	0
2	Column Offset Bit 2	R/W	0
1	Column Offset Bit 1	R/W	0
0	Column Offset Bit 0	R/W	0

Bits 7-0 **Column Offset Bits:** The main purpose of this register is to provide the panning function (640 pixels left or right) for MGA Reduction Mode and compensate for the CL-GD6340 internal pipeline delays. Programming a value for a specific panel, found in the table below, (and a '0' for Bit 8 at extension register index location D4[6]) will cause the data being sent to the display to start with the first (leftmost) pixel of the display to start at the first displayable location (0). In MGA reduction mode, this will cause the leftmost 640 out of 720 pixels to be displayed.

This register should be programmed to some value to account for internal pipeline delays from data input to data output. In the case of the C8SS panel, this register should be programmed with 0BH. See the table below for other panel settings. Setting a value will cause the display to start at the programmed location; thus, for displaying the rightmost 640 out of 720 pixels in MGA Mode, a value of 80 decimal (50 Hex) should be added to the recommended base value below for the appropriate panel type. See the following table:

Panel	Recommended Base Value (Hex)
C8SS†	0B
C4096SS†	0B
C512SS†	06
C8SSI†	0B
C8DD†	0B
M2DD†	0B (green pass-through) 0E (Sum-to-Gray green)
M2SS†	0B (green pass through) 0E (Sum-to-Gray green)

NOTE: † Refer to the glossary for explanation of these terms.

6.10 Panel Horizontal Displayed Register: PHDIS

I/O Port Address: 3C5

Index: D1 (and D4[5])

Read/Write Protection Bit: EXTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	Number of Horizontal Displayed Nibbles Bit 7	R/W	0
6	Number of Horizontal Displayed Nibbles Bit 6	R/W	0
5	Number of Horizontal Displayed Nibbles Bit 5	R/W	0
4	Number of Horizontal Displayed Nibbles Bit 4	R/W	0
3	Number of Horizontal Displayed Nibbles Bit 3	R/W	0
2	Number of Horizontal Displayed Nibbles Bit 2	R/W	0
1	Number of Horizontal Displayed Nibbles Bit 1	R/W	0
0	Number of Horizontal Displayed Nibbles Bit 0	R/W	0

Bits 7-0 **Number of Horizontal Displayed Nibbles Bits:** This 9-bit Register (See ERD4[5] for the eighth MSB) determines the width of the panel in nibbles (4-bit groups). For 640-column panels, this register should be programmed to (640/4)-1 = 159 decimal (9FH). Panels up to 2048 bits wide can be accommodated.

6.11 Row Offset Register: ROWOFF

I/O Port Address: 3C5
Index: D2 (and D4[6])
Read/Write Protection Bit: EXTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	Row Offset Value Bit 7	R/W	0
6	Row Offset Value Bit 6	R/W	0
5	Row Offset Value Bit 5	R/W	0
4	Row Offset Value Bit 4	R/W	0
3	Row Offset Value Bit 3	R/W	0
2	Row Offset Value Bit 2	R/W	0
1	Row Offset Value Bit 1	R/W	0
0	Row Offset Value Bit 0	R/W	0

Bits 7-0 **Row Offset Value Bits:** If the Enable1 Bit ERD4[3] of PNLCTL1 Register is '0' (Disable Auto-Center), the value in this register determines how many rows from the top of the panel the image will start being displayed.

6.12 Panel Row Segment Total Register: PRST

I/O Port Address: 3C5

Index: D3 (and D4[7])

Read/Write Protection Bit: EXTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	Panel Row Segment Total Bit 7	R/W	0
6	Panel Row Segment Total Bit 6	R/W	0
5	Panel Row Segment Total Bit 5	R/W	0
4	Panel Row Segment Total Bit 4	R/W	0
3	Panel Row Segment Total Bit 3	R/W	0
2	Panel Row Segment Total Bit 2	R/W	0
1	Panel Row Segment Total Bit 1	R/W	0
0	Panel Row Segment Total Bit 0	R/W	0

Bits 7-0 **Panel Row Segment Total Bits:** This register contains the number of rows of the panel.

For single-drive panels, the value programmed into this register is the panel vertical size (i.e., 480 for a 480-line panel)

For dual-drive LCDs, the value programmed into this register is half the panel vertical size (i.e., 240 for a 480-line panel).

The maximum panel size which can be accommodated is then two times the value loaded in this register (and Bit 8 located in ERD4[7]), or 512 x 2 = 1024.

6.13 Panel Control Register 1: PNLCTLI

I/O Port Address: 3C5

Index: D4

Read/Write Protection Bit: EXTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	Bit-8(MSB) Panel Row Seg Total	R/W	0
6	Bit-8(MSB) Row Offset	R/W	0
5	Bit-8(MSB) Panel Horizontal Displayed	R/W	0
4	Bit-8(MSB) Column Offset	R/W	0
3	Screen Alignment Enable1	R/W	0
2	Extra Line Clock Enable	R/W	0
1	RESERVED		x
0	Screen Alignment Enable0	R/W	0

Bit 7 — **Bit-8(MSB) Panel Row Seg Total:** This is the overflow (ninth) bit from Panel Row Segment Total Register: PRST,

Bit 6 — **Bit-8(MSB) Row Offset:** This is the overflow (ninth) bit from Row Offset: ROWOFF,

Bit 5 — **Bit-8(MSB) Panel Horizontal Displayed:** This is the overflow (ninth) bit from Panel Horizontal Displayed: PHDIS,

Bit 4 — **Bit-8(MSB) Column Offset:** This is the overflow (ninth) bit from Column Offset: COLOFF.

Bit 3, 0 — **Screen Alignment Enable1 and Enable0:**

3	0	Description
0	0	Bottom alignment of display
0	1	Top alignment of display
1	X	Center alignment of display

Bit 2 — **Extra Line Clock Enable:** When this bit is set, it generates an extra BCLCLK pulse for lower panel. This is useful for panels requiring an extra BCLCLK pulse for lower panel.

Bit 1 — RESERVED

6.14 Panel Control Register 2: PNLCTLII

I/O Port Address: 3C5

Index: D5

Read/Write Protection Bit: EXTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	RESERVED		x
6	Enable Reverse Video in Text Mode	R/W	0
5	RESERVED		x
4	RESERVED		x
3	Enable Reverse Video in Graphics Mode	R/W	0
2	RESERVED		x
1	MGA Reduction (MSB)	R/W	0
0	MGA Reduction (LSB)	R/W	0

Bit 7 RESERVED

Bit 6 **Enable Reverse Video in Text Mode:** When set, and in Text Mode, the screen image is reversed. See Attribute Controller Mode Control Register AR10[0] for determination of Text or Graphics Mode.

NOTE: This is ONLY for panels that use grayscales.

Bit 5, 4 RESERVED

Bit 3 **Enable Reverse Video in Graphics Mode:** Setting this bit will reverse the screen image when in Graphics Mode. See Attribute Controller Mode Control Register AR10[0] for determination of Text or Graphics Mode.

NOTE: This is ONLY for panels that use grayscales.

Bit 2 RESERVED

Bit 1-0 **MGA Reduction:** Displays 720-pixel Hercules graphics images on a 640-pixel display as follows:

Bit 1	Bit 0	Description
0	X	Display 640 pixels out of 720 pixels, position determined by the value stored in the Column Offset Register (ERD0).
1	0	Skip every ninth pixel.
1	1	The eighth pixel becomes the logical 'OR' of every eighth and ninth pixel, and the ninth pixel is skipped.

6.15 Grayscale Control 1 Register: GSCNTL1

I/O Port Address: 3C5

Index: D6

Read/Write Protection Bit: EXTSEL or ALLSEL

Bit	Description	Access	Reset State
7	RESERVED		x
6	RESERVED		x
5	RESERVED		x
4	RESERVED		x
3(MSB)	GS3	R/W	1
2	GS2	R/W	1
1	GS1	R/W	0
0(LSB)	GS0	R/W	1

Bit 7-4	RESERVED
Bit 3-0	**GS3-0:** This register is provided to adjust grayscale appearance. Normally, this register should not be modified.

6.16 Programmable Retrace LLCLK Register: PRLLCLK

I/O Port Address: 3C5

Index: D7

Read/Write Protection Bit: EXTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	RESERVED		x
6	RESERVED		x
5	RESERVED		x
4	Programmable Retrace Bit 4: MSB	R/W	0
3	Programmable Retrace Bit 3	R/W	0
2	Programmable Retrace Bit 2	R/W	0
1	Programmable Retrace Bit 1	R/W	0
0	Programmable Retrace Bit 0: LSB	R/W	0

Bit 7-5	RESERVED
Bit 4-0	**Programmable Retrace Bits:** This register inserts the specified number of BCLCLK pulses during vertical retrace. Extra BCLCLK pulses are necessary for sequentially displaying the data at 'unusual' boundary conditions of the panel shift registers that control which line is to be displayed, or controlling the effect of the AC inversion signals on some panels. **NOTE:** The value programmed into this register should be one more than is necessary. For example, to obtain eight extra line clock pulses, a value of nine must be written into this register.

6.17 Modulation (AC Inversion) Register: MOD

I/O Port Address: 3C5

Index: D9

Read/Write Protection Bit: EXTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	AC Modulation Bit 7	R/W	0
6	AC Modulation Bit 6	R/W	0
5	AC Modulation Bit 5	R/W	0
4	AC Modulation Bit 4	R/W	0
3	AC Modulation Bit 3	R/W	0
2	AC Modulation Bit 2	R/W	0
1	AC Modulation Bit 1	R/W	0
0(LSB)	AC Modulation Bit 0	R/W	0

Bits 7-0 **AC Modulation Bits**: The contents of this register determines the half-period of the square-wave output on the BMOD Pin. This period is either in terms of line clocks or frame clocks, determined by ERF5[3]. Normally, a number that does not divide evenly into the panel size is used.

NOTES:

LCD panels must have a modulation signal (sometimes referred to as AC inversion) to:

1) Invert the LCD drive voltages in order to prevent any net DC voltage from appearing on the LCD fluid (which can cause chemical breakdown of the LCD material and destroy the panel).
2) Reduce LCD crosstalk.

   Some panels have this function built-in, and may not require connection to the BMOD Pin, which this register controls.

6.18 Enable Readback Register: ENRDBK

I/O Port Address: 3C5

Index: E0

Read Protection Bit: INTSEL

Bit	Description	Access	Reset State
(7-4)	Enable Bits to Extension Register	R/W	F
(3-0)	Enable Bits to Extension Register	R/W	0

Bits 7-0 **Enable Bits to Extension Register:** This register is for read and write protection for the various registers, and shadow registers in the CL-GD6340. By writing the values described below to this register, certain register sets are enabled for reading and writing. See the table below for a full description of what is enabled for each register value. To disable reading and writing of the CL-GD6340 registers, write a value other than 9A, C5, A3, or F0 to this register.

NOTES:

1) This register, ENRDBK, is always writable, but may not be readable depending upon the security selection.
2) Index register 03C4 will be read/write protected when EXTSEL is not activated. However, when this occurs its contents point to index E0, since this was the last written value.

Register Value Enabled Registers	9A INTSEL	C5 VGASEL	A3 EXTSEL	F0 ALLSEL	All other values None
EGA/VGA	Write Only	Yes	Write Only	Yes	Write Only
Extension Set 1	No	No	Yes	Yes	No
Extension Set 2	Yes	No	No	Yes	No

EGA/VGA Set = These are the standard EGA/VGA registers shadowed in the CL-GD6340:
03C0, 03C1, 03C2, 03C3, 03C4, 03C5, 03C6, 03C7, 03C8, 03C9, 03CC, 03CE, 03CF, 46E8, 03?4, 03?5, 03?8.

Extension Set 1 = These are 'shared' registers between the VGA controller and the CL-GD6340:
3C4, 3C5[87], 3C5[8A], 3C5[A7], 3C5[C2], 3C5[CD], 3C5[CE], 3C5[CF], 3C5[D0], 3C5[D1], 3C5[D2], 3C5[D3], 3C5[D4], 3C5[D5], 3C5[D6], 3C5[D7], 3C5[D8], 3C5[D9].

Extension Set 2 = These are CL-GD6340 registers only:
3C5[E0], 3C5[E1], 3C5[E2], 3C5[E3], 3C5[E4], 3C5[E5], 3C5[E6], 3C5[E7], 3C5[E8], 3C5[E9], 3C5[EA], 3C5[EB], 3C5[EC], 3C5[ED], 3C5[EE], 3C5[EF], 3C5[F0], 3C5[F1], 3C5[F2], 3C5[F3], 3C5[F4], 3C5[F5], 3C5[F6].

NOTE: ? = 'D' hex for color and 'B' hex for monochrome.

6.19 Scratch Pad Registers: VSCR0-7

I/O Port Address: 3C5

Index: E1-E8

Read/Write Protection Bit: INTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	Scratch Register Bit 7	R/W	x
6	Scratch Register Bit 6	R/W	x
5	Scratch Register Bit 5	R/W	x
4	Scratch Register Bit 4	R/W	x
3	Scratch Register Bit 3	R/W	x
2	Scratch Register Bit 2	R/W	x
1	Scratch Register Bit 1	R/W	x
0(LSB)	Scratch Register Bit 0	R/W	x

Bits 7-0 **Scratch Register Bits:** These eight 8-bit read/write registers are provided for software (BIOS, etc.) to store values temporarily. None of the bits are connected to direct hardware functions. These registers are NOT reset on power-up or reset.

All of these registers are RESERVED for use by the BIOS and associated Cirrus Logic utility programs. None of these registers are available for user programs.

6.20 VIPAC Chip Revision Level Register: VIPREV

I/O Port Address: 3C5

Index: E9

Read/Write Protection Bit: INTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	VIPAC Identification Bit 3	R	1
6	VIPAC Identification Bit 2	R	0
5	VIPAC Identification Bit 1	R	0
4	VIPAC Identification Bit 0	R	0
3	VIPAC Revision Bit 3	R	1
2	VIPAC Revision Bit 2	R	1
1	VIPAC Revision Bit 1	R	1
0(LSB)	VIPAC Revision Bit 0	R	1

Bits 7-4	**VIPAC Identification Bits:** The identification of the CL-GD6340 is determined by reading this register twice. The first time the register is read, an ID of '8' is returned in these four bits. The second read will return the complement of this value or '7' from these four bits. This method is used by the BIOS to check for proper CL-GD6340 connection. The flip-flop that toggles the read is reset by any write to this register.
Bits 3-0	**VIPAC Revision Bits:** The CL-GD6340 chip revision is determined by these four bits. The value returned is uniquely fixed for each chip revision. The value above (F hex) is for revision 1. This value decrements by one with each revision.

6.21 Programmable CL1 Delay Register: PRGCL1

I/O Port Address: 3C5

Index: EA

Read/Write Protection Bit: INTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	CL1 Bit 7	R/W	0
6	CL1 Bit 6	R/W	0
5	CL1 Bit 5	R/W	0
4	CL1 Bit 4	R/W	0
3	CL1 Bit 3	R/W	0
2	CL1 Bit 2	R/W	0
1	CL1 Bit 1	R/W	0
0(LSB)	CL1 Bit 0	R/W	0

Bits 7-0	**CL1 Bits:** This register contains the eight lower bits for the Programmable CL1 Delay Counter. The ninth bit resides in ERED[3]. These bits are programmed to load a specific value to the extra line clock delay counter. This counter serves to delay the BRLCLK signal with respect to BCLCLK. This feature is useful for some C8SSI† panels.

NOTE: † Refer to the glossary for explanation of this term.

6.22 Border Control Register: BDRCTRL

I/O Port Address: 3C5

Index: EB

Read/Write Protection Bit: INTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	Force Frame Color	R/W	0
6	Disable Frame Color to LCD	R/W	0
5	Select RAMDAC Border	R/W	0
4	Force LCD Output Enable	R/W	0
3	RESERVED	R/W	0
2	RESERVED	R/W	0
1	RESERVED	R/W	0
0(LSB)	RESERVED	R/W	0

Bit 7 **Force Frame Color:** When set, this bit selects Red (ERCD), Green (ERCE), and Blue (ERCF) Frame Color Registers as the data source to the grayscale datapath. When reset, the normal datapath is selected, except in non-display time (in which Frame Color is selected).

NOTE: Currently frame color is not used for C512SS† panels.

Bit 6 **Disable Frame Color to LCD:** Normally, the frame color registers ERCD, ERCE, and ERCF determine the frame color to the panel. However, there may be applications where both the LCD and CRT should be the same. When this bit is set, the border color from the RAMDAC or the VGA AR11 Overscan Register is used. When reset, this bit allows the normal operation of frame color. See EREB[5] for more details.

NOTE: Currently frame color is not used for C512SS† panels.

Bit 5 **Select RAMDAC Border:** When set, this allows the border register in the RAMDAC to be used as the border for the CRT. When reset, it always selects the RAM data to the DAC. The normal VGA Border Register AR11 is used. When this bit is set and EREB[6] = 1 (Disable Frame Color Registers), the RAMDAC border register is used for CRT and LCD.

EREB [6:5]		Source for CRT During Non-display Time	Source for LCD During Non-display Time
0	0	VGA Overscan AR11	Frame color ERCD, ERCE, ERCF
0	1	RAMDAC Border	Frame color ERCD, ERCE, ERCF
1	0	VGA Overscan AR11	VGA Overscan AR11
1	1	RAMDAC Border	RAMDAC Border

Bit 4 **Force LCD Output Enable:** When set this forces the panel output pads (PDATA[15:0], BMOD, BSHCLK, BCLCLK, BRLCLK, BLFS, and BENRL/DEN) to be enabled regardless of the state of Power Sequencing (ERA7). This is NOT generally recommended.

Bits 3-0 RESERVED

NOTE: † Refer to the glossary for explanation of these terms.

6.23 Grayscale and Color Functions Register 1: GSCF1

I/O Port Address: 3C5
Index: EC
Read/Write Protection Bit: INTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	RESERVED	R/W	0
6	Enhanced Gray Shade Enable	R/W	0
5	RESERVED	R/W	0
4	RESERVED	R/W	0
3	Enable RAMDAC Read	R/W	0
2	Grayscale Select Bit 1	R/W	0
1	Grayscale Select Bit 0	R/W	0
0(LSB)	Sum-to-Gray Enable	R/W	0

Bit 7 RESERVED

Bit 6 **Enhanced Gray Shade Enable:** This bit is used for some C8SS† color panels. When set it enables proprietary logic to smooth colors.

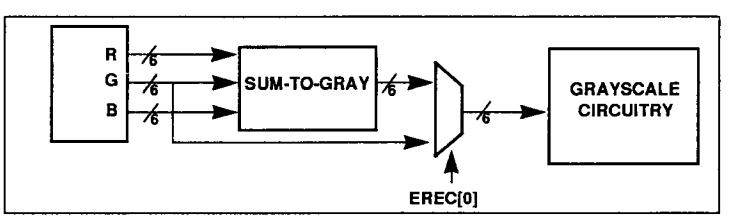
Bit 5, 4 RESERVED

Bit 3 **Enable RAMDAC Read:** When this bit is set, the internal RAMDAC of the CL-GD6340 is readable by the CPU. This avoids possible conflict with other RAMDACs.

Bit 2, 1 **Grayscale Select Bits:** (See Stippling Logic and Grayscale ROM)

1	0	Description
1	1	16 grayshades selected
1	0	8 grayshades selected
0	1	4 grayshades selected
0	0	2 grayshades selected

Bit 0 **Sum-to-Gray Enable:** When set, the CL-GD6340 performs a hardware-based Sum-To-Gray of its RGB input, processes the values, and displays them on the panel. When reset, the CL-GD6340 passes the value supplied by its G input lines from the RAMDAC. This is useful for monochrome monitor emulation.



NOTE: † Refer to the glossary for explanation of this term.

6.24 Grayscale and Color Functions Register 2: GSCF2

I/O Port Address: 3C5

Index: ED

Read/Write Protection Bit: INTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	RESERVED	R/W	0
6	Image Enhancement	R/W	0
5	Select Alternate Waveform	R/W	0
4	Select CL1 Clock	R/W	0
3	9th Bit for CL1 Counter	R/W	0
2	RESERVED	R/W	0
1	RESERVED	R/W	0
0(LSB)	RESERVED	R/W	0

Bit 7	RESERVED
Bit 6	**Image Enhancement:** When set, this bit reduces flicker to the panel. When reset, normal stippling occurs.
Bit 5	**Select Alternate Waveform:** When this bit is set, it selects the NGRAY waveform specified in ERF1. When this bit is cleared, it selects the default waveform, which is the same as in the CL-GD610/620.
Bit 4	**Select CL1 Clock:** When set, this selects an extra line clock (CL1) to the BRLCLK Pin for some C8SSI† panels. When reset, this bit selects normal upper panel shift clock to the BRLCLK pin. This bit is primarily used for C8SSI† with an 8-bit data interface.
Bit 3	**9th Bit for CL1 Counter:** This is the MSB of the Programmable CL1 Delay Counter contained in EREA.
Bit 2-0	RESERVED

NOTE: † Refer to the glossary for explanation of this term.

6.25 Panel Control Register 3: PNCTRL3

I/O Port Address: 3C5

Index: EE

Read/Write Protection Bit: INTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	RESERVED	R/W	0
6	RESERVED	R/W	0
5	RESERVED	R/W	0
4	RESERVED	R/W	0
3	RESERVED	R/W	0
2	RESERVED	R/W	0
1	RESERVED	R/W	0
0(LSB)	RESERVED	R/W	0

Bit 7-0 RESERVED: This register is RESERVED and should only be programmed to values specified by Cirrus Logic.

6.26 Panel Control Register 4: PNCTRL4

I/O Port Address: 3C5

Index: EF

Read/Write Protection Bit: INTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	RESERVED	R/W	0
6	RESERVED	R/W	0
5	RESERVED	R/W	0
4	RESERVED	R/W	0
3	RESERVED	R/W	0
2	RESERVED	R/W	0
1	RESERVED	R/W	0
0(LSB)	RESERVED	R/W	0

Bit 7-0 RESERVED: This register is RESERVED and should only be programmed to values specified by Cirrus Logic.

6.27 VSYNC Delay Register: VSDY

I/O Port Address: 3C5

Index: F0

Read/Write Protection Bit: INTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	Force VSYNC, HSYNC polarity	R/W	0
6	Stipple Control 0	R/W	0
5	Stipple Control 1	R/W	0
4	Stipple Control 2	R/W	0
3	RESERVED	R/W	0
2	Invert BLFS and BCLCLK	R/W	0
1	RESERVED	R/W	0
0(LSB)	RESERVED	R/W	0

Bit 7 **Force VSYNC, HSYNC polarity**: When set, this bit forces the VSYNC, HSYNC polarity to be the same as the 480-line Mode for the CRT. See Miscellaneous Output Register MISC Bits 6 and 7 for more details about 480-line Mode. This bit is only set by the BIOS when in simultaneous CRT/LCD Mode with the CL-GD6340 driving the CRT.

Bit 6-4 **Stipple Control:** Normally set to '010'.

6 5 4	Function	Dependencies
0 0 0	No stipple	none
0 0 1	H stipple in 256-color graphics	shift256
0 1 0	H or HV stipple in Mode 13	shift256, cell-height, scandbl, pixdbl
0 1 1	H stipple in all graphics modes	graphics
1 0 0	HV stipple in all graphics modes	graphics
1 0 1	H stipple in all modes (graphics and text)	none
1 1 0	HV stipple in all modes (graphics and text)	none
1 1 1	HV stipple in all modes (graphics and text)	none

NOTE:

H stipple means horizontal stipple

HV stipple means horizontal and vertical stippling

shift256 -> GR5[6] = 1

cell-height = 00001 -> CR9[4:0] = 00001

pixdbl -> AR10[6] = 1

graphics -> AR10[1] = 1

scandbl -> CR9[7] = 1

Mode13 -> shift256 and pixdbl and {(scandbl = 00001) or (cell-height = 00001)}

Bit 3 RESERVED

Bit 2 **Invert BLFS and BCLCLK:** When set, BLFS and BCLCLK are inverted.

Bits 1-0 RESERVED

6.28 Number of Grayscales Register: NGRAY

I/O Port Address: 3C5

Index: F1

Read/Write Protection Bit: INTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	RESERVED	R/W	0
6	RESERVED	R/W	0
5	RESERVED	R/W	0
4	NGRAY Bit 4 (MSB)	R/W	0
3	NGRAY Bit 3	R/W	0
2	NGRAY Bit 2	R/W	0
1	NGRAY Bit 1	R/W	0
0(LSB)	NGRAY Bit 0 (LSB)	R/W	1

Bit 7-5	RESERVED
Bit 4-0	**NGRAY Bits:** Set these bits to one less than the number of desired grayscales.

NOTE: Desired grayscales of N-1 MUST be loaded.

6.29 Panel Interface Control Register 1: PNCTRL1

I/O Port Address: 3C5

Index: F2

Read/Write Protection Bit: INTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	Select Color or Monochrome	R/W	0
6	Select Dual or Single Panel	R/W	0
5	Select Interleaved or Non-Interleaved	R/W	0
4	Panel Data Format Bit 2	R/W	0
3	Panel Data Format Bit 1	R/W	0
2	Panel Data Format Bit 0	R/W	0
1	Enable Border SimulSCAN	R/W	0
0(LSB)	Invert BSHCLK	R/W	0

Bit 7 **Select Color or Monochrome:** Color is selected when set (monochrome is default).

Bit 6 **Select Dual or Single Panel:** Dual panel is selected when set (single panel is default).

Bit 5 **Select Interleaved or Non-Interleaved:** Interleaved is selected when set (Non-interleaved is default).

7	6	5	Description	Type
0	0	0	Monochrome Single Panel	M2SS†
0	0	1	Monochrome Single Panel Interleaved	
0	1	0	Monochrome Dual Panel	M2DD†
0	1	1	Monochrome Dual Panel Interleaved	
1	0	0	Color Single Panel	C8SS†, C512SS†, C4096SS†
1	0	1	Color Single Panel Interleaved	C8SSI-16 bit†, C8SSI+CL1†, C8SSI-8bit
1	1	0	Color Dual Panel	C8DD†
1	1	1	RESERVED	

Bit 4-2 **Panel Data Format Bits:** These bits determine the data interface to the panel.

4	3	2	Type
0	0	0	C8SS, C512SS, C4096SS (default)†
0	0	1	RESERVED
0	1	0	C8DD†
0	1	1	M2DD†
1	0	0	RESERVED
1	0	1	M2SS†, C8SSI-8 bit†
1	1	0	C8SSI-16 bit, C8SSI+CL1†
1	1	1	RESERVED

6.29 Panel Interface Control Register 1: PNCTRL1 *(cont.)*

Bit 1	**Enable Border SimulSCAN:** When set, this suppresses the border on the CRT during SimulSCAN. When reset, this allows normal operation of the border on the CRT. See EREB[6:5] for border selection. Normally, this bit is set only when the CL-GD6340 is being driven by the CL-GD610/620 controllers.
Bit 0	**Invert BSHCLK:** When set, BSHCLK is inverted. When reset, BSHCLK has its normal phase relationship.

NOTE: † Refer to the glossary for explanation of these terms.

6.30 Frame Rate Duty Control Register 1: FRDC1

I/O Port Address: 3C5

Index: F3

Read/Write Protection Bit: INTSEL or ALLSEL

Bit	Description	Access	Reset State
7(MSB)	RESERVED		x
6	RESERVED		x
5	Frame Rate Duty Control 1 Bit 5	R/W	0
4	Frame Rate Duty Control 1 Bit 4	R/W	0
3	Frame Rate Duty Control 1 Bit 3	R/W	0
2	Frame Rate Duty Control 1 Bit 2	R/W	0
1	Frame Rate Duty Control 1 Bit 1	R/W	0
0(LSB)	Frame Rate Duty Control 1 Bit 0	R/W	0

Bit 7-6	RESERVED
Bit 5-0	**Frame Rate Duty Control 1 Bits 5-0:** This register is RESERVED and should only be programmed to values specified by Cirrus Logic.

6.31 Frame Rate Duty Control Register 2: FRDC2

I/O Port Address: 3C5

Index: F4

Read/Write Protection Bit: peasec or allsec

Bit	Description	Access	Reset State
7(MSB)	Unused		x
6	Unused		x
5	Unused		x
4	Frame Rate Duty Control 2 Bit 4	R/W	0
3	Frame Rate Duty Control 2 Bit 3	R/W	0
2	Frame Rate Duty Control 2 Bit 2	R/W	0
1	Frame Rate Duty Control 2 Bit 1	R/W	0
0(LSB)	Frame Rate Duty Control 2 Bit 0	R/W	0

Bit 7-5	Unused
Bit 4-0	**Frame Rate Duty Control 2 Bits 4-0:** This register is RESERVED and should only be programmed to values specified by Cirrus Logic.

6.32 Panel Interface Control Register 2: PNCTRL2

I/O Port Address: 3C5

Index: F5

Read/Write Protection Bit: INTSEL or ALLSEL

Bit	Description	Access	Reset State
7	Bypass HSYNC	R/W	0
6	HSYNC Bit 2	R/W	0
5	HSYNC Bit 1	R/W	0
4	HSYNC Bit 0	R/W	0
3	MOD Clock Source	R/W	0
2	Data Source Select Bit 2	R/W	0
1	Data Source Select Bit 1	R/W	0
0	Data Source Select Bit 0	R/W	1

Bit 7 **Bypass HSYNC:** When set, this bit passes the HSYNC Signal directly to the panel interface BCLCLK. When reset, it allows the normal HSYNC pipeline logic to occur.

NOTE: HSYNC is used for C512SS and C8SS panels.

Bit 6-4 **HSYNC Bits:** These bits are loaded into the HSYNC Delay Counter to delay the HSYNC Signal from the VGA controller to the panel. MCLK is the clock for the counter. The value loaded into these bits represents the number of pipeline stages the pixel data will traverse through before being output to the panel. By setting the correct value, HSYNC and panel data should coincide in time with each other.

Bit 3 **MOD Clock Source:** If set, then line clock is selected as the source to the modulation counter clock. When reset, this bit selects the frame clock as the clock to the modulation counter instead of line clock.

Bit 2-0 **Data Source Select Bits:** Used to select internal data path to panel interface.

2	1	0	Description
0	1	1	Color Palette (C512SS, C4096SS)†
1	0	0	Green Frame Rate (M2DD, M2SS)†
1	0	1	Color Frame Rate (C8SS, C8SSI, C8SSI+CL1, C8DD)†
Others			RESERVED

NOTE: † Refer to the glossary for explanation of these terms.

6.33 VGA Interface Register: VGAI

I/O Port Address: 3C5

Index: F6

Read/Write Protection Bit: INTSEL or ALLSEL

Bit	Description	Access	Reset State
7	Sleep Port Address Register	R/W	0
6	Enable RAMDAC Border Read/Write	R/W	0
5	Disable Analog Sense	R/W	0
4	MCLK invert	R/W	0
3	Display Type Select Bit 1	R/W	0
2	Display Type Select Bit 0	R/W	0
1	VGA Select Bit 1	R/W	0
0	VGA Select Bit 0	R/W	0

Bit 7 — **Sleep Port Address Register:** When set, 46E8 is selected as the active sleep register. When reset, 3C3 is selected as the active sleep register.

Bit 6 — **Enable RAMDAC Border Read/Write:** Controls access to RAMDAC registers. See RAMDAC I/O Port Summary Table for details.

Bit 5 — **Disable Analog Sense:** If reset, then any read at 03C2 will allow an output to the SENSE pad. If set, then SENSE is always off.

Bit 4 — **MCLK Invert:** Setting this pin inverts the MCLK used in the LCD portion of CL-GD6340. The MCLK to the RAMDAC is not inverted.

Bit 3-2 — **Display Type Select Bits:** When set, these bits cause power to be supplied to the CRT and LCD sections of the chip. This allows the power-down of specific modules but DOES NOT effect Power Sequencing. (See ERA7 for Power Sequencing information)

3	2	Description
0	0	CRT and panel sections are both off — DAC is off
0	1	LCD section is turned on — DAC is off
1	0	CRT section is turned on
1	1	LCD and CRT sections are both on

Bit 1-0 — **VGA Select Bits:** These bits select a specific value to be loaded into the delay display enable counter. This value represents the total time to delay the internal Display Enable.

1	0	Description
0	0	CL-GD610/620 and CL-GD6410
0	1	RESERVED
1	0	RESERVED
1	1	RESERVED

7. ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Storage temperature ..... -65° C to + 150° C

Ambient operating temperature ..... 0° C to 70° C

Input static discharge protection ..... 2000 Volts

Humidity ..... 20 to 95 Percent

Voltage on any pin with respect to ground ..... (Ground -0.5 Volts) to (V_{CC} + 0.5 Volts)

Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

7.2 DC Characteristics (Digital)

(V_{CC} = 5V + 5%, TA = 0°C to 70°C)

Symbol	Parameter	MIN	TYP	MAX	Conditions
V_{CC}	Power Supply Voltage	4.5V		5.5V	Normal operations
V_{IL}	Input Low Voltage	-0.5V	0.0V	0.8V	
$V_{IH\ TTL}$	Input High Voltage	2.0V	5.0V	V_{CC} + 0.5V	
$V_{IH\ CMOS}$	Input High Voltage	3.0V		V_{CC} + 0.5V	I_{OH} = 400 uA
$V_{OL\ CMOS}$	Output Low Voltage			0.4V	I_{OLC} = 3.2 mA
$V_{OH\ CMOS}$	Input High Voltage	3.5V		V_{cc}	I_{OH} = 400 uA
$I_{CC\ nom\ D}$	Digital Operating Supply Current		80 mA	145 mA	at 25 MHz, 5V
$I_{CC\ nom\ A}$	Analog Operating Supply Current		40 mA	80 mA	at 25 MHz, 5V
$I_{CC\ pd\ D}$	Digital Power-Down Mode current		4 mA	6 mA	at 25 MHz, 5V
$I_{CC\ pd\ A}$	Analog Power-Down Mode current		0.1 uA	1uA	at 25 MHz, 5V
$I_{CC\ Stby\ D}$	Digital Standby Mode current		16 mA	25 mA	at 25 MHz, 5V
$I_{CC\ Stby\ A}$	Analog Standby Mode current		0.1 uA	1 uA	at 25 MHz, 5V
I_L	Input Leakage	-10 uA		10 uA	$0 < V_{in} < V_{cc}$
C_{IN}	Input Capacitance			10 pF	
C_{OUT}	Output Capacitance			10 pF	

NOTES:

1) I_{OH} max for R, G, B = 25 mA source.

2) I_{CCpd} and I_{CCStby} measured with a quiescent bus.

3) I_{OL} MAX for BHSYNC, BVSYNC, BLFS, BMOD, BCLCLK, BSHCLK, BRCLK, and BENRL are 8 mA.

7.3 CL-GD6340 DC Specifications (RAMDAC)

(V_{CC} = 5V ± 10%, TA = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Conditions
V_{CC}/AV_{DD}	Power Supply Voltage	4.50	5.50	V	Normal Operations
I_{REF}	DAC Reference Current	-6.7	-10	mA	Notes 1 and 2
I_{DD}	Operating Supply Current		100.0	mA	Note 3

NOTES:

1) Reference currents below the minimum specified may cause the analog output to become invalid.
2) The pixel clock frequency must be stable for a period of 20 µS after power-up before proper device operation.
3) I_{DD} is dependent upon the digital output loading and pixel clock rate. The value specified is with the outputs unloaded and the pixel clock frequency equal to 33 MHz.

7.4 AC Specifications

The following timing information assumes that all outputs will drive one Schottky TTL load in parallel with 50 pF and all inputs are at TTL level. The MIN and MAX timings are those conforming to the operating ranges of a power supply voltage of 5V ± 10% and an ambient temperature of 0°C to 70°C.

7.4.1 Index of Timing Information

Table 7–1. I/O Read Cycle Timing

Symbol	Parameter	MIN	MAX	Unit
t_{ASBI}	Address setup before IORD* active	50	-	ns
t_{IPW}	IORD* pulse width	115	-	ns
t_{DVAI}	Data valid after IORD* active	-	90	ns
t_{DHAI}	Data valid hold after IORD* inactive	0	-	ns
t_{IRAZ}	IORD* active to Data low Z	0	-	ns
t_{IRIZ}	IORD* inactive to Data high Z	-	30	ns
t_{ADT}	Address hold time after IORD* inactive	0	-	ns
t_{AIS}	AEN inactive setup before IORD* active	0	-	ns
t_{AIH}	AEN inactive hold time after IORD* inactive	0	-	ns
t_{IIN}	IORD* inactive any command	80	-	ns

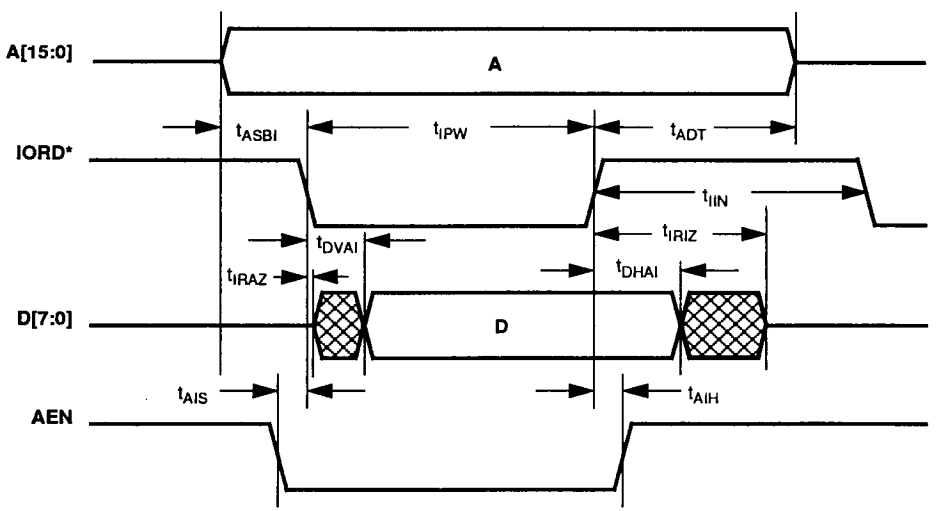


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Figure 7–1. I/O Read Cycle Timing

Table 7–2. I/O Write Cycle Timing

Symbol	Parameter	MIN	MAX	Unit
t_{ASBA}	Address setup before IOWR* active	50	-	ns
t_{IOP}	IOWR* pulse width	115	-	
t_{DSI}	Data setup time before rising edge of IOWR*	90	-	ns
t_{DHT}	Data hold time after rising edge of IOWR*	0	-	ns
t_{ADI}	Address hold time after IOWR* inactive	0	-	ns
t_{AES}	AEN inactive setup time before IOWR* active	0	-	ns
t_{AEH}	AEN inactive hold time after IOWR* inactive.	0	-	ns
t_{IIC}	IOWR* inactive to any command	80	-	ns

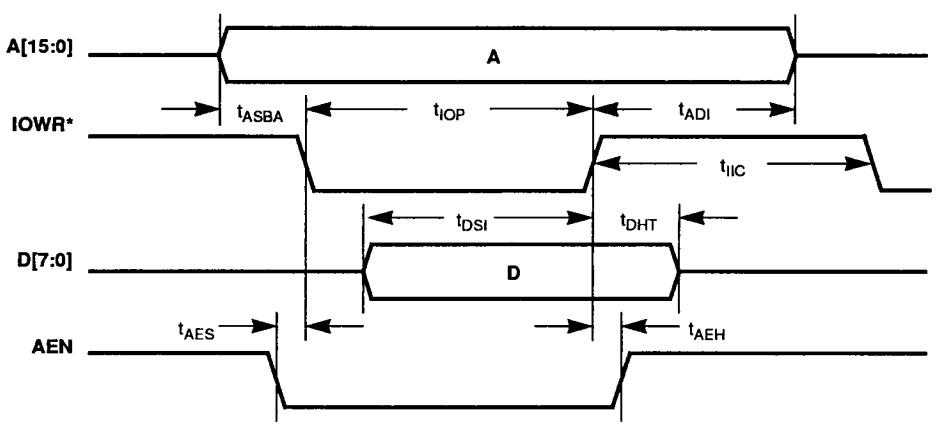

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Figure 7–2. I/O Write Cycle Timing

Table 7–3. Input Timing

Symbol	Parameter	MIN	MAX	Unit
t_{BTT}	MCLK transition time		2	ns
t_{BLT}	MCLK low time	5		ns
t_{BHT}	MCLK high time	5		ns
t_{MDS}	P0-P7 data setup to MCLK	3		ns
t_{MDH}	P0-P7 data hold from MCLK	3		ns
t_{MBS}	BLANK* setup time to MCLK	3		ns
t_{MBH}	BLANK* hold time from MCLK	3		ns
t_{MHS}	HSYNC setup to MCLK	5		ns
t_{MHH}	HSYNC hold from MCLK	5		ns
t_{MDS}	DE setup to MCLK	5		ns
t_{MDH}	DE hold from MCLK	5		ns

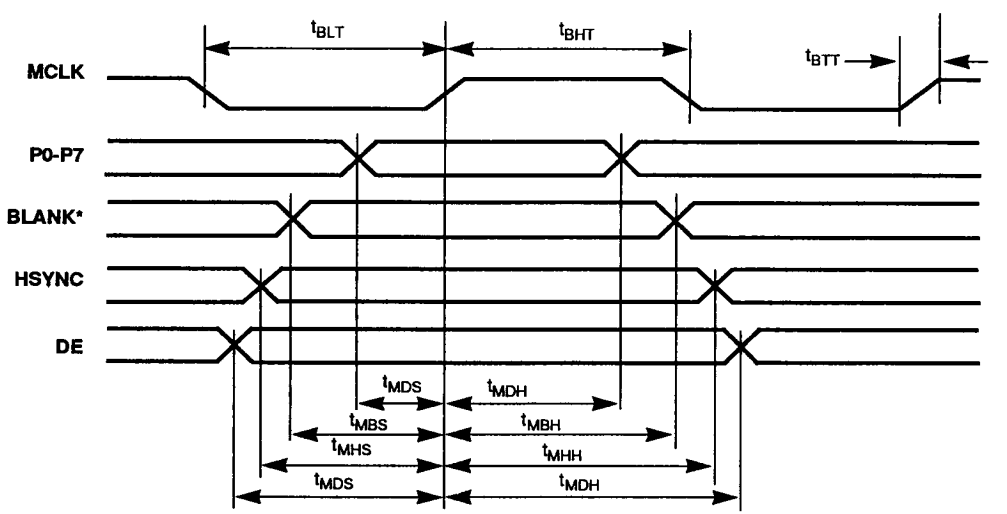

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Figure 7–3. Input Timing

Table 7–4. CRT Timing

Symbol	Parameter	MIN	MAX	Unit
t_{BHVS}	HSYNC and VSYNC setup to MCLK	5		ns
t_{BHVH}	HSYNC and VSYNC hold from MCLK	5		ns
* t_{ARF}	Analog R,G,B rise and fall time		8	ns
** t_{AST}	Analog R,G,B settling time	3	20	ns
t_{BAD}	Analog R,G,B valid delay from MCLK		30	ns

NOTES:

* Measured between 10% and 90%.

** Measured from 50% of final value to 1/2 LSB variation.

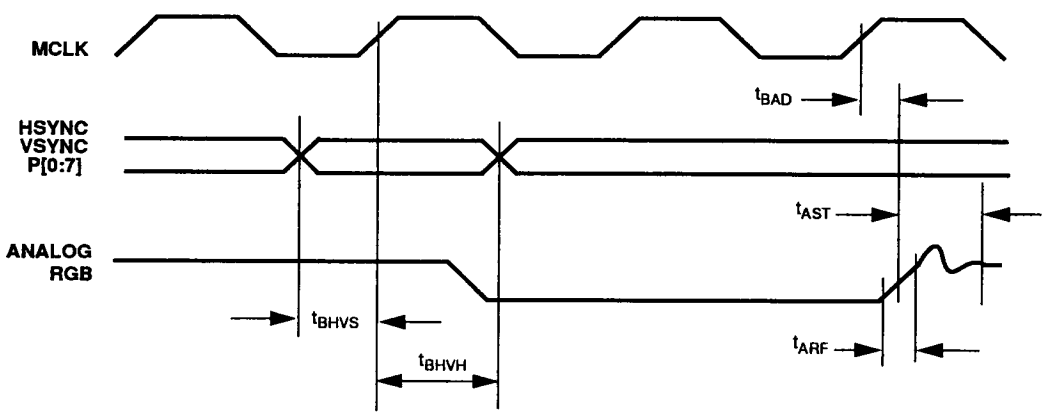

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Figure 7–4. CRT Timing

Table 7–5. Frame-Accelerator Cycle Timing

Symbol	Parameter	MIN	MAX	Unit
t_{FRS}	Row Address valid setup to FRRAS* active	2 Tc		ns
t_{FRH}	Row Address hold from FRRAS* active	0.5 Tc		ns
t_{FOD}	Read Data delay from FROE* active	5		ns
t_{FCS}	Column Address valid setup to FRCAS* active	0.5 Tc -5		ns
t_{FCH}	Column Address valid hold after FRCAS* active	0.5 Tc -5		ns
t_{FODH}	Read Data hold after FROE* inactive	2	0.5 Tc	ns
t_{FODS}	Read Data setup to FROE* inactive	5		ns
t_{FCOS}	FRCAS * active delay to FROE* active	0.5 Tc		ns
t_{FOE}	FROE* active pulse width	1 Tc		ns
t_{FWS}	Write Data setup to FRWE* active	0.5 Tc -10		ns
t_{FWH}	Write Data hold from FRWE* inactive	0.5 Tc -5	0.5 Tc + 5	ns
t_{FWA}	FRWE* active time	0.5 Tc -5	0.5Tc + 5	ns
t_{FCC}	FRCAS* cycle time	4 Tc		ns
t_{FCI}	FRCAS* inactive time	1 Tc -5		ns
t_{FCA}	FRCAS* active time	3 Tc -5		ns
t_{FRI}	FRRAS* inactive time	12 Tc -5		ns
t_{FRA}	FRRAS* active time	641 Tc -5		ns

NOTE: Tc = MCLK period

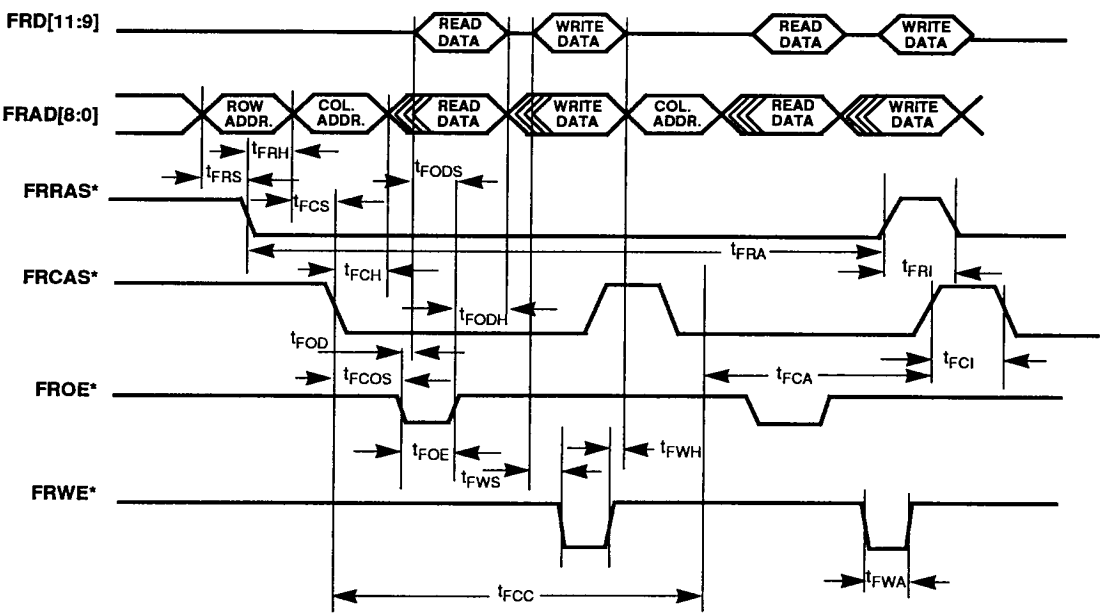

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Figure 7–5. Frame-Accelerator Interface Timing

Table 7–6. Monochrome LCD Interface Timing

Symbol	Parameter	MIN	MAX	Unit
t_{LPW}	BCLCLK pulse width	1		Tc
t_{FLS}	BSHCLK low setup to BCLCLK	Tc + 20		ns
t_{FCT}	BSHCLK cycle time	Tc - 10		ns
t_{FHT}	BSHCLK high time	0.5 Tc -10		ns
t_{FLT}	BSHCLK low time	0.5 Tc -10		ns
t_{FFT}	BSHCLK fall time		5	ns
t_{FRT}	BSHCLK rise time		5	ns
t_{FLH}	BSHCLK low hold time after BCLCLK low	Tc -20		ns
t_{VDS}	Video data setup time	0.5 Tc -5		ns
t_{VDH}	Video data hold time	0.5 Tc -5		ns
t_{LHH}	BLFS high hold time after BCLCKL low	Tc		ns
t_{LSL}	BLFS high setup to BCLCLK low	Tc		ns
t_{MDL}	BMOD delay from BCLCLK low		30	ns

NOTE: Tc = MCLK period x 4

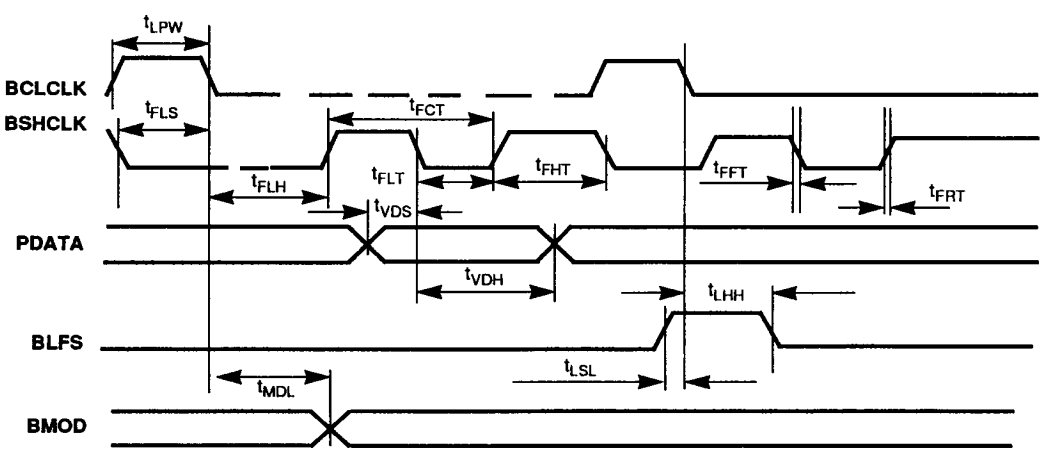

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Figure 7–6. Monochrome LCD Interface Timing

Table 7–7. Type 1 Color LCD Interface Timing

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{KP}	BCLCLK pulse width	1			Tc
t_{KLK}	BSHCLK low setup to BCLCLK		18		Tc
t_{KC}	BSHCLK cycle time	5 Tc -10		6 Tc	ns
t_{KH}	BSHCLK high time		2 Tc -10		ns
t_{KF}	BSHCLK fall time			5	ns
t_{KR}	BSHCLK rise time			5	ns
t_{KHL}	BSHCLK low hold time after BCLCLK low		143 Tc		ns
t_{VDS}	Video data setup time	2 Tc -15 ns	2 Tc		ns
t_{VDH}	Video data hold time	3 Tc -15 ns	3 Tc		ns
t_{LHK}	BLFS high hold time after BCLCKL low		138 Tc		ns
t_{LSK}	BLFS high setup to BCLCLK low		7.5 Tc		ns
t_{MDL}	BMOD delay from BCLCLK low		30		ns

NOTE: Tc = MCLK period
Type 1 = Panels with direct connection to column- and row-driven latches; similar to monochrome LCD interface.

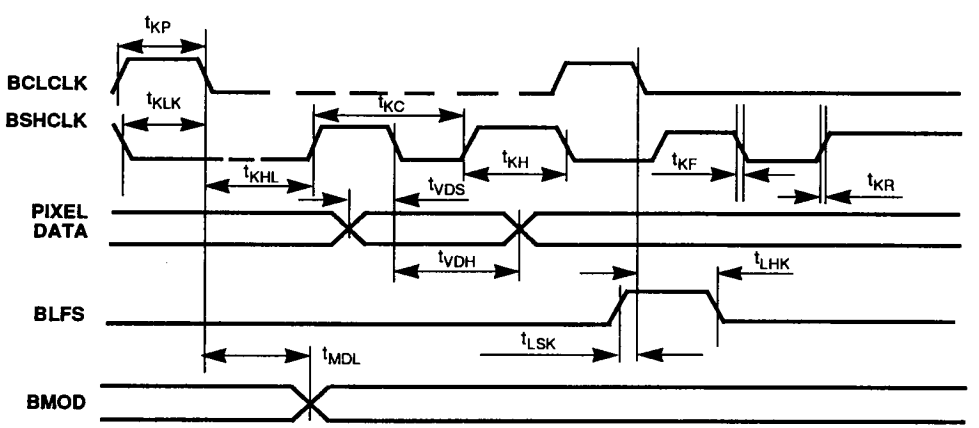

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Figure 7–7. Type 1 Color LCD Interface Timing

Table 7–8. Type 2 Color LCD Interface Timing

Symbol	Parameter	MIN	MAX	Unit
t_{KP}	BCLCLK pulse width	1600		T_C
t_{KC}	BSHCLK cycle time	$0.95T_C$	$1.05T_C$	T_C
t_{KH}	BSHCLK high time	$0.5T_C$-5	$0.5T_{C+}$5	T_C
t_{KL}	BSHCLK low time	$0.5T_C$-5	$0.5T_C$+5	T_C
t_{KF}	BSHCLK fall time		10	ns
t_{KR}	BSHCLK rise time		10	ns
t_{VDS}	Video data setup time	10		ns
t_{VDH}	Video data hold time	10		ns
t_{LHK}	BLFS active hold time after BCLCLK low	2		T_C
t_{LSK}	BLFS active setup to BCLCLK low	4		T_C
t_{DDS}	Panel Data valid to DEN active	0	5	ns
t_{DDH}	DEN inactive to BSHCLK low	10		ns
t_{BSD}	DEN active to BSHCLK low	15		ns
t_{BSH}	BSHCLK low to DEN inactive	10		ns
t_{BDD}	BLFS inactive to valid Data	0		ns
t_{BP}	BLFS pulse width	1600		T_C

NOTE: T_C = MCLK period

Type 2 = Panels with direct connection to VSYNC and HSYNC signals; similar to CRT interface.

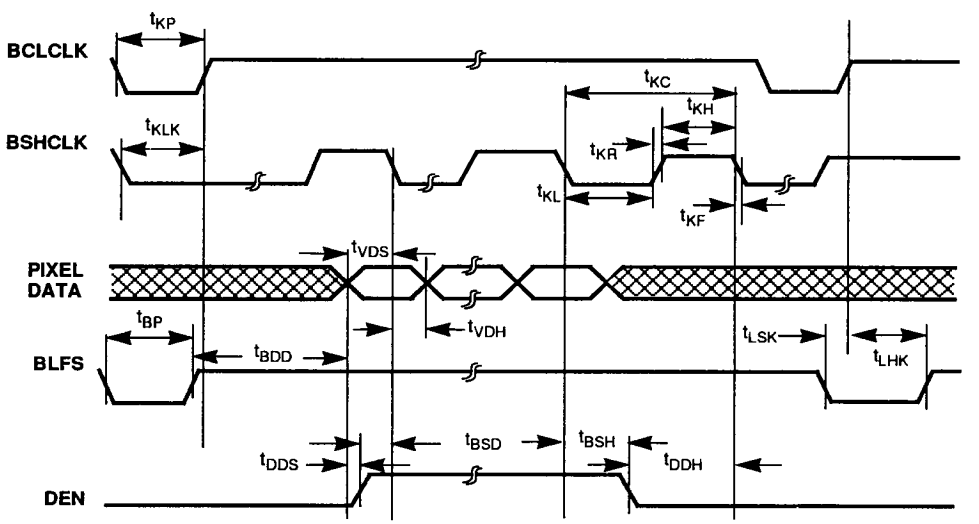

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Figure 7–8. Type 2 Color LCD Interface Timing

8. VGA CONTROLLER–TO–CL-GD6340 INTERFACES

8.1 CL-GD610/620-C–to–CL-GD6340 Interface

The CL-GD610/620-C is a VGA two-chip solution with LCD logic, and is capable of driving grayscale LCDs. However, for color LCDs the CL-GD6340 is needed. To start the CL-GD6340, DE from CL-GD610/620-C is decoded. This decoded DE is then delayed according to the settings in register 3C5.F6[1:0]. See SimulSCAN for CL-GD610/620-C to CL-GD6340 for additional details.

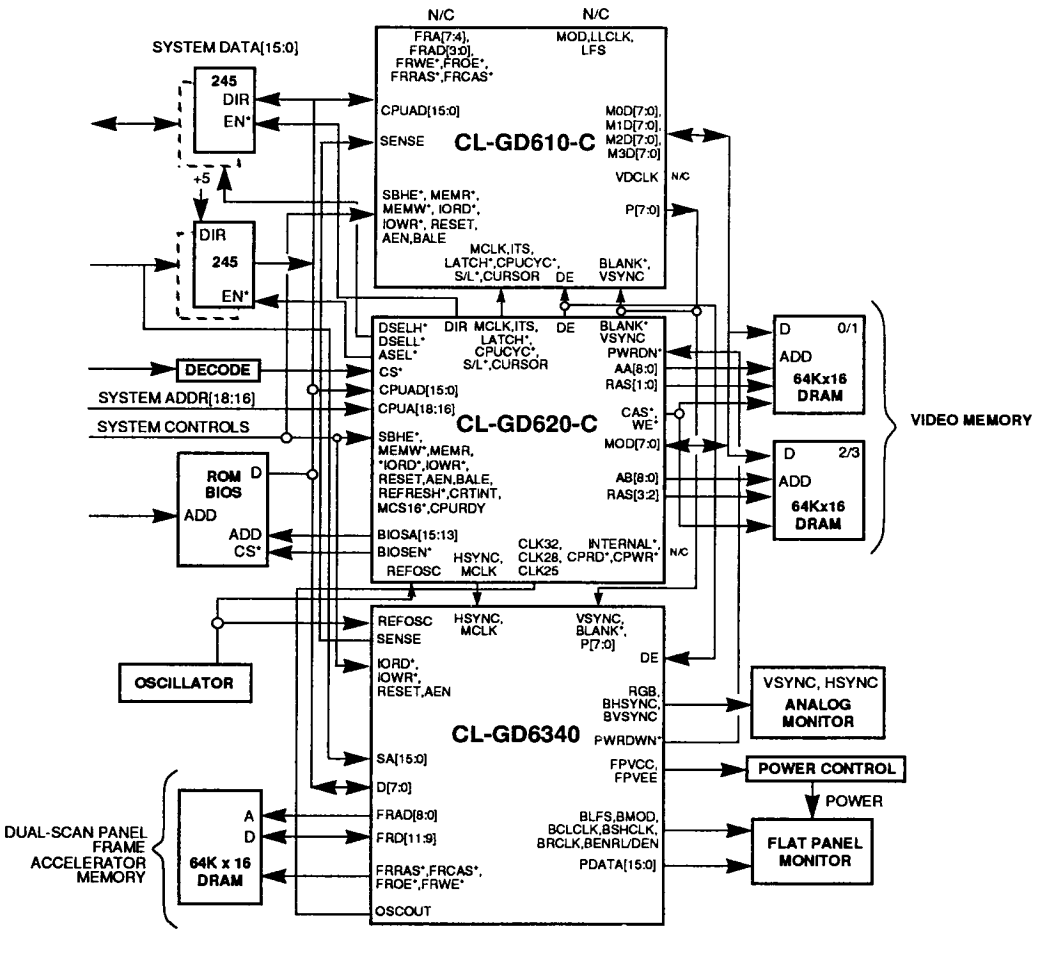

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Figure 8–1. CL-GD6340–to–CL-GD610/620-C System Block Diagram

8.2 CL-GD6340–to–CL-GD6410 Interface

The CL-GD6340 connects to the CL-GD6410 as if it were an external RAMDAC. Connections to system address, data lines, and CRT control signals are needed.

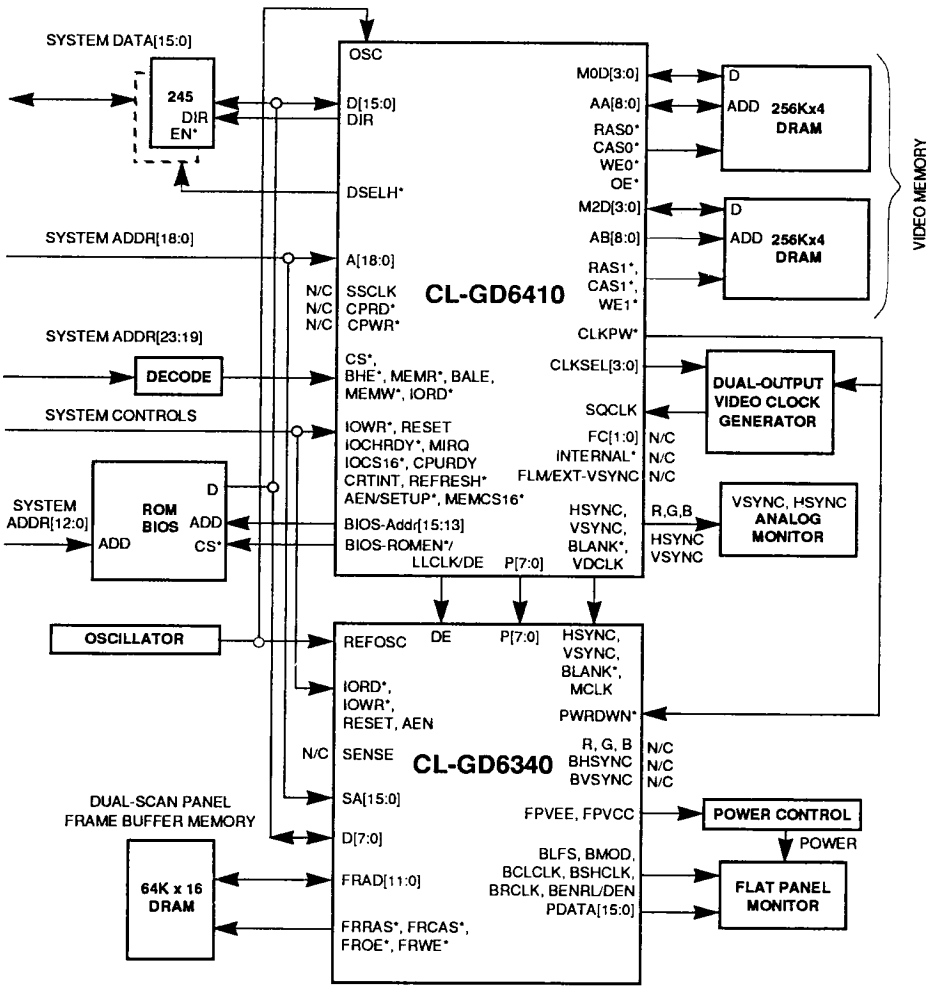

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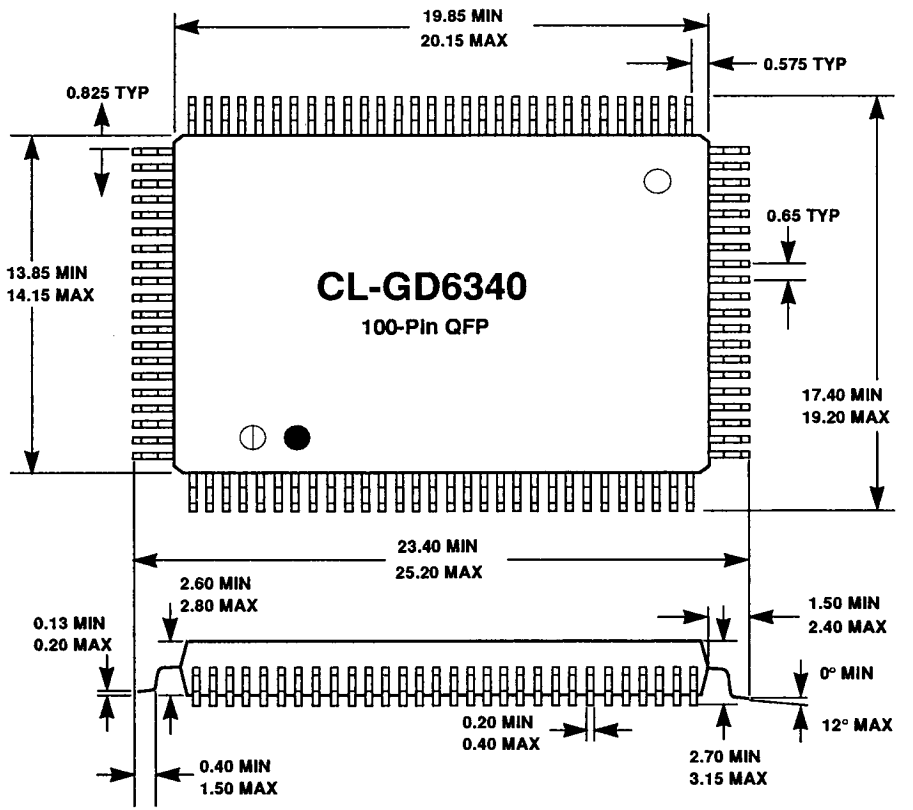
Figure 8–2. CL-GD6340–to–CL-GD6410 System Block Diagram

9. PACKAGE INFORMATION

9.1 100-Pin QFP Dimensions

The CL-GD6340 is provided in an EIAJ-standard, 100-pin plastic Quad Flat Pack (QFP).



NOTE: All measurements (except degrees of arc) are in millimeters.

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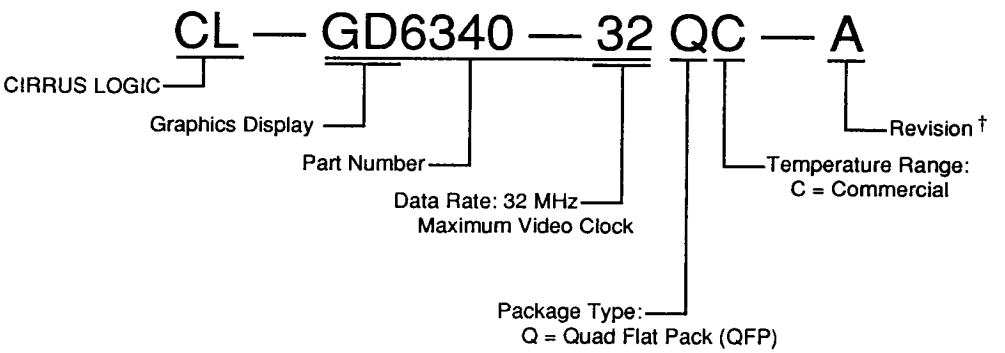
Figure 9–1. 100-Pin Plastic Quad Flat Pack Dimensions

10. ORDERING INFORMATION

10.1 Numbering Guide



† Contact Cirrus Logic for up-to-date information on revisions.

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Figure 10–1. Cirrus Logic Ordering Information

Glossary

C4096SS	**4096-Color, Single-panel, Single-scan, active matrix**
C512SS	**512-Color, Single-panel, Single-scan, active matrix**
C8DD	**8-Color, Dual-panel, Dual-scan**
C8SS	**8-Color, Single-panel, Single-scan**
C8SSI	**8-Color, Single-panel, Single-scan, Interleaved**
C8SSI-8 bit	**8-Color, Single-panel, Single-scan, 8-bit Interleaved**
C8SSI-16 bit	**8-Color, Single-panel, Single-scan, 16-bit Interleaved**
C8SSI+CL1	**8-Color, Single-panel, Single-scan, Interleaved with special line clock**
M2DD	**Monochrome, 2-shade, Dual-panel, Dual-scan, STN**
M2SS	**Monochrome, 2-shade, Single-panel, Single-scan, active matrix**

INDEX

INDEX *(cont.)*

Direct Sales Offices

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N. CALIFORNIA
San Jose
TEL: 408/436-7110
FAX: 408/437-8960

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The Company

Cirrus Logic, Inc., produces high-integration peripheral controller circuits for mass storage, graphics, and data communications. Our products are used in leading-edge personal computers, engineering workstations, and office automation equipment.

The Cirrus Logic formula combines proprietary S/LA™† IC design automation with system design expertise. The S/LA design system is a proven tool for developing high-performance logic circuits in half the time of most semiconductor companies. The results are better VLSI products, on-time, that help you win in the marketplace.

Cirrus Logic's fabless manufacturing strategy, unique in the semiconductor industry, employs a full manufacturing infrastructure to ensure maximum product quality, availability and value for our customers.

Talk to our systems and applications specialists; see how you can benefit from a new kind of semiconductor company.

† U.S. Patent No. 4,293,783

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