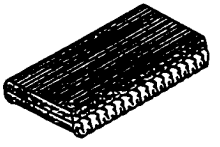
131,072-WORD X 8-BIT HIGH SPEED CMOS STATIC RAM

PRELIMINARY

DESCRIPTION

The CXK581120J is a high speed 1M-bit CMOS static RAM organized as a 131,072-word by 8-bit array. It operates at 12/15/20ns access time from a single 5V power supply, utilizing center-ground/power pin architecture.

CXK581120J
32 PIN SOJ
(PLASTIC)



FEATURES

- **High speed, low power consumption:**

	Access time (Max.)	Power consumption (Typ., Cycle = Min.)
CXK581120J- 12	12ns	690mW
CXK581120J- 15	15ns	550mW
CXK581120J-20	20ns	500mW

- **Single +5V power supply**
- **Fully static memory. No clock or timing strobe required.**
- **Equal access and cycle time.**
- **Directly TTL compatible: All inputs and outputs.**
- **Common data input and output: three state output.**
- **Available in a 32 pin 400mil SOJ package.**

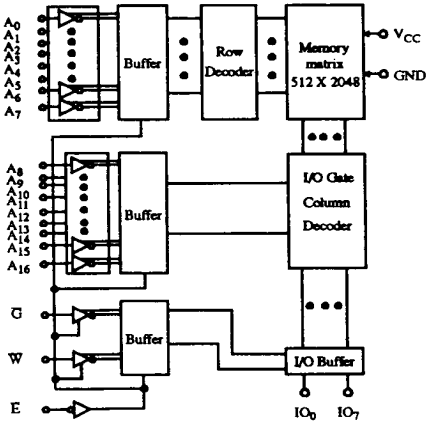
FUNCTION

131,072-word x 8-bit Static RAM

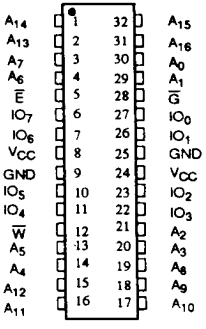
PIN DESCRIPTION

SYMBOL	DESCRIPTION
A_0 to A_{16}	Address input
IO_0 to IO_7	Data input/output
$\overline{E}$	Chip enable input
$\overline{W}$	Write enable input
$\overline{G}$	Output enable input
V_{CC}	+5V power supply
GND	Ground

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C, GND = 0V)

ITEM	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to V_{CC}+0.5	V
Input and output voltage	$V_{I/O}$	-0.5 to V_{CC}+0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	T_{OPR}	0 to +70	°C
Storage temperature	T_{STG}	-55 to +150	°C
Soldering temperature ● time	T_{SOLDER}	260 ● 10	°C ● sec

TRUTH TABLE

MODE	$\overline{E}$	$\overline{G}$	$\overline{W}$	IO_{0-7}	POWER
Not selected	H	X	X	Hi-Z	I_{SB1},I_{SB2}
Output disable	L	H	H	Hi-Z	I_{CC}
Read	L	L	H	Data out	I_{CC}
Write	L	X	L	Data in	I_{CC}

Note: X ■ H OR L

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DC RECOMMENDED OPERATING CONDITIONS

(T_A = 0 to +70°C, GND = 0V)

ITEM		SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	-12/15	V_{CC}	4.75	5.0	5.25	V
	20		4.5	5.0	5.5	V
Input high voltage		V_{IH}	2.2	—	V_{CC}+0.3	V
Input low voltage		V_{IL}	-0.3	—	0.8	V

ELECTRICAL CHARACTERISTICS

• DC AND OPERATING CHARACTERISTICS

ITEM	SYMBOL	TEST CONDITIONS			MIN.	TYP*	MAX.	UNIT
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}			-1	—	1	uA
Output leakage current	I_{LO}	$V_{I/O}$ = GND to V_{CC}, $\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH} or $\overline{W}$ = V_{IL}			-1	—	1	uA
Average operating current	I_{CC}	CYCLE = t_{MIN} DUTY = 100% IOUT = 0mA $\overline{E}$ = V_{IL} VIN = V_{IH} or V_{IL}	- 12	Write	—	—	250	mA
				Read	—	—	180	
			- 15	Write	—	—	220	
				Read	—	—	150	
			- 20	Write	—	—	200	
				Read	—	—	140	
Standby current	I_{SB1}	$\overline{E} \geq V_{CC}$-0.2V $V_{IN} \geq V_{CC}$-0.2V or $V_{IN} \leq 0.2V$			—	—	10	mA
	I_{SB2}	CYCLE = t_{MIN}, DUTY CYCLE = 100%, $\overline{E}$ = V_{IH}, V_{IN} = V_{IL} or V_{IH}			—	25	40	mA
Output high voltage	V_{OH}	I_{OH} = -4.0mA			2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0mA			—	—	0.4	V

* NOTE: V_{CC} = 5V, T_A = 25°C

I/O CAPACITANCE *

(T_A = 25°C, f = 1MHz)

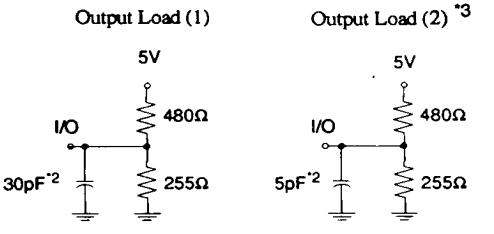
ITEM	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0V	—	5	pF
Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

* NOTE: This parameter is sampled and is not 100% tested

• AC CHARACTERISTICS AND TEST CONDITIONS (T_A = 0 to +70°C, VCC = 5V ± 5% *1)

ITEM	CONDITIONS
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	t_R = 3nS
Input fall time	t_F = 3nS
Input and output reference level	1.5V
Output load conditions	Figure 1

FIGURE 1



*1 V_{CC}=5V ±10% for CXK581120J-17
*2 Including scope and jig capacitance
*3 For t_{LZ}, t_{HZ}, t_{OHZ}, t_{OLZ}, t_{OW}, t_{WHZ}

READ CYCLE

ITEM	SYMBOL	- 12		- 15		- 20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read cycle time	t_{RC}	12	—	15	—	20	—	ns
Address access time	t_{AA}	—	12	—	15	—	20	ns
Chip enable access time	t_{CO}	—	12	—	15	—	20	ns
Output enable to output valid ($\overline{G}$)	t_{OE}	—	6	—	7	—	8	ns
Output hold from address change	t_{OH}	2	—	2	—	3	—	ns
Chip enable to output in low Z ($\overline{E}$)	t_{LZ}*	3	—	3	—	3	—	ns
Output enable to output in low Z ($\overline{G}$)	t_{OLZ}*	2	—	2	—	2	—	ns
Chip disable to output in high Z ($\overline{E}$)	t_{HZ}*	—	6	—	7	—	8	ns
Output disable to output in high Z ($\overline{G}$)	t_{OHZ}*	—	6	—	7	—	8	ns
Chip enable to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t_{PD}	—	12	—	15	—	20	ns

WRITE CYCLE

ITEM	SYMBOL	- 12		- 15		- 20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write cycle time	t_{WC}	12	—	15	—	20	—	ns
Address valid to end of write	t_{AW}	10	—	12	—	15	—	ns
Chip enable to end of write	t_{CW}	10	—	12	—	15	—	ns
Data to write time overlap	t_{DW}	6	—	8	—	12	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	10	—	12	—	15	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*	3	—	3	—	3	—	ns
Write to output in high Z	t_{WHZ}*	—	6	—	7	—	9	ns

* Transition is measured ±200mV from steady voltage with specified loading in Fig. 1-(2). This parameter is sampled and is not 100% tested.

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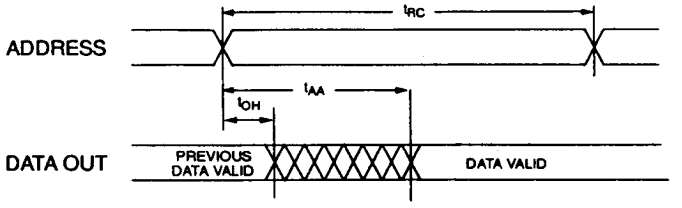
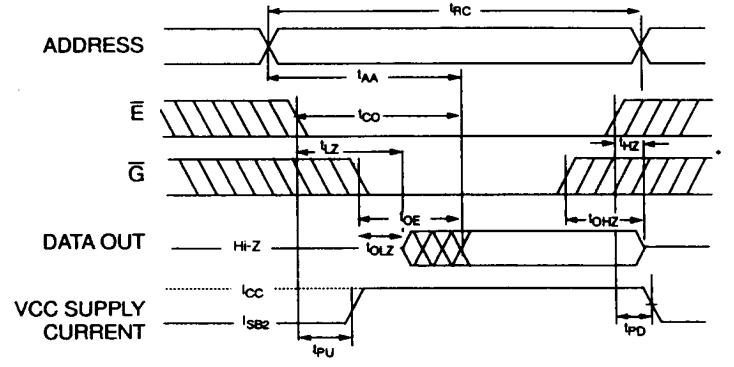
TIMING WAVEFORMS

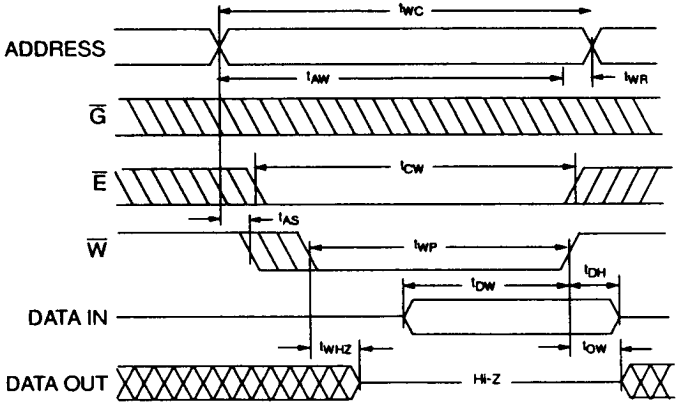
- **READ CYCLE (1): $\overline{E} = \overline{G} = V_{IL}$, $\overline{W} = V_{IH}$**



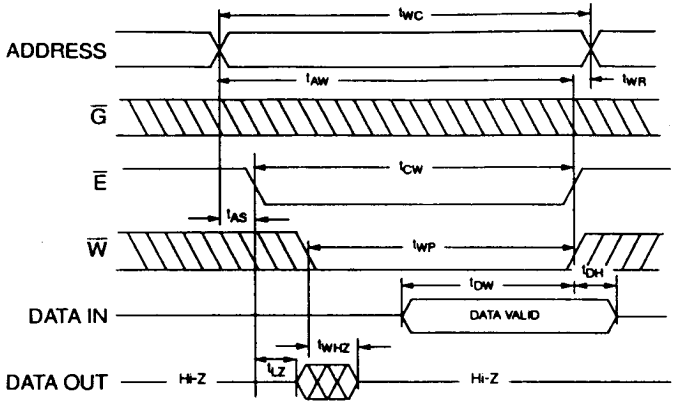
- **READ CYCLE (2): $\overline{W} = V_{IH}$**



- **WRITE CYCLE (1): $\overline{W}$ CONTROL**



- **WRITE CYCLE (2): $\overline{E}$ CONTROL**



Note: 1) Write occurs during the low overlap of $\overline{E}$ and $\overline{W}$.

2) During t_{WHZ}-t_{LZ}, the I/O pins are in the output state during which data input signals of the opposite phase to the output must not be applied.

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