CYPRESS SEMICONDUCTOR

16,384 x 16 Static R/W Cache Storage Unit

Features

- **Optimized for use with RISC processors, including SPARC®**
- **Address and $\overline{WE}$ registers**
- **CMOS for optimum speed/power**
- **High speed**
  — 18 ns
- **Data-in and Data-out latches**
- **Self-timed write**
- **Common I/O**
- **TTL-compatible inputs and outputs**

Functional Description

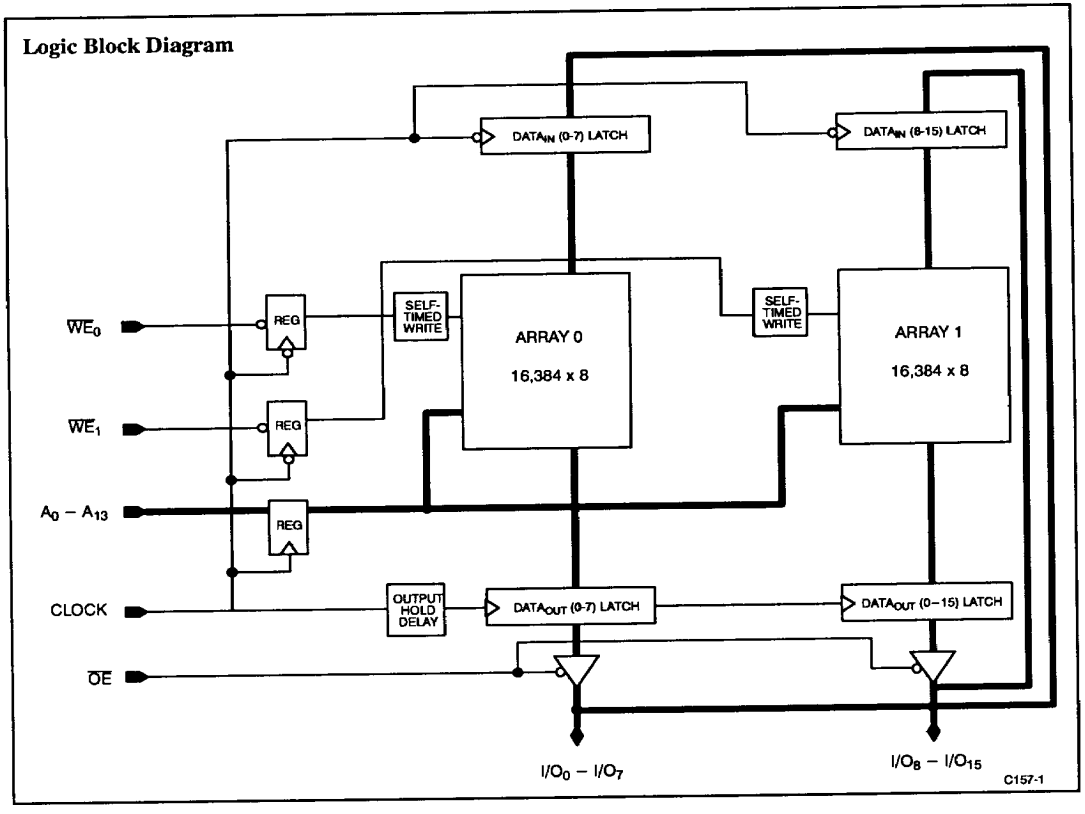
The CY7C157A cache storage unit is a high-performance CMOS static RAM organized as 16,384 x 16 bits. It is optimized for use as a high-speed cache memory device with RISC processors such as the CY7C600 SPARC® family of devices. The CY7C157A employs common I/O architecture, a self-timed byte write mechanism, and on-chip address update latches.

Reading the device is accomplished by taking $\overline{WE}$ HIGH and $\overline{OE}$ LOW. On the rising edge of CLOCK, addresses A_0 through A_{13} are loaded into the input registers. A memory access occurs, and data is held after a read cycle beyond the next rising edge of CLOCK in order to meet the hold-time requirements of the microprocessor.

To write the device correctly, $\overline{OE}$ must be taken HIGH. If the falling edge of CLOCK samples either or both of $\overline{WE_0}$ or $\overline{WE_1}$ LOW, a self-timed byte write mechanism is triggered. Data is written from the data-in latch into the memory array at the corresponding address.

Note that the $\overline{OE}$ signal must be HIGH for a proper write because the $\overline{WE_0}$ and $\overline{WE_1}$ signals do not three-state the outputs.

Logic Block Diagram



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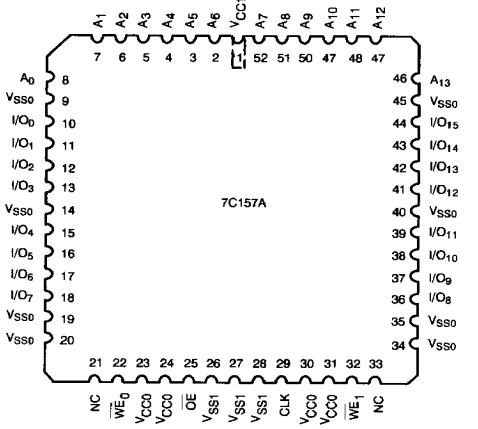
Pin Timing Cross Reference

Pin Name	Timing Reference	Description
Clock	C	Clock Inputs
$A_0 - A_{13}$	A	Address Inputs
$I/O_0 - I/O_{15}$ (Input)	D	Data Inputs
$I/O_0 - I/O_{15}$ (Output)	Q	Data Outputs
$\overline{WE_0}$, $\overline{WE_1}$, $\overline{WE_X}$	W	Write Enable
$\overline{OE}$	G	Output Enable

Pin Diagram

LCC and PLCC
Top View



C157-2

Selection Guide

		7C157A–18	7C157A–20	7C157A–24	7C157A–33
Maximum Clock to Output (ns)	Commercial	18	20	24	33
	Military			24	33
Maximum Output Enable to Output Time (ns)	Commercial	7	8	10	15
	Military			10	15
Maximum Current (mA)	Commercial	350	325	300	250
	Military			325	275

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage[1] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 50 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch–Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	− 55°C to +125°C	5V ± 10%

Notes:

1. V_{IL} (min.) = − 3.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature

Electrical Characteristics Over the Operating Range[3]

Parameters	Description	Test Conditions		7C157A–18 Min.	7C157A–18 Max.	7C157A–20 Min.	7C157A–20 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–10	+10	–10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–10	+10	–10	+10	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			–350		–350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		350		325	mA
			Mil					

Parameters	Description	Test Conditions		7C157A–24 Min.	7C157A–24 Max.	7C157A–33 Min.	7C157A–33 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–10	+10	–10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–10	+10	–10	+10	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			–350		–350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		300		250	mA
			Mil		325		275	

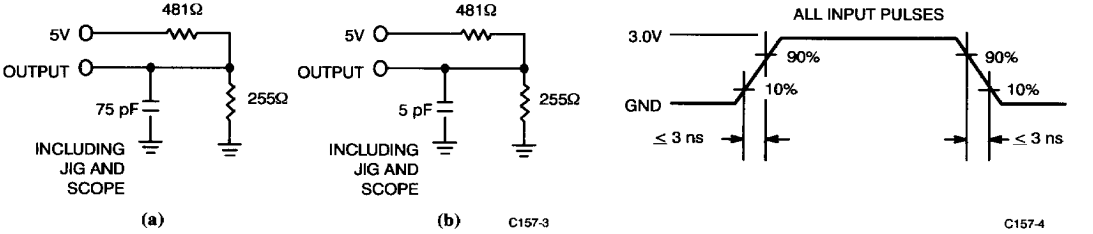
Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	pF

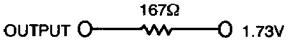
Notes:

3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at a time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THEVENIN EQUIVALENT

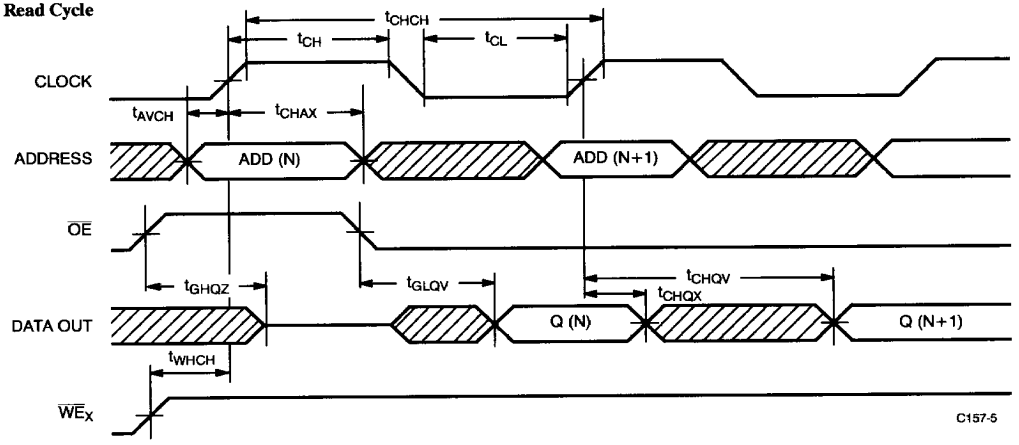


Switching Characteristics Over the Operating Range[6]

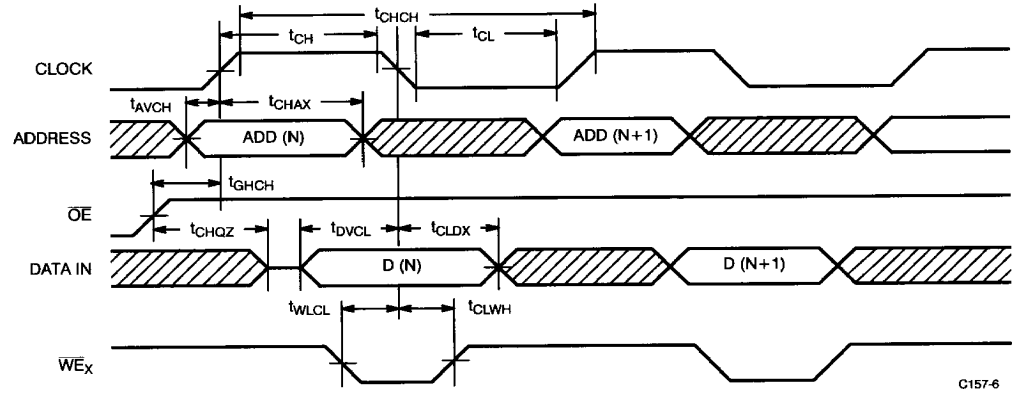
Parameters	Description	7C157A–18		7C157A–20		7C157A–24		7C157A–33		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE[7,8]										
t_{CHCH}	Clock Cycle Time	22		25		30		40		ns
t_{CH}	Clock HIGH Time	10		11		13		18		ns
t_{CL}	Clock LOW Time	10		11		13		18		ns
t_{CHQV}	Clock HIGH to Output Valid		18		20		24		33	ns
t_{CHQX}	Output Data Hold	5		5		5		5		ns
t_{WHCH}	$\overline{WE}_x$ HIGH to Next Clock HIGH	2		2		2		3		ns
t_{GLQV}	$\overline{OE}$ LOW to Output Valid		7		8		10		15	ns
t_{GHQZ}	$\overline{OE}$ HIGH to Output Tristate[9]		7		8		10		15	ns
t_{GHCH}	$\overline{OE}$ HIGH to Next Clock HIGH	7		7		7		7		ns
t_{AVCH}	Address Set-Up	2		2		2		3		ns
t_{CHAX}	Address Hold	5		6		6		6		ns
WRITE CYCLE[10]										
t_{CHCH}	Clock Cycle Time[11]	22		25		30		40		ns
t_{CH}	Clock HIGH Time	10		11		13		18		ns
t_{CL}	Clock LOW Time	10		11		13		18		ns
t_{GHQZ}	$\overline{OE}$ HIGH to Output Tristate[9]		7		8		10		15	ns
t_{GHCH}	$\overline{OE}$ HIGH to Next Clock HIGH	7		7		7		7		ns
t_{DVCL}	Data in Set-Up to Clock	5		6		6		7		ns
t_{CLDX}	Data in Hold from Clock	2		2		2		2		ns
t_{WLCL}	$\overline{WE}_x$ LOW to Clock LOW[12,13]	2		2		2		3		ns
t_{CLWH}	Clock LOW to $\overline{WE}_x$ HIGH[12,13]	4		6		6		7		ns
t_{AVCH}	Address Set-Up	2		2		2		3		ns
t_{CHAX}	Address Hold	5		6		6		6		ns

Switching Waveforms

Read Cycle



Write Cycle



Notes:

6. Test conditions assume signal transition times of 5 ns or less, timimg reference levels of 1.5 V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 75-pF load capacitance.
7. $\overline{WE}$ is HIGH for read cycle.
8. $\overline{OE}$ is selected (LOW).
9. At any given temperature and voltage condition, t_{GHQZ} is less than t_{GLQV} for any given device.
10. $\overline{OE}$ must be HIGH for data-in to propagate to latch.
11. t_{GHQZ} is tested with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500mV from steady-state voltage.
12. Self-timed write is triggered on falling edge of registered $\overline{WE_0}$ or $\overline{WE_1}$ signals.
13. X = 0 or 1 for low byte and high byte, respectively.

Truth Table

$\overline{OE}$	$\overline{WE_0}$	$\overline{WE_1}$	Operation	Inputs/Outputs
L	L	L	Invalid	Invalid
L	L	H	Invalid	Invalid
L	H	L	Invalid	Invalid
L	H	H	Read	Data Out (I/O_0 – I/O_{15})
H	L	L	Write	Data In (I/O_0 – I/O_{15})
H	L	H	Low Byte Write	Data In (I/O_0 – I/O_7)
H	H	L	High Byte Write	Data In (I/O_8 – I/O_{15})
H	H	H	Disabled	High Z

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
18	CY7C157A-18LC	L69	Commercial
	CY7C157A-18JC	J69	
20	CY7C157A-20LC	L69	Commercial
	CY7C157A-20JC	J69	
24	CY7C157A-24LC	L69	Commercial
	CY7C157A-24JC	J69	
	CY7C157A-24LMB	L69	Military
	CY7C157A-24YMB	Y59	
33	CY7C157A-33LC	L69	Commercial
	CY7C157A-33JC	J69	
	CY7C157A-33LMB	L69	Military
	CY7C157A-33YMB	Y59	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{CHCH}	7, 8, 9, 10, 11
t_{CHQV}	7, 8, 9, 10, 11
t_{GHQZ}	7, 8, 9, 10, 11
t_{CHQX}	7, 8, 9, 10, 11
t_{GHQV}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{CHCH}	7, 8, 9, 10, 11
t_{DVCL}	7, 8, 9, 10, 11
t_{AVCH}	7, 8, 9, 10, 11
t_{CHAX}	7, 8, 9, 10, 11
t_{CLDX}	7, 8, 9, 10, 11
t_{DVWL}	7, 8, 9, 10, 11
t_{WLDX}	7, 8, 9, 10, 11

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