MINI-ANALOG SERIES
CMOS SINGLE OPERATIONAL AMPLIFIER

S-8944XA Series

The mini-analog series is a family of standard analog circuits mounted in ultra-small packages.
The S-8944XA series is a CMOS operational amplifier with a built-in phase compensation circuit.
The S-8944XA series is suitable for applications in battery powered compact portable devices due to its lower operation voltage and lower current consumption compared to bipolar operational amplifiers.

■ Features

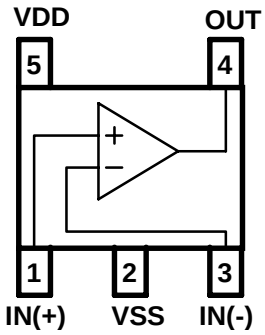
- Low operation voltage: VDD= 0.9 to 5.5 V
- Low current consumption: IDD= 0.5 μA (typ)
- Wide input/output voltage range: VSS to VDD
- Low input offset voltage: 5.0 mV max.
- Internal phase compensation No external parts
- Small package (SC-88A) 2.0 mm × 2.1 mm)

■ Applications

- Cellular phone
- PDA
- Note PC
- Digital camera
- Digital video camera

■ Pin Assignment

5-pin SC-88A
Top View



(S-8944XANC)

Figure 1

Pin No.	Symbol	Functions
1	IN(+)	Non-invert input pin
2	VSS	GND pin
3	IN(–)	Invert input pin
4	OUT	Output pin
5	VDD	Positive power pin

■ Package

- SC-88A (PKG code: NP005-B)

■ Selection Guide

Off-set voltage	Product Name
VIO = 10 mV max.	S-89440ANC–HBX–TF
VIO = 5 mV max.	S-89441ANC–HBY–TF

■ Absolute Maximum Ratings

Table 1

Parameter	Symbol	Ratings	Unit
Power voltage	V_{DD}	7.0	V
Input voltage	V_{IN}	0 to 7.0	V
Differential input voltage	V_{IND}	±5.5	V
Allowable loss	P_D	200	mW
Operating temperature	T_{opr}	–40 to 85	°C
Storage temperature	T_{stg}	–55 to +125	°C

■ Recommended Operation Voltage Range

Table 2

Parameter	Symbol	Range
Operation voltage range	V_{DDope}	0.9 to 5.5 V

■ Electrical Characteristics

A difference between the S-89440ANC and S-894411ANC is only offset voltage.
The other specifications are the same.

1. V_{DD}=3.0 V

DC Characteristic (V_{DD}=3.0 V)

Table 3

(Ta=25 °C unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test circuit
Supply current	IDD	$V_{CM}=V_{OUT}$=1.5V	—	0.5	0.9	µA	Figure 7
Offset voltage	VIO	S-89440ANC V_{CM}=1.5V	—	5	10	mV	Figure 3
		S-89441ANC V_{CM}=1.5V	—	3	5	mV	
Input offset current	IIO	—	—	1	—	pA	—
Input vias current	IBIAS	—	—	1	—	pA	—
Common mode input voltage	VCMR	—	0	—	3.0	V	Figure 4
Voltage gain (Open loop)	AVOL	V_{SS}+0.1V ≤V_{OUT} ≤V_{DD}-0.1V; V_{CM}=1.5V, RL=1MΩ	70	80	—	dB	Figure 11
Maximum output amplitude voltage	VOH	RL=100kΩ	2.95	—	—	V	Figure 5
	VOL	RL=100kΩ	—	—	0.05	V	Figure 6
Common mode input signal rejection rate	CMRR	V_{SS} ≤ V_{CM} ≤ V_{DD}	45	65	—	dB	Figure 4
		V_{SS} ≤ V_{CM} ≤ V_{DD}-0.1V	50	65	—	dB	
Power supply rejection ratio	PSRR	V_{DD}=0.9 to 5.5V	70	80	—	dB	Figure 2
Source current (*1)	ISOURCE	V_{OUT}=VDD-0.1V	400	500	—	µA	Figure 8
		V_{OUT}=0V	4800	6000	—	µA	
Sink current	ISINK	V_{OUT}=0.1V	400	550	—	µA	Figure 9
		V_{OUT}=VDD	4800	6000	—	µA	

AC Characteristic (V_{DD}=3.0 V)

Table 4

(Ta=25 °C unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test circuit
Slew rate (*2)	SR	RL=1.0MΩ, CL=15pF	—	5.0	—	V/ms	Figure 10
Cut-off frequency (*3)	f_T	CL=0pF	—	4.8	—	kHz	—
Maximum load capacitance (*4)	CL	—	—	47	—	pF	—

(*1) Use the device within the range under 7 mA of the source current.
(*2)(*3)(*4) 100% inspection is not performed.

2. V_{DD}=1.8 V

DC Characteristic (V_{DD}=1.8 V)

Table 5

(Ta=25 °C unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test circuit
Supply current	IDD	V_{CM}=V_{OUT}=1.5 V	—	0.5	0.9	μA	Figure 7
Offset voltage	VIO	S-89440ANC:V_{CM}=0.9 V	—	5	10	mV	Figure 3
		S-89441ANC:V_{CM}=1.5 V	—	3	5	mV	
Input offset current	IIO	—	—	1	—	pA	—
Input vias current	IBIAS	—	—	1	—	pA	—
Common mode input voltage	VCMR	—	0	—	1.8	V	Figure 4
Voltage gain (Open loop)	AVOL	V_{SS}+0.1V ≤V_{OUT} ≤V_{DD}-0.1V; V_{CM}=0.9V, RL=1MΩ	66	75		dB	Figure 11
Maximum output amplitude voltage	VOH	RL=100 kΩ	1.75	—	—	V	Figure 5
	VOL	RL=100 kΩ	—	—	0.05	V	Figure 6
Common mode input signal rejection rate	CMRR	V_{SS} ≤ V_{CM} ≤ V_{DD}	35	55	—	dB	Figure 4
		V_{SS} ≤ V_{CM} ≤ V_{DD}-0.3 V	45	60	—	dB	
Power supply rejection ratio	PSRR	V_{DD}=0.9 to 5.5 V	70	80	—	dB	Figure 2
Source current (*1)	ISOURCE	V_{OUT}=VDD-0.1 V	220	300	—	μA	Figure 8
		V_{OUT}=0 V	1200	1800	—	μA	
Sink current	ISINK	V_{OUT}=0.1 V	220	300	—	μA	Figure 9
		V_{OUT}=VDD	1200	1800	—	μA	

AC Characteristic (V_{DD}=1.8 V)

Table 6

(Ta=25 °C unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test circuit
Slew rate (*1)	SR	RL=1.0MΩ, CL=15pF	—	4.5	—	V/ms	Figure 10
Cut-off frequency (*2)	f_T	CL=0pF	—	5.0	—	kHz	—
Maximum load capacitance (*3)	CL	—	—	47	—	pF	—

(*1)(*2)(*3) 100% inspection is not performed.

3. V_{DD}=0.9 V

DC Characteristic (V_{DD}=0.9 V)

Table 7

(Ta=25 °C unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test circuit
Supply current	IDD	V_{CM}=V_{OUT}=0.45 V	—	0.5	0.9	µA	Figure 7
Offset voltage	VIO	S-89440ANC:V_{CM}=0.45 V	—	5	10	mV	Figure 3
		S-89441ANC:V_{CM}=0.45 V	—	3	5	mV	
Input offset current	IIO	—	—	1	—	pA	—
Input vias current	IBIAS	—	—	1	—	pA	—
Common mode input voltage	VCMR	—	0	—	0.9	V	Figure 4
Voltage gain (Open loop)	AVOL	V_{SS}+0.1V ≤V_{OUT} ≤V_{DD}-0.1V; V_{CM}=0.45V, RL=1MΩ	60	75		dB	Figure 11
Maximum output amplitude voltage	VOH	RL=100 kΩ	0.85	—	—	V	Figure 5
	VOL	RL=100 kΩ	—	—	0.05	V	Figure 6
Common mode input signal rejection rate	CMRR	V_{SS} ≤ V_{CM} ≤ V_{DD}	25	55	—	dB	Figure 4
		V_{SS} ≤ V_{CM} ≤ V_{DD}-0.35 V	40	60	—	dB	
Power supply rejection ratio	PSRR	V_{DD}=0.9 to 5.5 V	70	80	—	dB	Figure 2
Source current (*1)	ISOURCE	V_{OUT}=VDD-0.1 V	25	65	—	µA	Figure 8
		V_{OUT}=0 V	40	140	—	µA	
Sink current	ISINK	V_{OUT}=0.1 V	10	65	—	µA	Figure 9
		V_{OUT}=VDD	12	120	—	µA	

AC Characteristic (V_{DD}=0.9 V)

Table 8

(Ta=25 °C unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test circuit
Slew rate (*1)	SR	RL=1.0MΩ, CL=15pF	—	4.0	—	V/ms	Figure 10
Cut-off frequency (*2)	f_T	CL=0pF	—	5.0	—	kHz	—
Maximum load capacitance (*3)	CL	—	—	47	—	pF	—

(*1)(*2)(*3) 100% inspection is not performed.

■ Test Circuits

1. Power supply rejection ratio

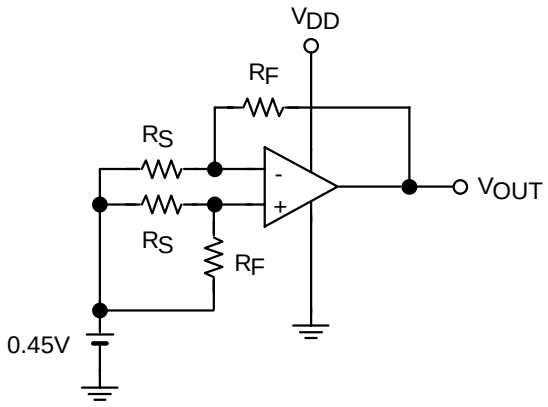


Figure 2

- Power supply rejection ratio (PSRR)
  Measure V_{OUT} when power supply voltage is V_{DD}. Calculate a power supply rejection ratio (PSRR) by the following formula:

  Test Conditions:
  When V_{DD}=0.9 V; V_{DD}=V_{DD1}, V_{OUT}=V_{OUT1}
  When V_{DD}=5.5 V; V_{DD}=V_{DD2}, V_{OUT}=V_{OUT2}

$$PSRR = -20\log\left(\left|\frac{V_{OUT1}-V_{OUT2}}{V_{DD1}-V_{DD2}}\right|\times\frac{R_S}{R_F+R_S}\right)$$

2. Off-set voltage

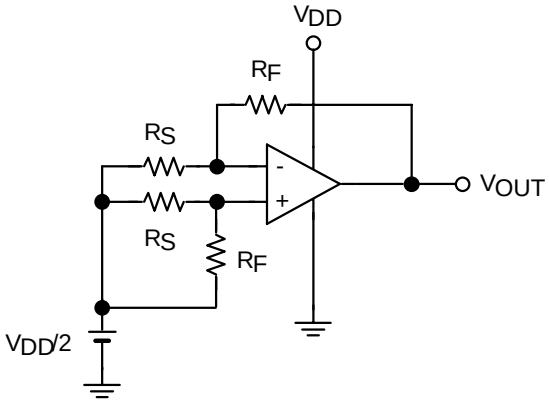


Figure 3

- Off-set voltage (VIO)

$$VIO = \left(VOUT - \frac{V_{DD}}{2}\right)\times\frac{R_S}{R_F+R_S}$$

3. Common mode input signal rejection ratio, Common mode input voltage

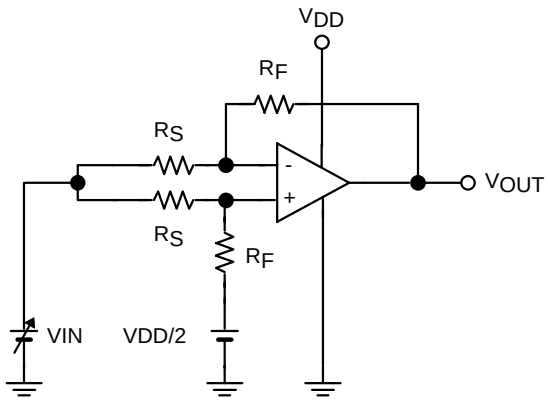


Figure 4

- Common mode input signal rejection ratio (CMRR)
  Measure V_{OUT} for each V_{IN}. Calculate a common mode rejection ratio (CMRR) by the following formula:

  Test Conditions:
  When $V_{IN} = V_{CMR}$ (MAX); $V_{IN}= V_{IN1}$, $V_{OUT}=V_{OUT1}$

  When $V_{IN} = V_{CMR}$ (MAX); $V_{IN}= V_{IN2}$, $V_{OUT}=V_{OUT2}$

$$CMRR = 20\log\left(\left|\frac{V_{IN1}-V_{IN2}}{V_{OUT1}-V_{OUT2}}\right| \times \frac{(R_F+R_S)}{R_S}\right)$$

- Common mode input voltage(VCMR)
  An Input voltage range in which V_{OUT} satisfies the standard for a common mode input signal rejection ratio when changing V_{IN}.

4. Maximum output amplitude voltage

- Maximum output amplitude voltage (V_{OH})

Test Conditions:

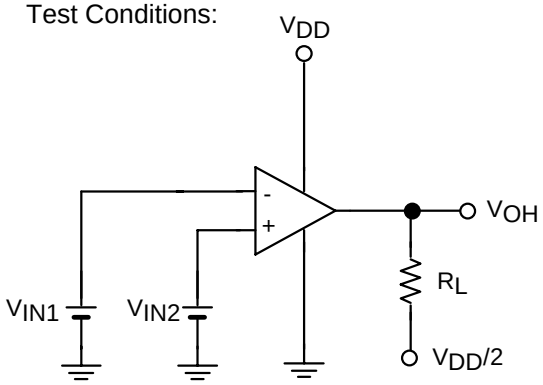


Figure 5

$$V_{IN1} = \frac{V_{DD}}{2} - 0.1V$$

$$V_{IN2} = \frac{V_{DD}}{2} + 0.1V$$

R_L=100kΩ

- Maximum output amplitude voltage (V_{OL})

Test Conditions:

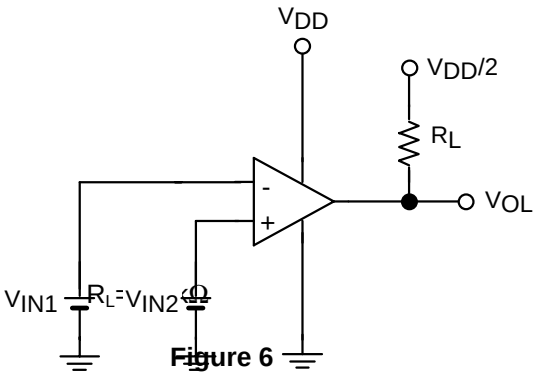


Figure 6

$$V_{IN1} = \frac{V_{DD}}{2} + 0.1V$$

$$V_{IN2} = \frac{V_{DD}}{2} - 0.1V$$

5. Supply current

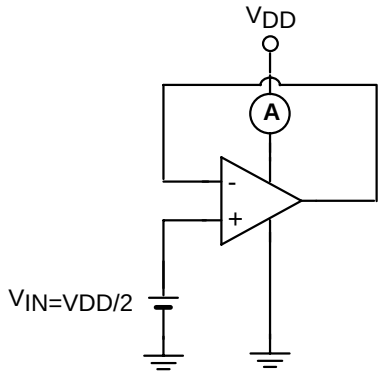


Figure 7

- Supply current (I_{DD})

6. Source current

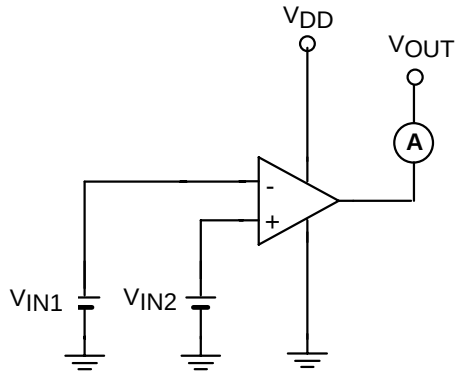


Figure 8

- Source current (I_{SOURCE})

Test Condition:

$V_{OUT}=V_{DD}-0.1V$ or $V_{OUT}=0V$

$$V_{IN1}=\frac{V_{DD}}{2}-0.1V$$

$$V_{IN2}=\frac{V_{DD}}{2}+0.1V$$

7. Sink current

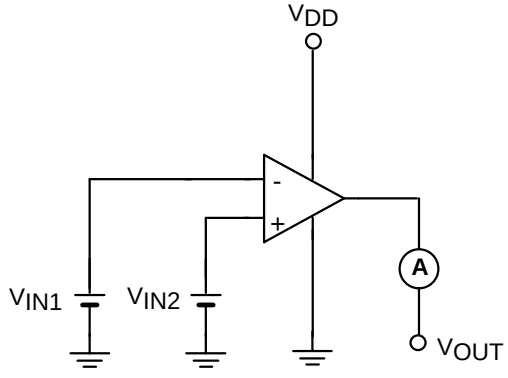


Figure 9

- Sink current (I_{SINK})

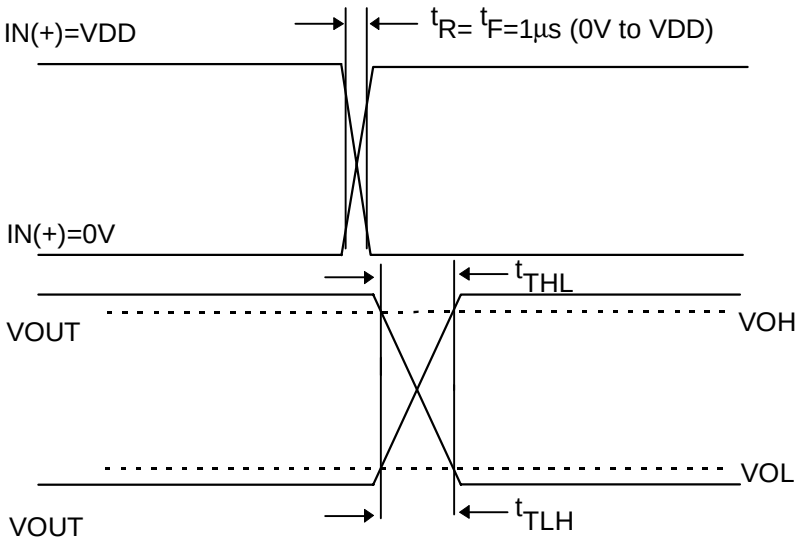
Test Condition:

$V_{OUT}=0.1V$ or $V_{OUT}=V_{DD}$

$$V_{IN1}=\frac{V_{DD}}{2}+0.1V$$

$$V_{IN2}=\frac{V_{DD}}{2}-0.1V$$

8. Slew rate (SR)



Falling:

$$SR = \frac{VOH - VOL}{t_{THL}}$$

Rising:

$$SR = \frac{VOH - VOL}{t_{TLH}}$$

Figure 10

VOH=2.7 V (at V_{DD}=3.0 V), 1.62 V (at V_{DD}=1.8 V), 0.81 V (at V_{DD}=0.9 V)
VOL=0.3 V (at V_{DD}=3.0 V), 0.18 V (at V_{DD}=1.8 V), 0.09 V (at V_{DD}=0.9 V)

9. Voltage gain (Open loop)

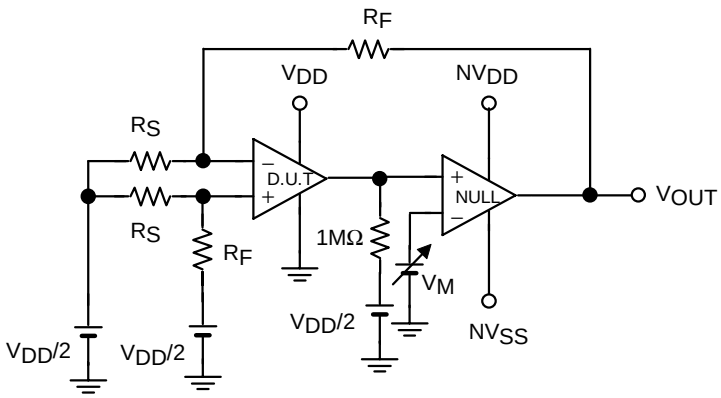


Figure 11

- Voltage gain (Open loop) (AVOL)
  Measure V_{OUT} for each V_M.
  Calculate the voltage gain (AVOL) by the following fomula:

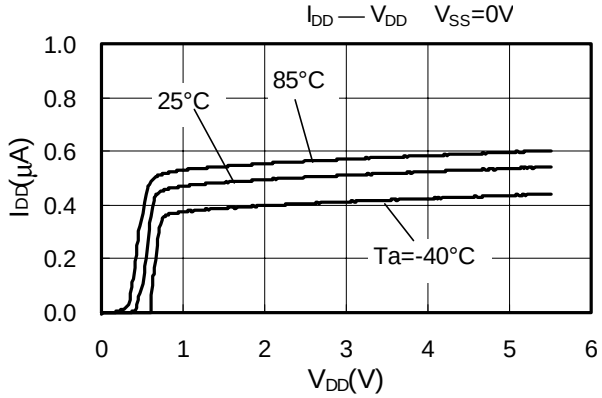
  Test Conditions:
  When $V_M = V_{DD}$-0.1 V;
  $V_M=V_{M1}$
  $V_{OUT}=V_{OUT1}$

  When V_M = 0.1 V;
  $V_M=V_{M2}$
  $V_{OUT}=V_{OUT2}$

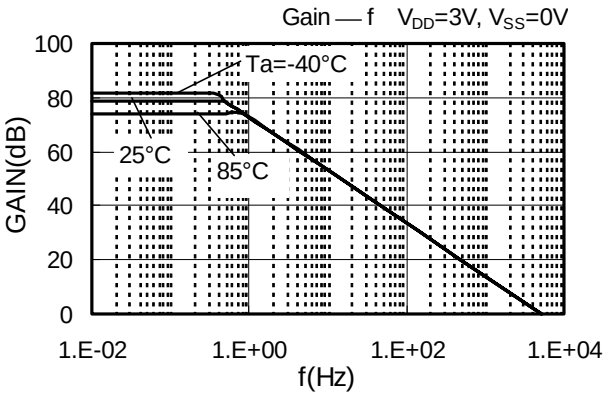
$$AVOL = 20\log\left(\left|\frac{V_{M1} - V_{M2}}{V_{OUT1} - V_{OUT2}}\right| \times \frac{(R_F + R_S)}{R_S}\right)$$

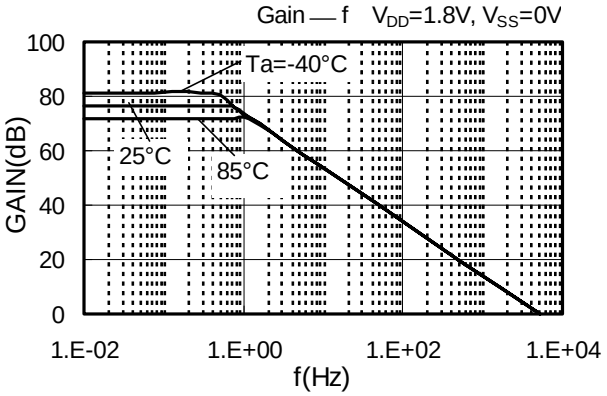
■ Typical Performance Characteristics

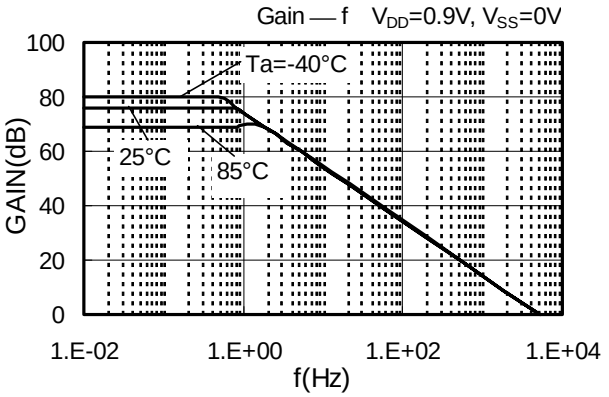
1. Current consumption vs Supply voltage



2. Voltage gain vs Frequency

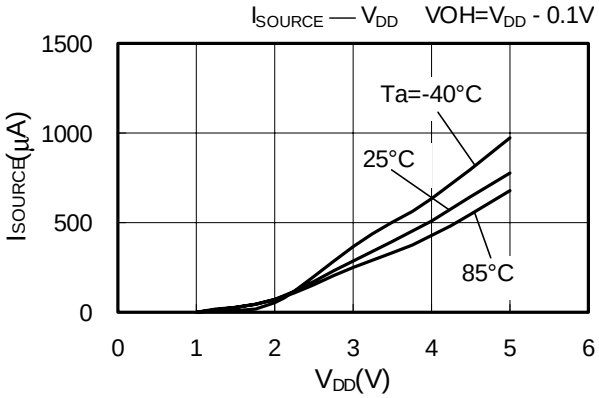




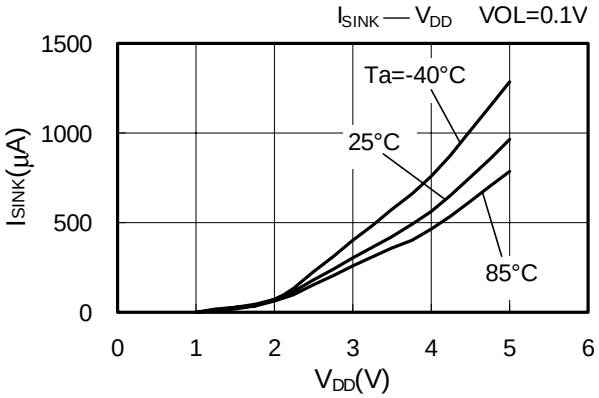


3. Output current

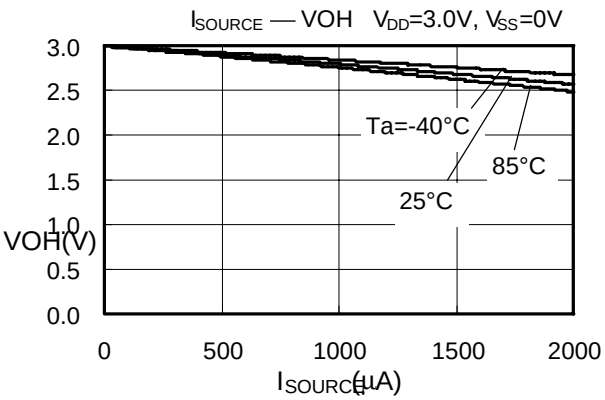
3-1. I_{SOURCE} vs Supply voltage

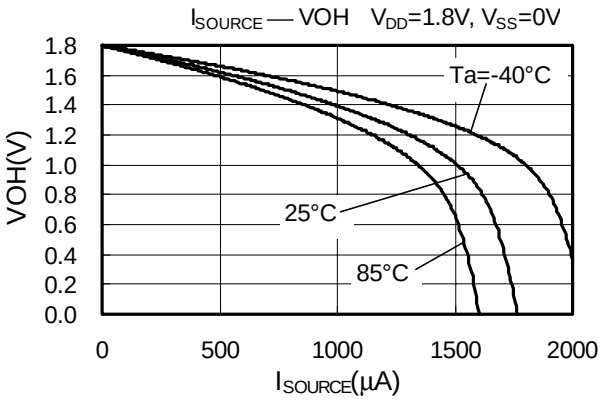


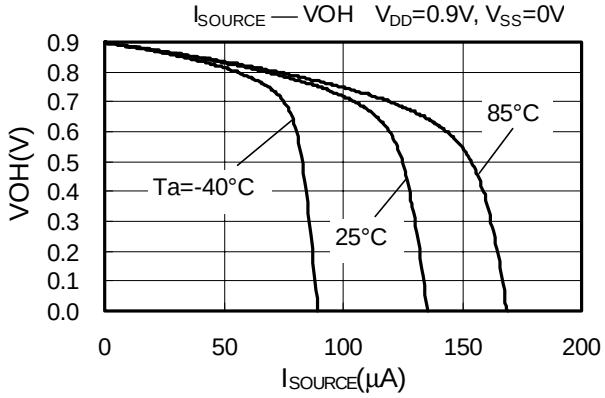
I_{SINK} vs Supply voltage



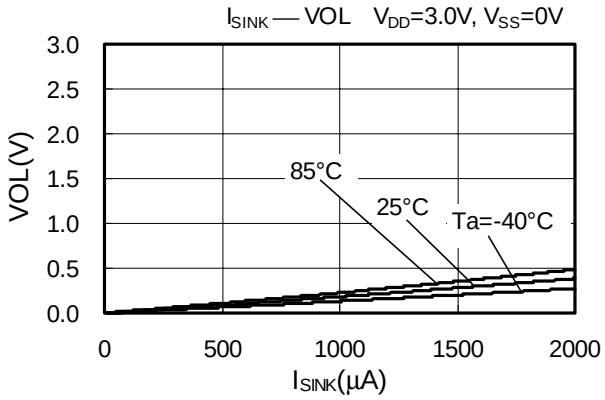
3-2. Output voltage (V_{OH}) vs I_{SOURCE}

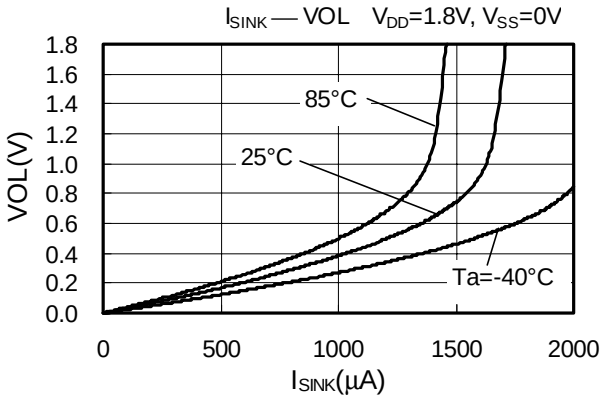


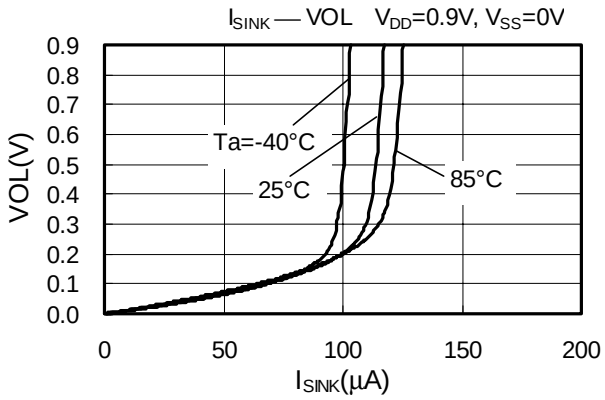




3-3. Output voltage (V_{OL}) vsI_{SINK}



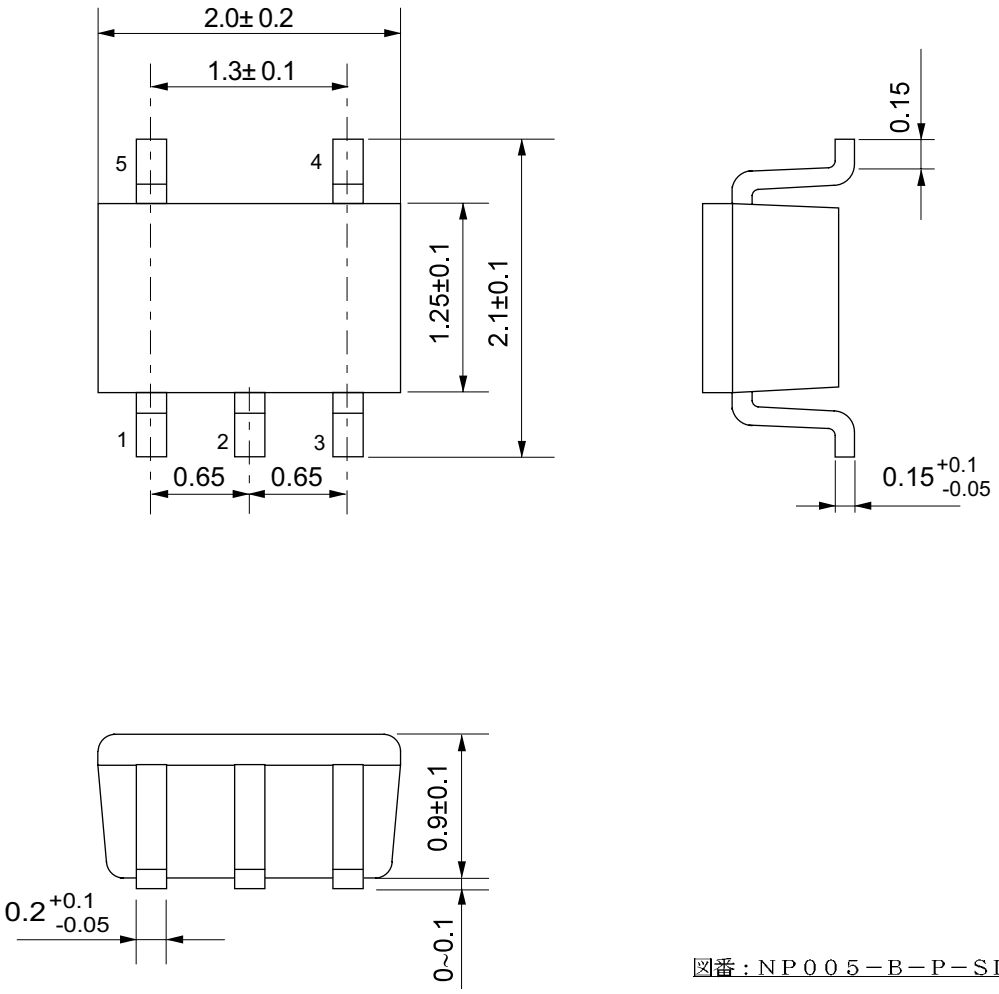




■ SC-88A

●Dimensions 外形図

Unit：mm



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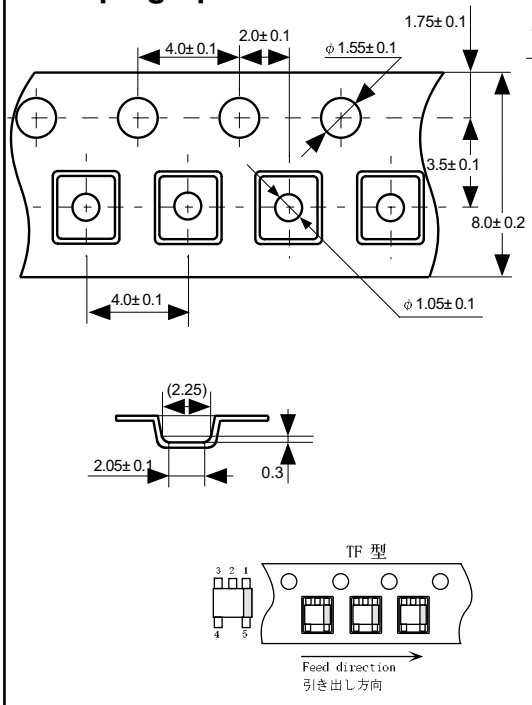
●Taping Specifications テーピング図



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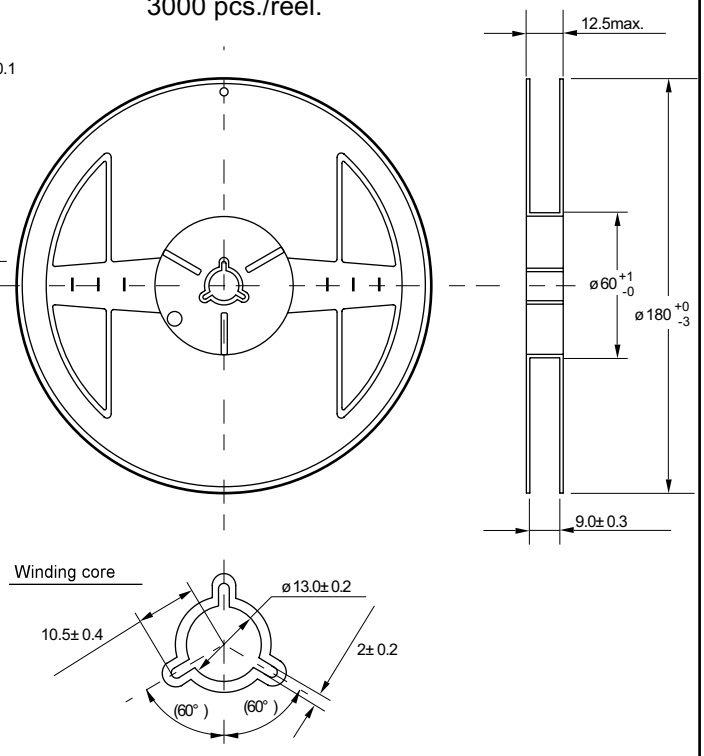
●Reel Specifications リール図

3000 pcs./reel.



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