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SSI 32R1570AR
+5, -5 V, 12-Channel MR Head Read/Write Device
Advance Information

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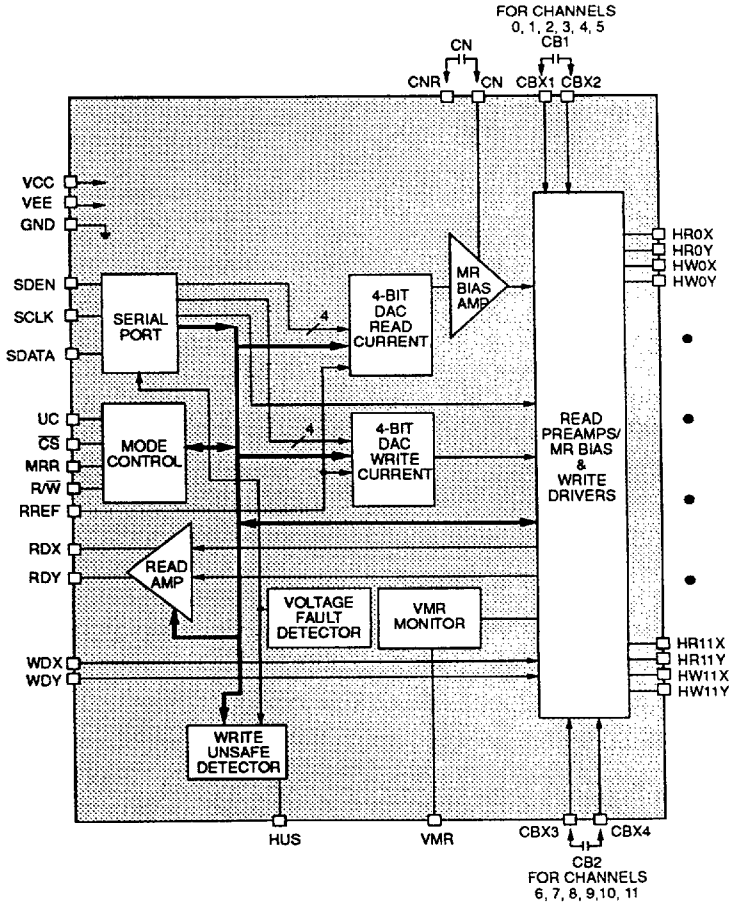
DESCRIPTION

The SSI 32R1570AR is a BiCMOS monolithic integrated circuit designed for use with four-terminal Magneto-Resistive recording heads. The reader architecture is MR current bias/voltage sense. A write-only back capability serial port is provided to enable the implementation of on-chip MR bias and write current DACs. It provides a write driver, low noise read amplifier, serial port controlled head selection, servo bank write, write current MR read bias current and fault detection circuitry for up to twelve channels. In servo write mode, 3 channels can be separately selected. The device requires +5 V and -5 V and comes in an 80-Lead TQFP package.

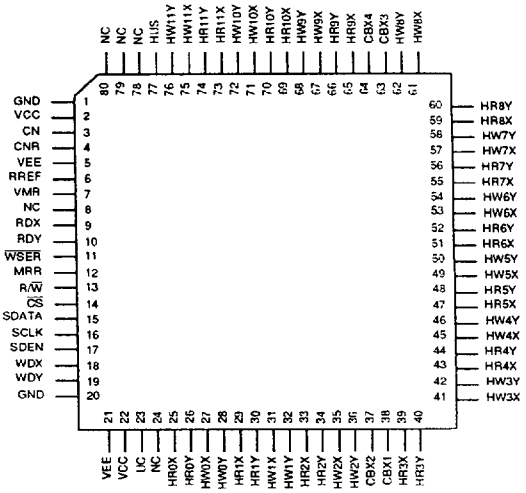
FEATURES

- **+5 V, -5 V ±10% supply**
- **Designed for four-terminal MR heads with minimum external components**
- **Truly differential current bias/voltage sense MR read amp**
- **MR head bias current range = 4 - 15 mA**
- **MR read gain = 220 V/V (nom)**

BLOCK DIAGRAM



PIN DESCRIPTION



SSI 32R1570AR-12 CGT
12-Channel
80-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

FEATURES (continued)

- MR read input noise = 0.75 nV√Hz (nom)
- Differential PECL write data inputs
- Head voltage swing = 12 Vp-p (typ)
- Write current range = 10 - 40 mA
- Read and write fault detection
- Power supply fault protection
- Enhanced system write to read recovery time
- Head select, write current magnitude and MR bias current are controlled by serial interface

FUNCTIONAL DESCRIPTION

The SSI 32R1570AR addresses up to 12 MR heads providing write drive or read bias and amplification. Mode control is accomplished with TTL pins MRR, R/$\overline{W}$ and $\overline{CS}$. The TTL inputs have internal pull-up resistors so that when left opened, they will default to the TTL high state.

WRITE MODE

Write current is enabled to the selected channel, write data controls the write current polarity, and the chip drives the WUS, VMR and RDX, RDY outputs. Enabling of reader bias current is independent of this mode (see descriptions of the MRR input and the MRR_S bit for information on control of bias current).

The WUS output is low in this mode unless there is a write fault, which causes the output to go high.

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects the write mode which configures the SSI 32R1570AR as a current switch and activates the write unsafe (WUS) detect circuitry. The head current is toggled between the X (HWnX) and Y (HWnY) side of the selected head on each low to high transition of the differential PECL signal WDX-WDY. With WDX>WDY Iw will flow from the Y to the X pin, i.e., the Y side of the head will be higher potential than the X side. Write current magnitude is controlled by a 4-bit on-board digital to analog converter. This DAC is programmed via the serial port.

The magnitude of the write current (0-pk) is given by:

$$Iw = 10\ mA + 30\ mA\ (N/15)$$

where N = decimal value of WC0 - WC3 (Register 32d).

Note that the actual head current Ix,y is given by:

$$Ix,y = \frac{Iw}{1+Rh/Rd}$$

where Rh is the head DC resistance and Rd is the damping resistance.

While in the write mode the voltages on CN and CB1/CB2 will be held to the values they were during the last read. This facilitates fast switching from write to read.

BANK WRITE AND DUAL-CHIP BANK WRITE MODES

A special mode which uses two different features to facilitate reduced servo/write time. Bank write feature allows writing in parallel on multiple channels within one chip, and/or two chips at a time in a dual-chip configuration. Banks are arranged in four groups of three channels each. The dual write feature allows writing one channel in each of the two preamps in a dual-chip configuration. Dual write is only defined for two preamp implementation.

These modes are entered by setting the proper select/enable bits in the Control Register (5) and Multi-Write Register (3) (see Serial Interface section for details). Writing begins when R/$\overline{W}$ is asserted.

The VMR, WUS and RDX, RDY outputs are not driven in this mode regardless of the state of R/$\overline{W}$.

READ MODE

Bias current is enabled to the selected head, the chip drives the WUS, VMR and RDX, RDY outputs. The read signal output is the amplified head signal.

The WUS signal is high in this mode unless there is a read fault which causes the output to go low.

The $\overline{UC}$ input allows dual preamp operation transparent to firmware. When high or left open (internally pulled-up) head channels 0-11 map to select values 0-11. When tied to a logic low, preamp channels 0-11 are mapped to head select values 16-27.

Taking $\overline{CS}$ low with R/$\overline{W}$ and MRR high select read mode which activates the MR bias current generator and low noise differential amplifier. The outputs of the read amplifier RDX and RDY are emitter followers and are in phase with the resistivity change at the selected input ports HRnX and HRnY where the respective MR head is attached. The DC current necessary for biasing the MR sensor is internally programmed by a 5-bit DAC via the serial port and the current value is set externally by a resistor connected from pin RREF to GND or by a current sink.

$$Imr\ (mA) = [0.4 + 1.2\mu\ (N/31)]\ [3223/(329 + R_{MR})] + [66/\ (329 + R_{MR})]$$

where N = decimal value of MR0 - MR4

R_{MR} = MR Head Resistance

An external capacitor connected from pin CN to CNR is used for reducing the noise from the MR bias current source. A low inductance capacitor with a value of 0.1 µF is recommended. Two external floating capacitors CB1 and CB2, connected between pins CBX1/CBX2 and CBX3/CBX4, respectively, are required for DC blocking. Care should be taken to use low inductance high frequency capacitors and to locate them as close to the pins as possible. The stray inductance will degrade the amplifier's noise and frequency response performance. The value of the DC blocking capacitors will have direct effect on the write to read recovery time. For fast recovery time, the capacitor value should be kept as small as possible. The value of the capacitor also sets the low frequency cutoff of the read amplifier. The -3 dB low-frequency corner is given by:

$$f_L = 1/(2\pi \cdot 15\Omega \cdot C)$$

For example, a 0.033 µF capacitor will result in the -3 dB low-frequency of about 320 kHz.

The voltage drop across the MR head is monitored internally. The VMR pin provides a monitor voltage referenced to ground of the MR head bias voltage. The maximum output current of the VMR pin should not exceed 1 mA.

READ-INACTIVE MODE

Similar to read mode, but the MR bias current is diverted to an internal dummy resistor. The chip is in its normal power-consumption mode, and drives the WUS, VMR and RDX, RDY outputs. Entered when an illegal head number within the preamp's assigned range is selected, or when a valid head is selected and the MR bias current is disabled.

Recovery time from this mode to read mode will be no longer than the worst-case head-switch time. The AC read signal output in this mode is undefined. The DC read outputs are the same as in normal read mode in order to facilitate fast recovery to read mode.

The WUS output is a constant low during this mode.

READ BIAS ACTIVE IN WRITE (RBAW) MODE

Taking $\overline{CS}$ and R/$\overline{W}$ low and MRR high selects the RBAW (read bias active in write) mode. In this mode the write driver is active just as in the write mode but the MR bias circuitry is also active. The outputs of the read amplifier RDX/RDY remain inactive, i.e., high impedance. The purpose of this mode is to speed up the write to read transition times by selecting this mode just prior to switching to the read mode. To be effective it is suggested that RBAW mode be selected at least 10 µs prior to selecting read mode. Switching times from RBAW to read mode are guaranteed to be less than 1 µs.

FUNCTIONAL DESCRIPTION (continued)

IDLE MODE

Taking $\overline{CS}$ high selects idle mode which deactivates both the write driver and read amp/MR bias circuitry.

All outputs are disabled, with the reader and writer sections put into a minimum power-consumption standby mode. The chip does not drive any of the outputs in this mode.

In this mode, the chip unconditionally cannot write to any channel and bias current is off in all head channels. The serial bus continues to operate in this mode.

Read bias current will be diverted to an internal dummy head with proper bias current will be selected to deep the DC-blocking and noise-filtering caps biased, and all critical nodes on chip will remain selected to facilitate quick recovery from this mode. Recovery from this mode to read mode is expected to be no longer than the worst-case head switch time. Recovery from this mode to write mode is not specified.

The WUS output is a constant HIGH during this mode.

The pins RDX/RDY are switched into high impedance state to facilitate multiple device applications where these pins could be wire OR'ed.

POWER SUPPLY FAULT PROTECTION

A voltage fault detection circuit improves data security by disabling the write current generator and the MR bias current/read amplifier during a voltage fault or power start-up regardless of mode.

WUS OPERATION

WUS pin flags a fault condition in the read or write modes:

Read Fault Detection

A logic low on the WUS pin in read mode indicates a read fault condition. A read fault may be any one of the following conditions:

- Open head
- MR bias current too high
  (Ibias > 1.5 • programmed value)

Write Fault Detection

A logic high on the WUS pin in write mode indicates a write fault condition. A write fault may be any one of the following conditions:

- Open head
- No write data (f < 1 MHz)
- No write current

In addition to generating a write fault condition, the following conditions also disable the write current:

- Device in read mode
- Low power supply voltage
- Invalid head selected

TABLE 1: Mode Select

$\overline{CS}$ chip select	R/$\overline{W}$ write enable	MRR read bias enable	$\overline{WSER}$ servo	SE_S servo enable REG 5, BIT 3	MRR_S read bias enable REG 5, BIT 2	$\overline{CS}$_S chip select REG 5, BIT 1	WRITE current	MR BIAS in selected head	MODE
0	1	1	X	X	X	0	OFF	ON	READ
0	1	X	X	X	1	0	OFF	ON	READ
0	1	0	X	X	0	0	OFF	OFF (dummy)	READ-INACTIVE
0	0	1	1	0	X	0	ON	ON	WRITE (read bias active)
0	0	X	1	0	1	0	ON	ON	WRITE (read bias active)
0	0	0	1	0	0	0	ON	OFF (dummy)	WRITE
0	0	X	X	1	X	0	ON	OFF	SERVO WRITE
0	0	X	0	X	X	0	ON	(dummy)	SERVO WRITE
1	X	X	X	X	X	X	OFF	OFF	IDLE
X	X	X	X	X	X	1	OFF	OFF	IDLE

Note that $\overline{CS}$ is the logical OR of the $\overline{CS}$ input and the $\overline{CS}$_S bit. MRR is the logical OR of the MRR input and the MRR_S bit. Servo write is the logical OR of the $\overline{WSER}$ and SE_S bit.

SERIAL INTERFACE OPERATION

The write only serial data port is used to control head selection, write current magnitude and MR bias current. It does this by writing data into five on board registers addressed 1, 2, 3, 4, and 5.

A complete data transfer is sixteen (16) bits long and loaded LSB first. Addresses and data are loaded least significant bit (LSB) first, and addresses are loaded first. The first bit is the R/$\overline{W}$ bit and is always set to zero. The next three bits (S0-S2) are the device select bits and are always written S0 = 1, S1 = 0, and S2 = 0 for R/W amplifiers. The following four bits (A0-A3) are the address bits and the last eight (D0-D7) are the data bits.

Asserting the serial port enable line SDEN initiates a transfer. SDATA is clocked into the internal shift register by the rising edge of SCLK. A counter on the chip ensures that exactly 16 clock pulses occurred prior to SDEN being deasserted otherwise the transfer will be aborted. Loading of the registers takes place on the falling edge of SDEN.

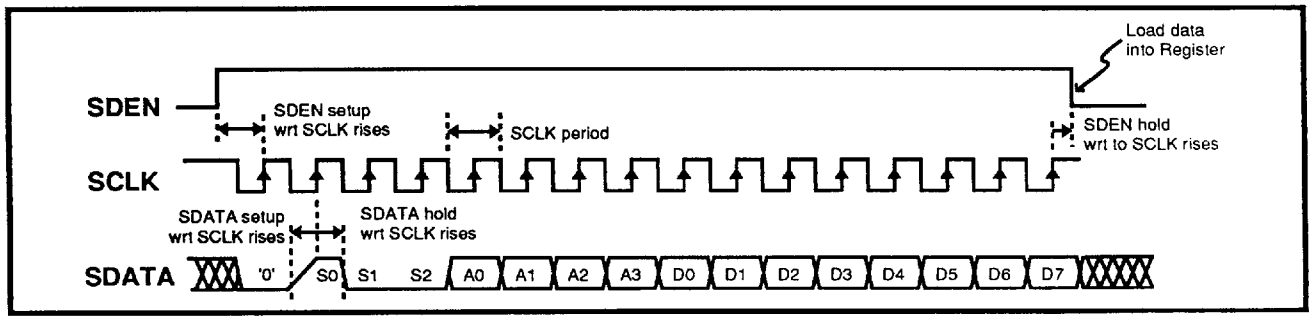


FIGURE 1: Serial Interface Timing Diagram - Writing Control Register

SERIAL INTERFACE OPERATION (continued)

TABLE 2: Serial Port Bit Map

FUNCTION	REG	R/W	S0	S1	S2	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
Head Select	1	0	1	0	0	1	0	0	0	HS0	HS1	HS2	HS3	HS4	X	X	X
Bank/Dual Write	2	0	1	0	0	0	1	0	0	MW0	MW1	MW2	MW3	MW4	MW5	MW6	X
Write Current DAC	3	0	1	0	0	1	1	0	0	WC0	WC1	WC2	WC3	X	X	X	X
MR Bias Current DAC	4	0	1	0	0	0	0	1	0	RB0	RB1	RB2	RB3	RB4	X	X	X
Control	5	0	1	0	0	1	0	1	0	CM0	CM1	CM2	CM3	CM4	CM5	X	X

TABLE 3: Register Definitions

REGISTER	BIT	DESCRIPTION
1	0-4	Head Address Select (see Table 5). Sets the head to read or write via a 5-bit address word.
2	0-6	Bank/Dual Write (See Functional Description, bank and dual write modes. See Table 6). This is the Servo Write Mode Select Register. Selects bank write or dual write mode.
3	0-3	Write Current DAC (see Functional Description, Write Mode). Sets the input to a 4-bit DAC controlling write current. A value of 0 corresponds to minimum current, and 15d corresponds to maximum current.
4	0-4	MR Bias Current (see Functional Description, Read Mode). Sets the value to a 5-bit DAC controlling MR element bias current. A value of 0 corresponds to minimum bias current and 31d corresponds to maximum current.
5	0-5	Set Control Mode (see Table 8).

TABLE 4: Serial Port Bit Map, Power-up or Power Supply Fault

FUNCTION	REG	R/W	S0	S1	S2	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
Head Select	1	0	1	0	0	1	0	0	0	1	1	1	1	1	0	0	0
Multi-Write	2	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Write Current	3	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
MR Bias Current	4	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Control	5	0	1	0	0	1	0	1	0	0	1	0	0	0	0	0	0

TABLE 5: 12-Channel Head Select, Normal Mode

UC*	HS4	HS3	HS2	HS1	HS0	HEAD SELECTED LOWER PREAMP	HEAD SELECTED UPPER PREAMP
1	0	0	0	0	0	0	
1	0	0	0	0	1	1	
1	0	0	0	1	0	2	
1	0	0	0	1	1	3	
1	0	0	1	0	0	4	
1	0	0	1	0	1	5	
1	0	0	1	1	0	6	
1	0	0	1	1	1	7	
1	0	1	0	0	0	8	
1	0	1	0	0	1	9	
1	0	1	0	1	0	10	
1	0	1	0	1	1	11	
0	1	0	0	0	0		0
0	1	0	0	0	1		1
0	1	0	0	1	0		2
0	1	0	0	1	1		3
0	1	0	1	0	0		4
0	1	0	1	0	1		5
0	1	0	1	1	0		6
0	1	0	1	1	1		7
0	1	1	0	0	0		8
0	1	1	0	0	1		9
0	1	1	0	1	0		10
0	1	1	0	1	1		11

* Dual-chip head selection

SERIAL INTERFACE OPERATION (continued)

TABLE 6: Dual-Chip Write and Servo Bank Select

This is the Servo Write Mode Select Register. Selects bank write or dual-chip write mode as described in Section 2.0.

MW6	MW5	MW4	MW3	MW2	MW1	MW0
Dual Write Enable	Upper Bank Enable	Lower Bank Enable	Upper Bank MSB	Upper Bank LSB	Lower Bank MSB	Lower Bank LSB

00	Upper Bank	0	00 Lower Bank	0
01	Upper Bank	1	01 Lower Bank	1
10	Upper Bank	2	10 Lower Bank	2
11	Upper Bank	3	11 Lower Bank	3

BANK NUMBER	WRITE CHANNELS
0	0,4,8
1	1,5,9
2	2,6,10
3	3,7,11

BIT	FUNCTION
MW0-1	Selects lower preamp bank.
MW2-3	Selects upper preamp bank. Not defined in single preamp application.
MW4	Enables lower preamp bank write mode. When set, overrides dual write mode.
MW5	Enables upper preamp bank write mode. When set, overrides dual write mode.
MW6	Enables dual write mode. Both preamps respond to lower preamp address field. Only has effect for MW5 = MW4 = 0. Not defined in single preamp application.

TABLE 7: 12-Channel Head Select, Servo Mode

$\overline{WSER}$, OR SE_S REG 5, BIT CM3	MW6	MW5	MW4	MW3	MW2	MW1	MW0	UC = HIGH HS4 = LOW HEADS SELECTED, LOWER PREAMP	UC = LOW HS4 = HIGH HEADS SELECTED, HIGHER PREAMP
0	X	X	X	X	X	X	X	All Servo Write Modes Disabled	
1	0	X	X	X	X	X	X	Dual Write Disabled	
1	X	0	1	X	X	0	0	0,4,8	
1	X	0	1	X	X	0	1	1,5,9	
1	X	0	1	X	X	1	0	2,6,10	
1	X	0	1	X	X	1	1	3,7,11	
1	X	1	0	0	0	X	X		0,4,8
1	X	1	0	0	1	X	X		1,5,9
1	X	1	0	1	0	X	X		2,6,10
1	X	1	0	1	1	X	X		3,7,11
1	1	0	0	X	X	X	X	Write enabled either lower or higher. Writes to channels selected by HS0-HS4 (register 02).	

TABLE 8: Set Control Mode

BIT	NAME	FUNCTION
CM0	HPHIGH	When reset, the normal (low) high-pass frequency is in effect; when set, the high frequency is in effect.
CM1	$\overline{CS}$_S	This is the idle override bit. When set, forces the chip into idle mode. When reset, entry into the idle mode is controlled by $\overline{CS}$ input pin.
CM2	MRR_S	When set, forces the MR bias current on in the selected head. When reset, bias current enabling is controlled by the MRR pin.
CM3	SE_S	When set, forces the chip onto the special servo write mode used for multi-channel writing.
CM4	PWR_S	When set, forces the inactive preamp in dual preamp configurations to a reduced power consumption state (standby). When reset, forces the inactive preamp in dual preamp configurations to a minimum power consumption state (sleep).
CM5	VMR_S	When set, the VMR output is in its normal low impedance state and is driven with the selected reader head voltage. When reset, the VMR output is off and goes into a high impedance state to help prevent any noise coupling back into the preamp.

PIN DESCRIPTION

CONTROL INPUT PINS

NAME	TYPE	DESCRIPTION
HR0X–HR11X HR0Y–HR11Y	I/O	MR read head input X and Y connections
HW0X–HW11X HW0Y–HW11Y	O	Inductive write head X and Y connections
CBX1/CBX2	O	Floating DC blocking cap CB1; for head 0, 1, 2, 3, 4, 5
CBX3/CBX4	O	Floating DC blocking cap CB2: for head 6, 7, 8, 9, 10, 11
WDX, WDY	I	Differential PECL write data input
RDX, RDY	O	Differential MR head read data output
RREF	O	3.32 kΩ resistor to ground sets reference current for read/write DAC
HUS	O	Open-collector R/W fault indicator from the selected preamp. May be wire-OR'd in multiple preamp configuration.
SDATA	I	Serial data used for head selection, setting write current magnitude and MR bias current TTL.
SCLK	I	Serial clock, TTL
SDEN	I	Serial data enable, TTL
VCC		+5V Supply
VEE		-5V Supply
GND		Ground
VMR	O	MR head DC voltage drop monitor; referenced to ground
R/$\overline{W}$	I	A low-level selects write mode on the selected channel if a valid head is selected. A high level selects read or read-inactive depending on the state of head selects and bias current enable.
MRR	I	Real-time MR bias current control pin. A high level enables bias current to the selected head. Logically OR'd with the MRR_S in register (5) to produce actual bias current control.
$\overline{CS}$	I	A low level places the chip in its normal power up state. A high level forces the chip into idle mode. Logically OR'd with the CS_S bit in register (5) to produce the actual internal low power control signal.
$\overline{UC}$	I	Configuration hardware strap to allow dual preamp operation transparent to firmware. When high or left open (internally pulled-up), head channels 0-11 map to head select values 0-11. When tied to a logic low preamp channels 0-11 are mapped to head select values 16-27 (see Table 7).
CN	I/O	Noise Filter Capacitor
CNR	I/O	Noise Filter Capacitor Return
$\overline{WSER}$	I	Servo pin control input. Logically OR'd with SE_S in register (5) to produce the actual servo write control signal.

ELECTRICAL SPECIFICATIONS

Recommended conditions apply unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation outside these maximum ratings may cause permanent damage to this device.

PARAMETER		RATING
DC Supply Voltage	V_{CC} V_{EE}	+6 VDC -6 VDC
Logic Input Voltage	(All except WDX, WDY) CMOS (WDX, WDY) PECL	-0.3 to Vcc +0.3 VDC 0 to Vcc VDC
Write Current	I_W	50 mA
MR Bias Current	I_R	30 mA
Output Current	WUS RDX/RDY	+8 mA -5 mA
Operating Junction Temperature	T_J	+135° C
Storage Temperature	T_{STG}	-65° C to +150° C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage	V_{CC} V_{EE}	4.5 V to 5.5 V -4 V to -5.5 V
Operating Ambient Temperature	Ta	0 to 70° C

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. I_R = 10 mA, I_W = 30 mA.

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Supply Current	Vcc	Read mode		59		mA
		Read inactive		25		mA
		Write mode		78		mA
		RBAW mode		102		mA
		Idle mode		14		mA
		Servo write (@ Iw = 40 mA)		197		mA
Supply Current	V_{EE}	Read mode		59		mA
		Read inactive		34		mA
		Write mode (no RBAW)		91		mA
		RBAW mode		115		mA
		Idle mode		21		mA
		Servo write (@ Iw = 40 mA)		221		mA

ELECTRICAL SPECIFICATIONS (continued)

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Power Dissipation	Read mode, Imr = 10 mA		600		mW
	Write mode, Iw = 30 mA		850		mW
	RBAW mode, Iw = 30 mA, Imr = 10 mA		1090		mW
	Read-Inactive mode, Imr = 10 mA		295		mW
	Idle mode		170		mW
VCC Fault Voltage	Iw < 0.2 mA, Imr < 0.2 mA	3.5	3.85	4.2	VDC
VEE Fault Voltage	Iw < 0.2 mA, Imr < 0.2 mA	-4.2	-3.85	-3.5	VDC

DIGITAL INPUTS AND OUTPUTS

Input Low Voltage	V_{IL}	TTL			0.8	VDC
Input High Voltage	V_{IH}	TTL	2			VDC
Input Low Current	I_{IL}	V_{IL} = 0.8 V	-0.4	-0.2		mA
Input High Current	I_{IH}	V_{IH} = 2 V			100	µA
Inut Low Voltage	V_{IL2}	WDX, WDY	Vcc - 2.2		V_{IH2} - 0.25	VDC
Input High Voltage	V_{IH2}	WDX, WDY	Vcc - 1.08		Vcc - 0.5	VDC
Input Differential Voltage		V(WDX) - V(WDY)	0.3			VDC
Input Low Current	I_{IL2}	V_{IL2} = Vcc - 1.25 V		50		µA
Input High Current	I_{IH2}	V_{IH2} = Vcc - 0.75 V		50		µA
Output High Current	I_{OH}	WUS			50	µA
Output Low Current	I_{OL}	WUS		4		mA
Output Low Voltage	V_{OL}	WUS, I_{OL} = 4 mA			0.5	VDC

SERIAL PORT TIMING

Serial Clock Rate				20		MHz
SDEN_H to SCLK Delay	T_{SENSE}		30			ns
SDATA Set-up Time	T_{DS}		5			ns
SDATA Hold Time	T_{DH}		5			ns
SCLK Cycle Time	T_C		50			ns
SCLK High Time	T_{CKH}		20			ns
SCLK Low Time	T_{CKL}		20			ns
SDEN Hold Time	T_{SHLD}		25			ns
Time Between Operation	T_{SL}		100			ns
Duration of Head Select Programming	SDEN_H		855			ns

NOTE: SDEN_H assertion level is high.

READ CHARACTERISTICS, MR HEAD AMPLIFIER
Recommended operating conditions apply unless otherwise specified.

Imr = 10 mA, RMR = 30 Ω, Lhead = 75 nH, RDX/RDY Rload = 300 Ω Differential 300 µV < Vin < 3 mV; REF = 3.32 K is set for read & write current DAC 4.5 V < Vcc < 5.5 V < VEE < -4 V, CL (RDX, RDY) < 20 pF RL (RDX, RDY) > 1 K; 0° C < Temp < 70° C

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
MR Head Resistance		15	30	50	Ω
MR Inductance Range		35	50	75	nH
Imr Current Range		3.8	10	15.2	mA
Imr Absolute Accuracy	Include 1% ext. res.	-5		5	%
Imr Current Limit	Short to any other point			50	%
Vcm with Respect to GND		-50	0	50	mV
Differential Voltage Gain	Vin = 1 mVp-p @ 5 MHz	180	220	260	V/V
Voltage BW -1 dB	Rmr = 30 Ω	70			MHz
-3 dB		100			MHz
Input Noise Voltage	Exclude head noise			0.75	nV/rt.Hz
Noise Floor Variation	2 MHz < f < 100 MHz			3	dB
Differential Input Resistance	Vin = 1 mVp-p @ 5 MHz C2 = C3 = 0.1 µF	180	230		Ω
Differential Input Capacitance	Vin = 1 mVp-p @ 5 MHz C2 = C3 = 0.1 µF		10		pF
Input Dynamic Range	AC input voltage where gain falls to 90% of its small signal value, @ 5 MHz	5			mVp-p
VMR Gain			4		V/V
VMR Gain Tolerance		-2		2	%
VMR Input Referred Vos		-4		4	mV
Group Delay Variation	10 MHz < f < 80 MHz			0.5	ns
Group Delay Delta	Over Vcc/VEE/Temp			5	ns
CMRR	Vin = 100 mVp-p @ 5 MHz (2 MHz < f < 60 MHz)	55			dB
PSRR	100 mVp-p @ 5 MHz on Vcc or VEE	50			dB
Channel Separation	Unselected channels driven with 100 mVp-p @ 5 MHz	45			dB
Output Offset Voltage		-100		100	mV
RDX/RDY Source Impedance	@ 80 MHz			25	Ω
Load Impedance	Differential DC and AC	300			
Load Impedance	Single-ended DC to GND	1000			

READ CHARACTERISTICS, MR HEAD AMPLIFIER (continued)
Recommended operating conditions apply unless otherwise specified.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Output Resistance	Single-ended	35		75	Ω
Output Current		1.5		2.2	mA
RDX/RDY Common Mode Output Voltage			Vcc - 1.65		V
High Pass -3 dB Corner	CB1 = CB2 = 0.033 µF		320		kHz
Fast Mode Bandwidth Ratio		2:1	2.5:1	3:1	

WRITE CHARACTERISTICS
Recommended operating conditions apply unless otherwise specified. Iw = 20 mA, Lh = 150 nH, Rh = 17 Ω

Write Current Range		10		40	mA0-p
Iwc Absolute Accuracy	Includes 1% ext. res.	-10		10	%
Write Resistance Range		5		30	Ω
Write Inductance Range		100	220	300	nH
Write Coil CM Voltage			0		V
WDX/WDY Termination Resistance	Differential part of split π scheme	80			Ω
Differential Head Voltage Swing	Open head		9		Vp-p
Unselected Head Current	DC			0.1	mA
	AC			1	mApk
Head Differential					
Damping Resistance		670	900	1150	Ω
Head Differential Load Capacitance			15		pF
Upper Frequency Limit of Open Head Detector	Over Vcc/VEE/Temp Iwc = 25 mA, LCOIL = 25 nH RCOIL = 15 Ω	35			MHz

NOTE: Transition spacings shorter than 1/35 MHz = 28.6 ns will be masked out. Open head detector will respond to any transition spacings greater than 28.6 ns.

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

Imr = 10 mA, Rmr = 30 Ω, Lhead = 75 nH, RDX/RDY Rload = 300 Ω Differential, 300 µV < Vin < 3 mV; REF = 3.32 K is set for read & write current DAC, Iwc = 25 mA, Rcoil = 15 Ω, Lcoil = 150 nH, Fdata = 80 MHz, 4.5 V < Vcc < 5.5 V, -5.5 V < VEE < -4 V, CL (RDX, RDY) < 20 pF RL (RDX, RDY) > 1 K 0° C < Temp < 70° C

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Write Data to 90% Iwc Variation				0.1	ns
Write Data to 90% Iwc Asymmetry	Over Vcc/VEE/Temp measured from 50% front of rising edge to 50% of the falling edge			0.1	ns
Write Data to 90% Iwc Jitter				0.1	ns
Read to Write R/$\overline{W}$	To 90% of write current			100	ns
Write to Read R/$\overline{W}$	To 90% of 50 mV 5 MHz read signal envelope (see note)			1	µs
Idle to Read $\overline{CS}$	To 90% of 50 mV 5 MHz read signal envelope			7	µs
HSO, 1, 2, 3 to any MR	To 90% of 50 mV 5 MHz read signal envelope			5	µs
Safe to Unsafe (TD1) WUS	Write mode, from loss of WDX/WDY transition		0.7	1.4	µs
Unsafe to Safe (TD2) WUS	Fault cleared, from first positive (WDX/WDY) trans.			0.5	µs
Head Current (TD3) Ix-y	From 50% point		6	20	ns
Rise/Fall Time	With head, 20% to 80% Lhead = 150 nH Rhead = 15 Iwc = 25 mA		2	3	ns
Write Current Assymetry				0.5	ns
Iwc Turn-on Time	To 90% final value			100	ns
Iwc Turn-off Time	To 10% final value			100	ns
Iwc Settling Time	From R/$\overline{W}$ to within 5% Iwc			5	µs
Iwc and Imr Settling After Programming	From deassertion of SDEN_H to within 5% programmed Iwc			0.5	µs
Imr Turn-on Time	From MRR asserted to Imr within 5% of final value			5	µs
Head Switch Recovery	See note, full Rmr/Imr range			5	µs
Bias Turn-on Overshoot				0	%

NOTE: Read signal recovery criteria is defined in term of baseline and signal envelope. Recovery times are specified as the time it takes for the DC baseline at RdOut to settle within ±20 mV of its final value and the signal envelope at RdOut to settle within 90% of its final value (see Figure 2).

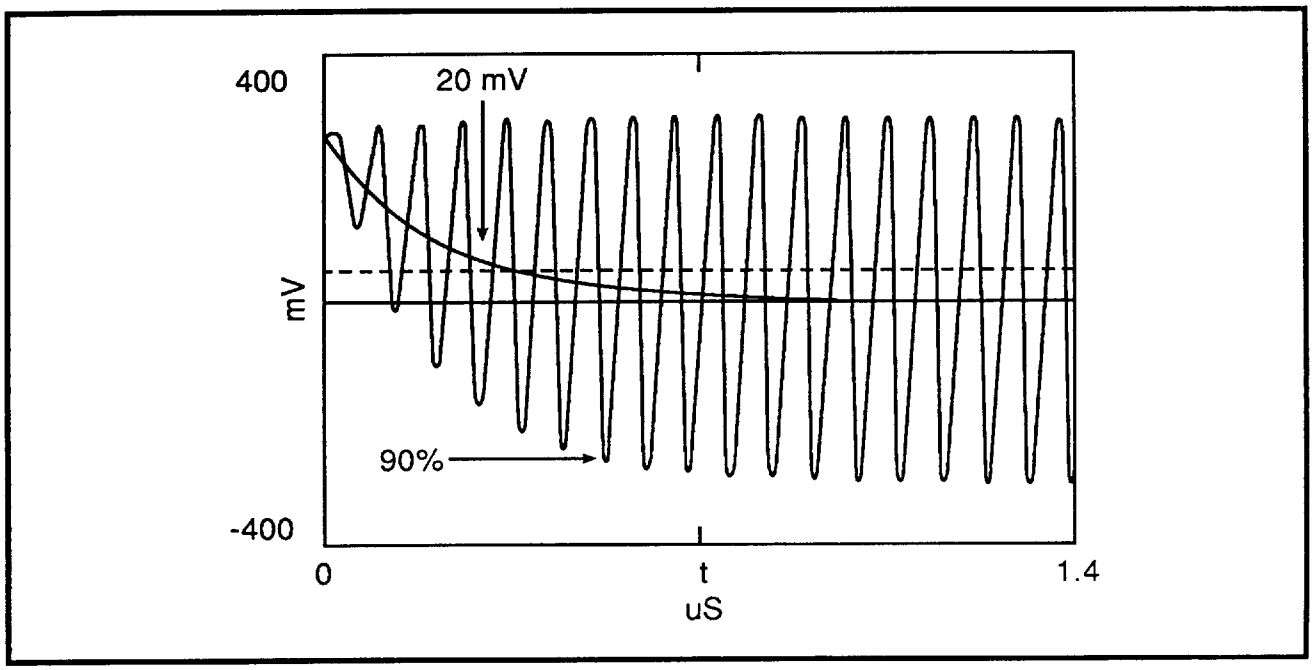


FIGURE 2: Read Recovery Data

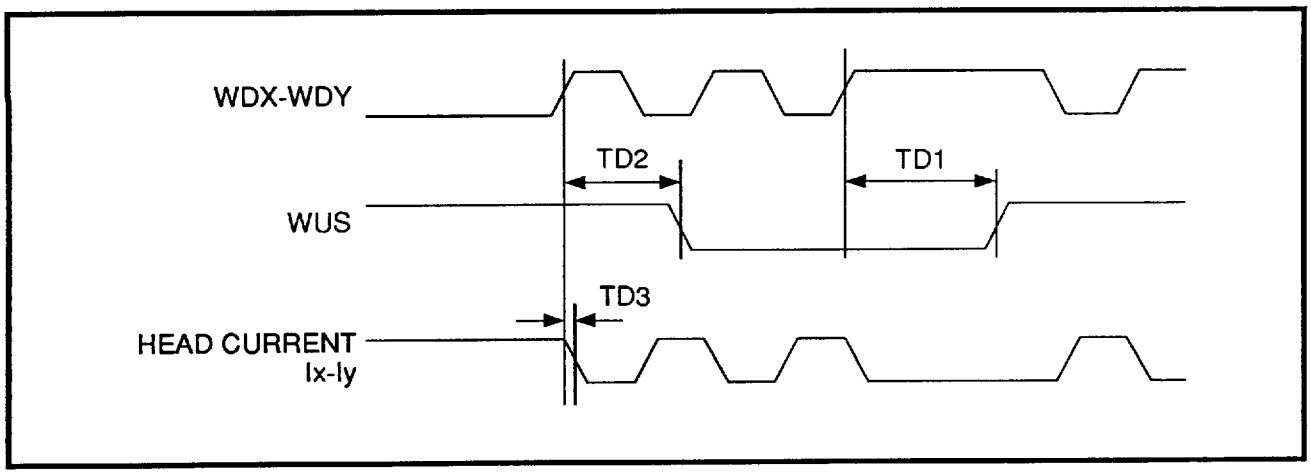
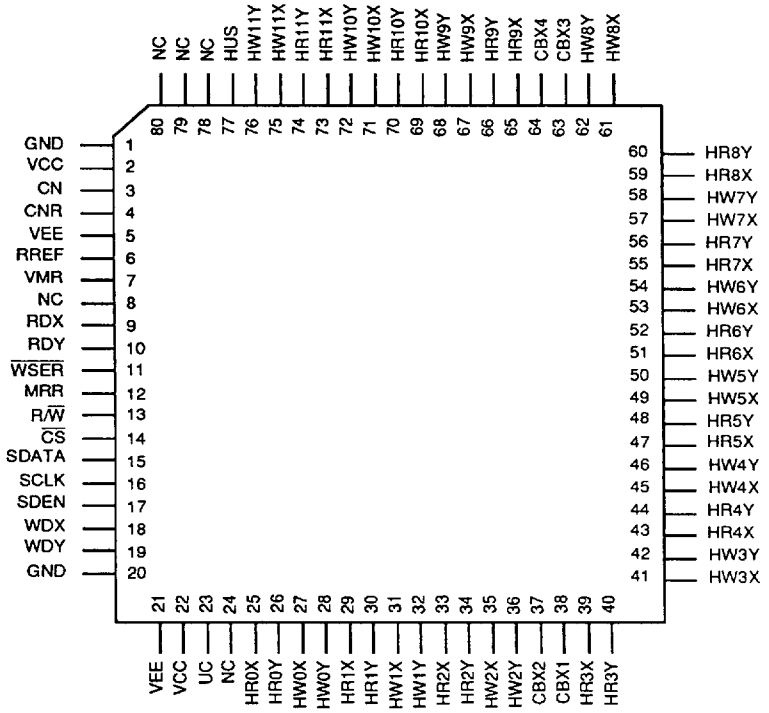


FIGURE 3: WUS Timing

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



SSI 32R1570AR-12 CGT
12-Channel
80-Lead TQFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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