



512Kx8 MONOLITHIC FLASH

PRELIMINARY*

FEATURES

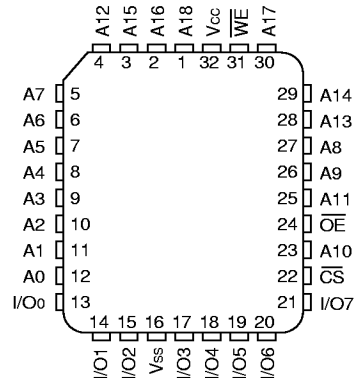
- Access Times of 70, 90, 120 and 150nS
- Packaging
 - 32 Lead, Plastic J-Leaded Chip Carrier PLCC
 - 32 Lead, Plastic Thin Small Outline Package TSOP
- Standard Commercial Off-The-Shelf (COTS) Memory Devices for Extended Temperature Range
- Electrical and Speed Characteristics for:
 - Military Temperature (-55°C to +125°C)
 - Industrial Temperature (-40°C to +85°C)
- Burn-in and Temperature Cycling Available
- Minimum 100,000 Erase/Program Cycles Guaranteed (0° to 70°C)

- Sector Erase Architecture
 - 8 equal size sectors of 64K bytes each
 - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Organized as 512Kx8
- 5 Volt Programming. 5V ±10% Supply.
- Low Power CMOS, 30mA Read Current, Typical
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Page Program Operation and Internal Program Control Time.

* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.

Note: Programming information available upon request.

PIN CONFIGURATIONS

32 TSOP (STANDARD)
TOP VIEW32 TSOP (REVERSE)
TOP VIEW32 PLCC
TOP VIEW

PIN DESCRIPTION

A0-18	Address Inputs
I/O0-7	Data Input/Output
CS	Chip Select
OE	Output Enable
WE	Write Enable
Vcc	+5.0V Power
Vss	Ground

PLASTIC PLUS FLASH



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage (V _{CC}) (1)	-2.0 to +7.0	V
Signal Voltage Range(any pin except A ₉) (2)	-2.0 to +7.0	V
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10 seconds)	+300	°C
Data Retention	10 years	
Endurance (erase/program cycles)	10,000	
A ₉ Voltage for sector protect (V _{IO}) (3)	-2.0 to +14.0	V

NOTES:

- Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot V_{SS} to -2.0 V for periods of up to 20nS. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods of up to 20nS.
- Minimum DC input voltage on A₉ pin is -0.5V. During voltage transitions, A₉ may overshoot V_{SS} to -2V for periods of up to 20nS. Maximum Dc input voltage on A₉ is +13.5V which may overshoot to 14.0 V for periods up to 20nS.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.0	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C
Operating Temp. (Ind.)	T _A	-40	+85	°C
A ₉ Volatage for Sector Protect	V _{IO}	11.5	12.5	V

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
Address Input capacitance	C _{AD}	V _{IO} = 0 V, f = 1.0 MHz	15	pF
Output Enable capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	15	pF
Write Enable capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	15	pF
Chip Select capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	15	pF
Data I/O capacitance	C _{IO}	V _{IO} = 0 V, f = 1.0 MHz	15	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min		Unit
				Max	
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LOx32}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
V _{CC} Active Current for Read (1)	I _{CC1}	$\overline{CS} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 5MHz		50	mA
V _{CC} Active Current for Program or Erase (2)	I _{CC2}	$\overline{CS} = V_{IL}$, $\overline{OE} = V_{IH}$		60	mA
V _{CC} Standby Current	I _{CC4}	V _{CC} = 5.5, $\overline{CS} = V_{IH}$, f = 5MHz		1.6	mA
Output Low Voltage	V _{OL}	I _{OL} = 12.0 mA, V _{CC} = 4.5		0.45	V
Output High Voltage	V _{OH1}	I _{OH} = -2.5 mA, V _{CC} = 4.5	0.85 x V _{CC}		V
Low V _{CC} Lock-Out Voltage	V _{LKO}		3.2	4.2	V

NOTES:

- The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
- I_{CC} active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

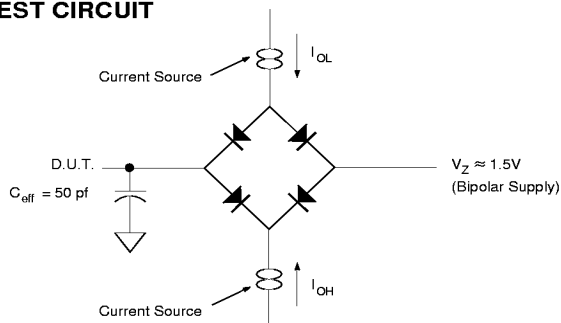


AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED

($V_{CC} = 5.0V$, $V_{SS} = 0V$, $T_A = -55^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	70		90		120		150		nS
Write Enable Setup Time	tWLLE	tWS	0		0		0		0		nS
Chip Select Pulse Width	tELEH	tCP	45		45		50		50		nS
Address Setup Time	tAVEL	tAS	0		0		0		0		nS
Data Setup Time	tDVEH	tDS	45		45		50		50		nS
Data Hold Time	tEHDX	tDH	0		0		0		0		nS
Address Hold Time	tELAX	tAH	45		45		50		50		nS
Chip Select Pulse Width High	tEHLE	tCPH	20		20		20		20		nS
Duration of Byte Programming Operation	tWHWH1		16		16		16		16		μ S
Sector Erase Time	tWHWH2			30		30		30		30	Sec
Read Recovery Time	tGHLE		0		0		0		0		μ S
Chip Programming Time				50		50		50		50	Sec
Chip Erase Time	tWHWH2			120		120		120		120	Sec

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0$, $V_{IH} = 3.0$	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.

I_{OL} & I_{OH} programmable from 0 to 16mA.

Tester Impedance $Z_0 = 75 \Omega$.

V_Z is typically the midpoint of V_{OH} and V_{OL} .

I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.

ATE tester includes jig capacitance.



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{WE}$ CONTROLLED

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol		<u>-70</u>		<u>-90</u>		<u>-120</u>		<u>-150</u>		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	70		90		120		150		nS
Chip Select Setup Time	t _{ELWL}	t _{CS}	0		0		0		0		nS
Write Enable Pulse Width	t _{WLWH}	t _{WP}	45		45		50		50		nS
Address Setup Time	t _{AVWH}	t _{AS}	0		0		0		0		nS
Data Setup Time	t _{DVWH}	t _{DS}	45		45		50		50		nS
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		0		nS
Address Hold Time	t _{WHAX}	t _{AH}	45		45		50		50		nS
Write Enable Pulse Width High	t _{WHWL}	t _{WPH}	20		20		20		20		nS
Duration of Byte Programming Operation	t _{WHWH1}		16		16		16		16		μS
Sector Erase Time	t _{WHWH2}			30		30		30		30	Sec
Read Recovery Time before Write	t _{GHWL}		0		0		0		0		μS
V _{CC} Set-up Time	t _{VCS}		50		50		50		50		μS
Chip Programming Time				50		50		50		50	Sec
Output Enable Setup Time		t _{OES}	0		0		0		0		nS
Output Enable Hold Time (1)		t _{OEH}	10		10		10		10		nS
Chip Erase Time	t _{WHWH2}			120		120		120		120	Sec

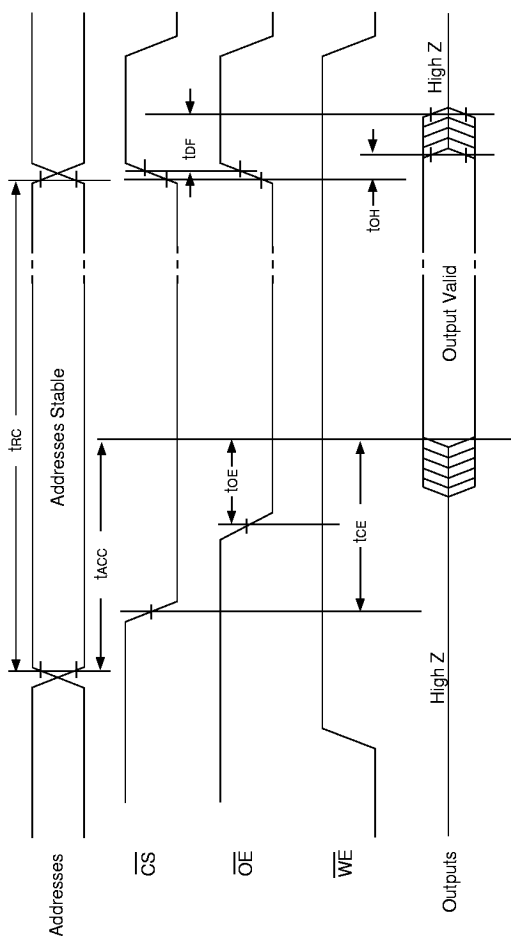
1. For Toggle and Data Polling.

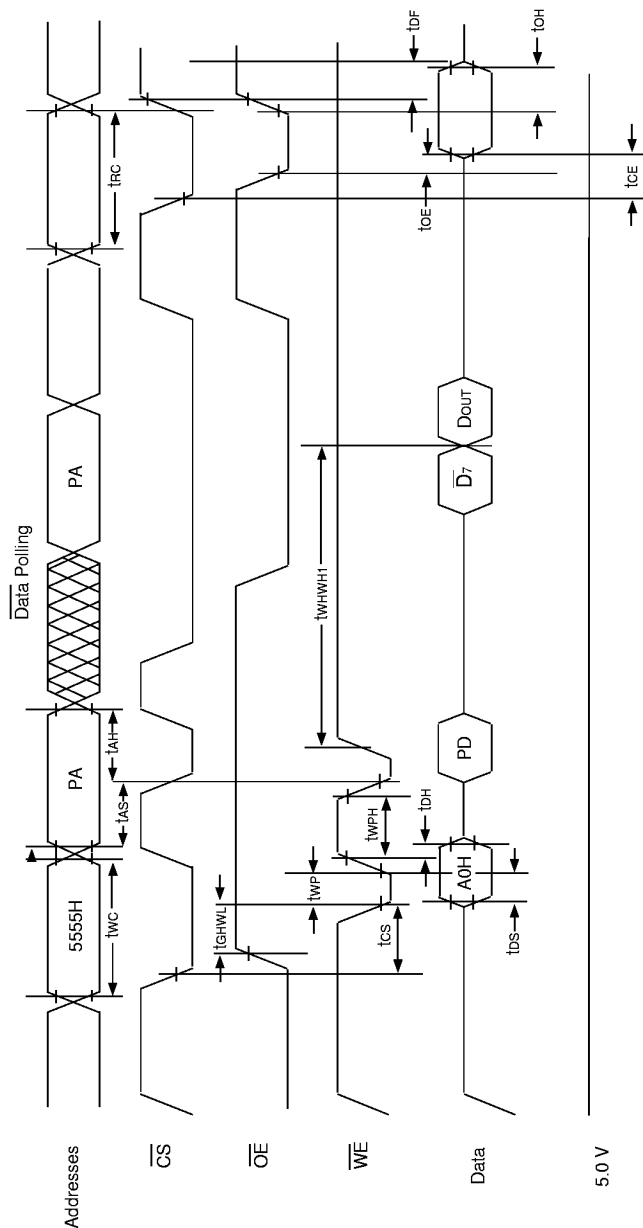
AC CHARACTERISTICS – READ ONLY OPERATIONS

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

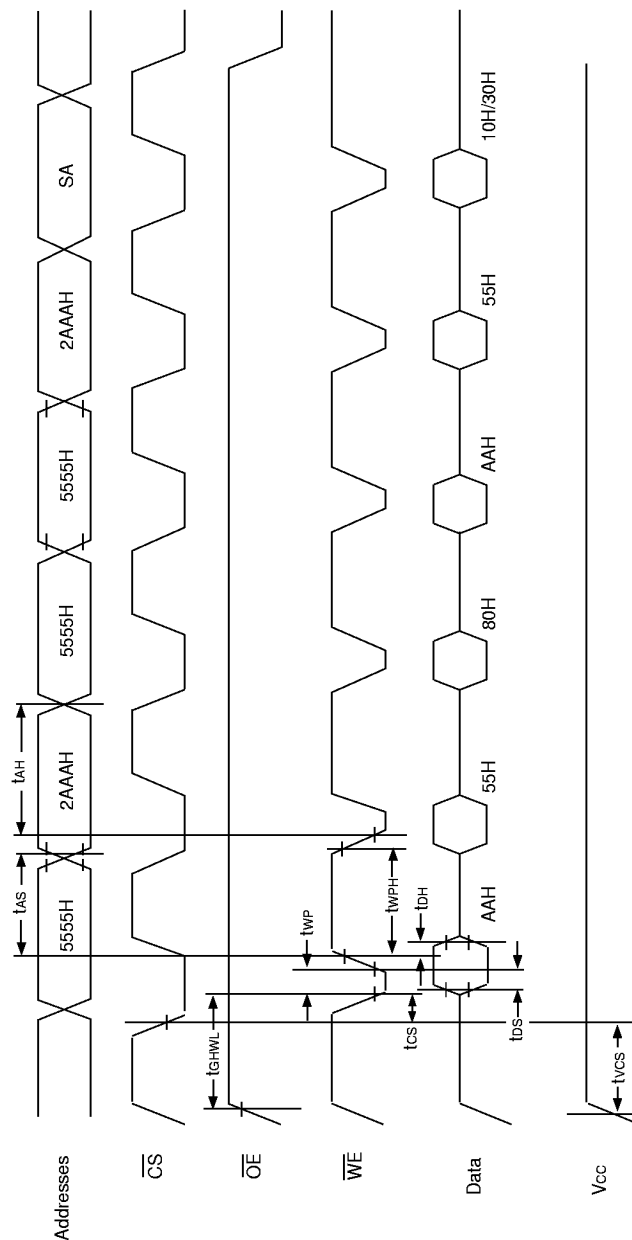
Parameter	Symbol		<u>-70</u>		<u>-90</u>		<u>-120</u>		<u>-150</u>		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	70		90		120		150		nS
Address Access Time	t _{AVQV}	t _{ACC}		70		90		120		150	nS
Chip Select Access Time	t _{ELQV}	t _{CE}		70		90		120		150	nS
Output Enable to Output Valid	t _{GLQV}	t _{OE}		35		35		50		55	nS
Chip Select to Output High Z (1)	t _{EHQZ}	t _{DF}		20		20		30		35	nS
Output Enable High to Output High Z (1)	t _{GHQZ}	t _{DF}		20		20		30		35	nS
Output Hold from Address, $\overline{CS}$ or $\overline{OE}$ Change, whichever is First	t _{AXQX}	t _{OH}	0		0		0		0		nS

1. Guaranteed by design, but not tested

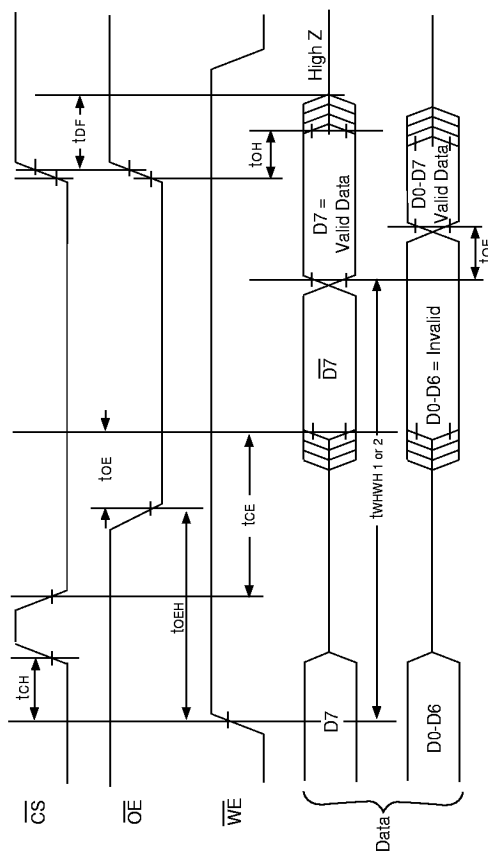
**AC WAVEFORMS FOR READ OPERATIONS**

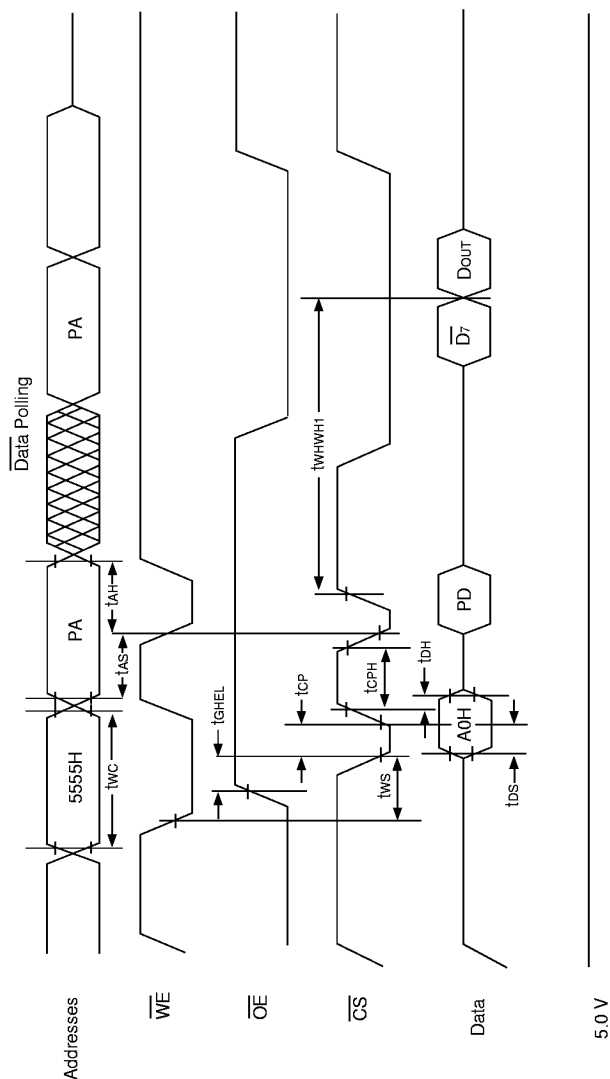
**WRITE/ERASE/PROGRAM
OPERATION, WE CONTROLLED****NOTES:**

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D7 is the output of the complement of the data written to the device.
4. Dout is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

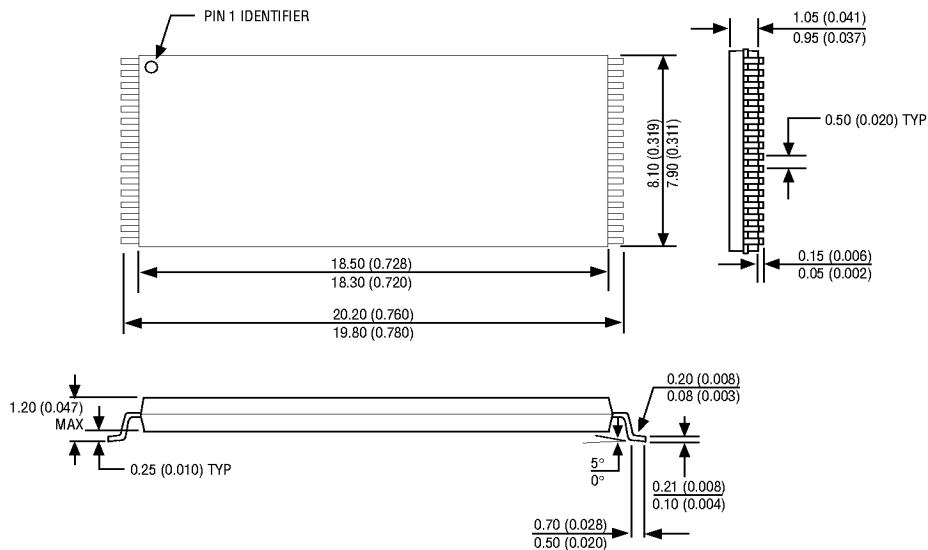
**AC WAVEFORMS CHIP/SECTOR
ERASE OPERATIONS****NOTE:**

1. SA is the sector address for Sector Erase.

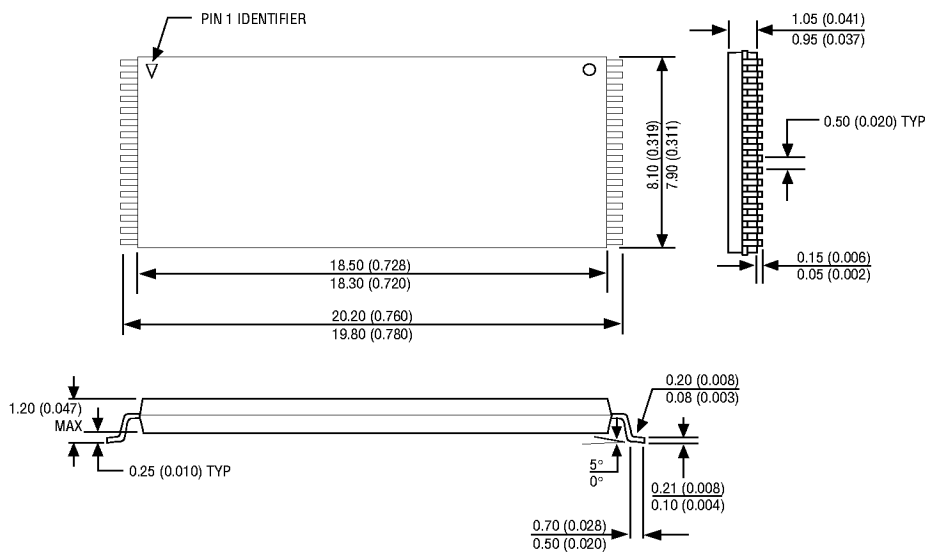
**AC WAVEFORMS FOR DATA POLLING
DURING EMBEDDED ALGORITHM OPERATIONS**

**ALTERNATE $\overline{CS}$ CONTROLLED
PROGRAMMING OPERATION TIMINGS****NOTES:**

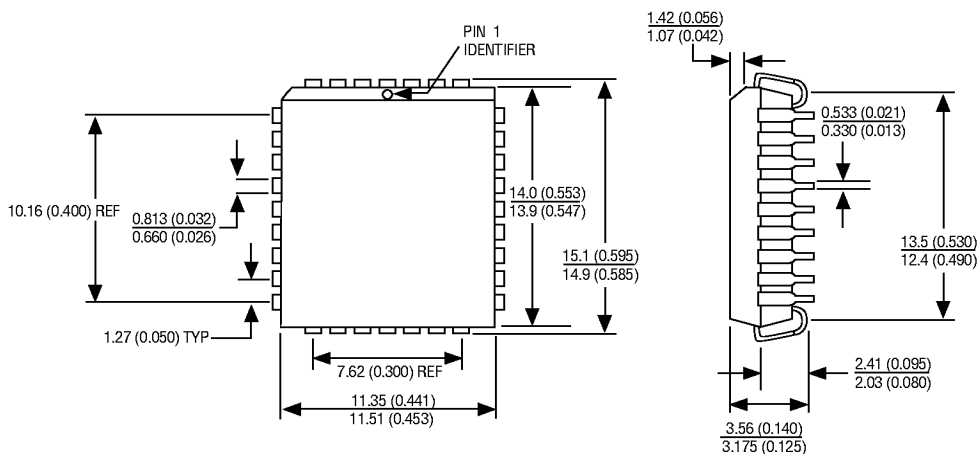
1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. D7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

**32 LEAD, STANDARD PLASTIC TSOP PACKAGE DIMENSION**

DIMENSIONS IN MILLIMETERS AND (INCHES)

32 LEAD, REVERSED PLASTIC TSOP PACKAGE DIMENSION

DIMENSIONS IN MILLIMETERS AND (INCHES)

**32 LEAD, PLASTIC J-LEADED PLCC PACKAGE DIMENSION**

DIMENSIONS IN MILLIMETERS AND (INCHES)

ORDERING INFORMATION**W P F 512K 8 X - XXX X X 5****V_{PP} PROGRAMMING VOLTAGE**

5 = 5 V

DEVICE GRADE:

M = Military Temperature -55°C to +125°C

I = Industrial Temperature -40°C to +85°C

PACKAGE:

TF= 32 lead Plastic TSOP

TR= 32 lead Plastic TSOP Reverse

PL= 32 lead Plastic LCC (J-lead)

ACCESS TIME in nS**IMPROVEMENT MARK**

B = Burn-in

T = Temperature Cycle

C = Burn-in and Temp Cycle

ORGANIZATION, 512K x 8**FLASH****PLASTIC PLUS™****WHITE MICROELECTRONICS**