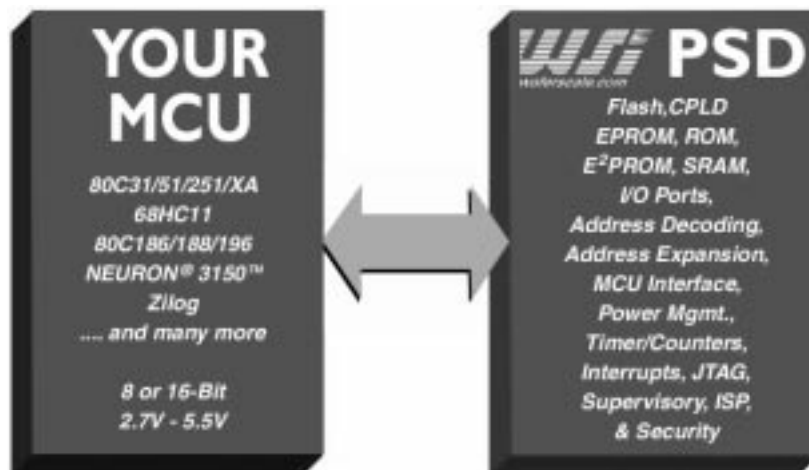


PSD813F Family

PSD813F ZPSD813F ZPSD813FV

Flash In-System-Programmable Microcontroller Peripherals

***June, 1999
Preliminary***



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PSD813F Family

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Flash In-System-Programmable Microcontroller Peripherals

Table of Contents

1.0	Introduction	1
2.0	Key Features	2
	PSD813F Block Diagram	4
3.0	General Information	5
4.0	PSD813F Family	5
5.0	PSD813F Architectural Overview	6
	5.1 Memory	6
	5.2 Page Register	6
	5.3 PLDs	6
	5.4 I/O Ports	7
	5.5 Microcontroller Bus Interface	7
	5.6 JTAG Port	7
	5.7 In-System Programming	8
	5.8 Power Management	8
6.0	Development System	9
7.0	PSD813F Pin Descriptions	10
8.0	PSD813F Register Description and Address Offset	14
9.0	PSD813F Functional Blocks	15
	9.1 Memory Blocks	15
	9.1.1 Main Flash and Optional Secondary EEPROM or Flash Boot Memory Description	15
	9.1.2 SRAM	30
	9.1.3 Memory Select Signals	30
	9.1.4 Page Register	35
	9.2 PLDs	36
	9.2.1 Decode PLD (DPLD)	38
	9.2.2 Complex PLD (CPLD)	38
	9.3 Microcontroller Bus Interface	47
	9.3.1 Interfacing 16-bit MCUs with Two PSD813F Devices	47
	9.3.2 PSD813F Interface to a Multiplexed 8-bit Bus	47
	9.3.3 PSD813F Interface to a Non-Multiplexed 8-bit Bus	47
	9.3.4 Data Byte Enable Reference	50
	9.3.5 Microcontroller Interface Examples	50
	9.4 I/O Ports	55
	9.4.1 General Port Architecture	55
	9.4.2 Port Operating Modes	57
	9.4.3 Port Configuration Registers (PCRs)	60
	9.4.4 Port Data Registers	63
	9.4.5 Ports A and B – Functionality and Structure	64
	9.4.6 Port C – Functionality and Structure	66
	9.4.7 Port D – Functionality and Structure	66
	9.5 Power Management	70
	9.5.1 Automatic Power Down (APD) Unit and Power Down Mode	70
	9.5.2 Other Power Saving Options	74
	9.5.3 Reset Input	75



PSD813F Family
PSD813F ZPSD813F ZPSD813FV
Flash In-System-Programmable Microcontroller Peripherals

Table of Contents (cont.)

9.6 Programming In-Circuit Using the JTAG Interface	76
9.6.1 Standard JTAG Signals.....	77
9.6.2 JTAG Extensions.....	78
9.6.3 Security and Flash Memories and EEPROM Protection	78
Absolute Maximum Ratings.....	79
AD/DC Parameters.....	80
Example of PSD813F Typical Power Calculation at $V_{CC} = 5.0\text{ V}$	81
Example of ZPSD813F Typical Power Calculation at $V_{CC} = 5.0\text{ V}$	82
PSD813F/ZPSD813F DC Characteristics (5 V \pm 10% Versions)	83
PSD813F DC Characteristics (I_{CC}).....	84
ZPSD813F DC Characteristics (I_{CC}).....	84
PSD813F AD/DC Parameters – CPLD Timing Parameters (5 V \pm 10% versions)	85
ZPSD813FV DC Characteristics (3 V \pm 10% Versions).....	95
ZPSD813FV AC/DC Parameters – CPLD Timing Parameters (3 V \pm 10% versions)	96
Timing Diagrams	104
Programming.....	111
PSD813F Pin Assignments	112
PSD813F Package Information	114
Selector Guide.....	117
Part Number Construction.....	118
Ordering Information.....	118
Temporary Exceptions to Specifications	122
Product Revisions.....	124
Worldwide Sales, Service and Technical Support.....	128

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Programmable Peripheral PSD813F Family

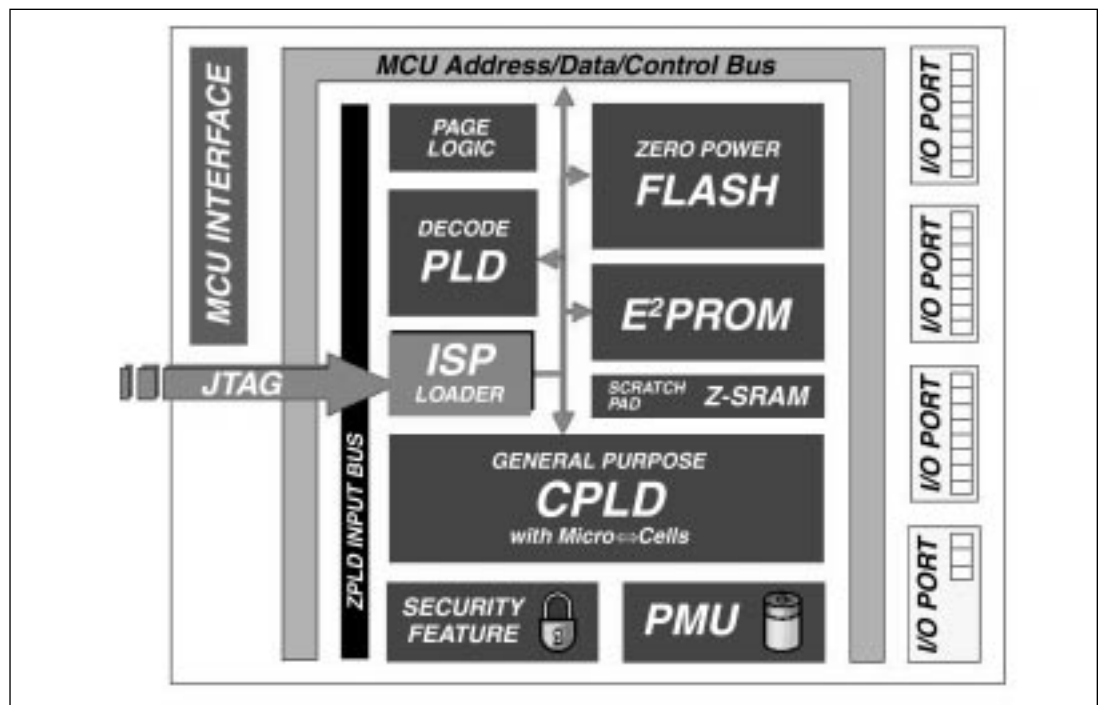
PSD813F ZPSD813F ZPSD813FV
Flash In-System-Programmable
Microcontroller Peripherals

Preliminary

1.0 Introduction

The PSD813F family of Programmable Microcontroller (MCU) Peripherals brings In-System-Programmability (ISP) to Flash memory and programmable logic. The result is a simple and flexible solution for embedded designs. PSD813F devices combine many of the peripheral functions found in MCU based applications:

- 1 Mbit of Flash memory
- A second EEPROM or Flash memory
- Over 3,000 gates of Flash programmable logic
- SRAM
- Reconfigurable I/O ports
- Programmable power management.



PSD813F devices integrate an optimized “microcontroller macrocell” logic architecture called the Micro↔Cell™. The Micro↔Cell was created to address the unique requirements of embedded system designs. It allows direct connection between the system address/data bus and the internal PSD registers to simplify communication between the MCU and other supporting devices.

Updated June 18, 1999. See page 124.

For lowest power operation refer to the ZPSD813F/813FV products.

1.0 Introduction (Cont.)

The PSD813F family includes a JTAG serial programming interface to allow in-system-programming of the **entire device**. This feature reduces development time, simplifies the manufacturing flow, and dramatically lowers the cost of field upgrades. Using WSI's special Fast-JTAG programming, a design can be programmed into the PSD813F in as little as seven seconds.

The innovative Flash PSD813F family solves key problems faced by designers when managing discrete Flash memory devices, such as:

- First-time programming
- Complex address decoding
- Simultaneous read and write to Flash.

The PSD813F's serial JTAG interface allows in-system-programming and eliminates the need for a boot EPROM or an external programmer. To simplify Flash updates, the PSD813F1, PSD813F2, and PSD813F4 devices perform program execution out of a secondary EEPROM (F1) or Flash (F2/F4) memory block while the main Flash memory is being updated. This solution avoids the complicated overhead circuitry and software necessary to implement in-system Flash memory updates.

PSDsoft —WSI's software development tool—now has the ability to generate ANSI-C compliant code for use with your target MCU. The code generated allows you to manipulate the non-volatile memory (NVM) within the PSD. Code examples are also provided for:

- Flash ISP via the UART of the host MCU
- Memory paging to execute code across several PSD memory pages
- Loading, reading, and manipulation of PSD Micro \leftrightarrow Cells by the MCU

The PSD813F is available in a 52-pin PLCC package and a 64-pin plastic Thin Quad Flatpack (TQFP) package.

2.0 Key Features

- A simple interface to 8-bit microcontrollers that use either multiplexed or non-multiplexed busses. The bus interface logic uses the control signals generated by the microcontroller automatically when the address is decoded and a read or write is performed. A partial list of the MCU families supported include:
 - Intel 8031, 80196, 80186, 80C251, and 80386EX
 - Motorola 68HC11, 68HC16, 68HC12, and 683XX
 - Philips 8031 and 8051XA
 - Zilog Z80 and Z8
 - NEURON[®] 3150 CHIP[™].
- Internal 1 Mbit Flash memory. This is the main Flash memory. It is divided into eight equal-sized blocks that can be accessed with user-specified addresses.
- Optional internal secondary 256 Kbit EEPROM or Flash boot memory. It is divided into four equal-sized blocks that can be accessed with user-specified addresses. This secondary memory brings the ability to execute code and update the main Flash **concurrently**.
- Optional 16 Kbit scratchpad SRAM. The SRAM's contents can be protected from a power failure by connecting an external battery.

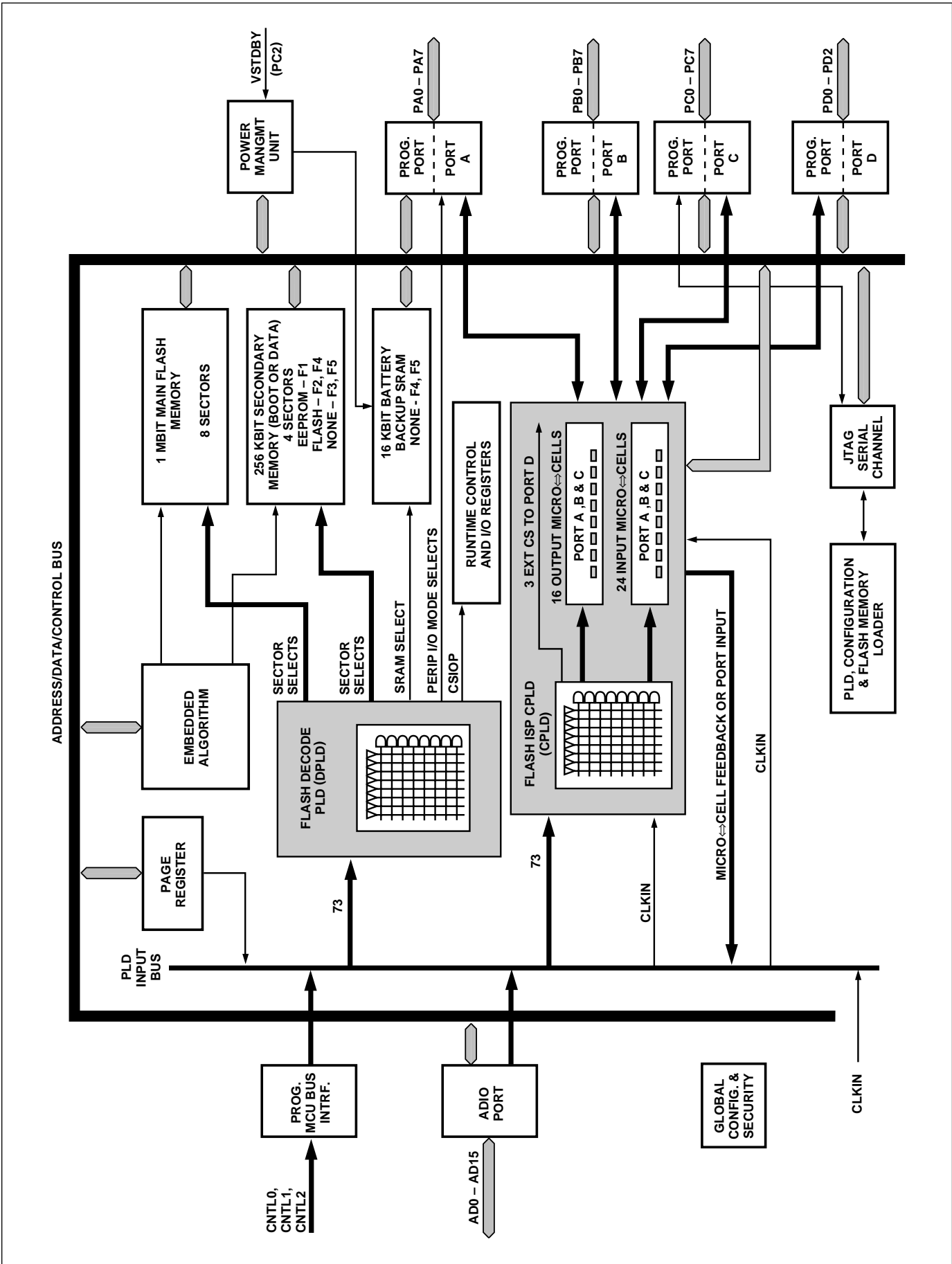
Please refer to the revision block at the end of this document for updated information.



2.0 Key Features (cont.)

- Optional 64 byte One Time Programmable (OTP) memory that can be used for product configuration and calibration.
- CPLD with 16 Output Micro↔Cells (OMCs) and 24 Input Micro↔Cells (IMCs). The CPLD may be used to efficiently implement a variety of logic functions for internal and external control. Examples include state machines, loadable shift registers, and loadable counters.
- Decode PLD (DPLD) that decodes address for selection of internal memory blocks. The DPLD can also be used to generate external chip selects.
- 27 individually configurable I/O port pins that can be used for the following functions:
 - MCU I/Os
 - PLD I/Os
 - Latched MCU address output
 - Special function I/Os.
 - 16 of the I/O ports may be configured as open-drain outputs.
- Standby current as low as 50 μ A for 5 V devices, 25 μ A for 3 V devices.
- Built-in JTAG compliant serial port allows full-chip In-System Programmability (ISP). With it, you can program a blank device or reprogram a device in the factory or the field.
- Internal page register that can be used to expand the microcontroller address space by a factor of 256.
- Internal programmable Power Management Unit (PMU) that supports a low power mode called Power Down Mode. The PMU can automatically detect a lack of microcontroller activity and put the PSD813F into Power Down Mode.
- Erase/Write cycles:
 - Flash memory – 100,000 minimum
 - EEPROM – 10,000 minimum
 - PLD – 1,000 minimum

Figure 1. PSD813F Block Diagram



3.0 General Information

The PSD813F series architecture allows In-System Programming of all Memory, PLD Logic and Device Configuration. The embedded Input and Output Micro \leftrightarrow Cells enable efficient implementation of user defined logic functions that require both software and hardware interaction. The devices eliminate the need for discrete 'glue' logic, and allow the development of entire systems using only a few highly integrated devices.

4.0 PSD813F Family

There are 5 variants in the PSD813F family. All PSD813F devices provide these base features: 1 Mbit main Flash Memory, JTAG port, CPLD, DPLD, power management, and 27 I/O pins. The following statements show what each PSD813F family member adds to this set of basic features:

- PSD813F1** Adds 256 Kbits EEPROM and 16 Kbits SRAM to the base feature set. These independent memories can operate concurrently with each other and with the main Flash memory. The PSD813F1 also adds 64 bytes of OTP memory for any use (product serial number, calibration constants, etc.). Once written, the OTP memory can never be altered.
- PSD813F2** Adds 256 Kbits Flash memory and 16 Kbits SRAM to the base feature set. These independent memories can operate concurrently with each other and with the main Flash memory.
- PSD813F3** Adds 16 Kbits SRAM to the base feature set. This independent memory can operate concurrently with the main Flash memory.
- PSD813F4** Adds 256 Kbits Flash memory to the base feature set. This independent memory can operate concurrently with the main Flash memory.
- PSD813F5** No additions to base feature set.

The following table summarizes all the devices in the PSD813F family. The ZPSD family members offer extra power savings features (slight penalty to memory access time and PLD propagation delay).

Table 1. PSD813F Product Matrix

Part #		I/O Pins	No. of Micro \leftrightarrow Cells Input/Output	Serial ISP JTAG/ISC Port	Flash Main Memory Kbit (8 Sectors)	Additional Memory for Boot and/or Data (4 Sectors)	SRAM Kbit	Turbo Mode	Supply Voltage
PSD813F Family	Device								
PSD813F	PSD813F1	27	24/16	Yes	1024	256 Kbit EEPROM	16	–	5V
	PSD813F2	27	24/16	Yes	1024	256 Kbit Flash	16	–	5V
	PSD813F3	27	24/16	Yes	1024	None	16	–	5V
	PSD813F4	27	24/16	Yes	1024	256 K Bit Flash	None	–	5V
	PSD813F5	27	24/16	Yes	1024	None	None	–	5V
ZPSD813F	ZPSD813F1	27	24/16	Yes	1024	256 Kbit EEPROM	16	Yes	5V
	ZPSD813F2	27	24/16	Yes	1024	256 Kbit Flash	16	Yes	5V
	ZPSD813F3	27	24/16	Yes	1024	None	16	Yes	5V
	ZPSD813F4	27	24/16	Yes	1024	256 K Bit Flash	None	Yes	5V
	ZPSD813F5	27	24/16	Yes	1024	None	None	Yes	5V
ZPSD813FV	ZPSD813F1V	27	24/16	Yes	1024	256 Kbit EEPROM	16	Yes	3V
	ZPSD813F2V	27	24/16	Yes	1024	256 Kbit Flash	16	Yes	3V
	ZPSD813F3V	27	24/16	Yes	1024	None	16	Yes	3V
	ZPSD813F4V	27	24/16	Yes	1024	256 K Bit Flash	None	Yes	3V
	ZPSD813F5V	27	24/16	Yes	1024	None	None	Yes	3V

5.0 PSD813F Architectural Overview

PSD813F devices contain several major functional blocks. Figure 1 on page 3 shows the architecture of the PSD813F device family. The functions of each block are described briefly in the following sections. Many of the blocks perform multiple functions and are user configurable.

5.1 Memory

The PSD813F contains the following memories:

- A 1 Mbit Flash
- An optional secondary 256 Kbit EEPROM or Flash boot memory
- An optional 16 Kbit SRAM.

Each of the memories is briefly discussed in the following paragraphs. A more detailed discussion can be found in section 9.

The 1 Mbit Flash is the main memory of the PSD813F. It is divided into eight equally-sized sectors that are individually selectable.

The optional 256 Kbit EEPROM or Flash is divided into four equally-sized sectors. Each sector is individually selectable.

The optional 16 Kbit SRAM is intended for use as a scratchpad memory or as an extension to the microcontroller SRAM. If an external battery is connected to the PSD813F's Vstby pin, data will be retained in the event of a power failure.

Each block of memory can be located in a different address space as defined by the user. The access times for all memory types includes the address latching and DPLD decoding time.

5.2 Page Register

The eight-bit Page Register expands the address range of the microcontroller by up to 256 times. The paged address can be used as part of the address space to access external memory and peripherals or internal memory and I/O. The Page Register can also be used to change the address mapping of blocks of Flash memory into different memory spaces for in-circuit reprogramming.

5.3 PLDs

The device contains two PLD blocks, each optimized for a different function, as shown in Table 2. The functional partitioning of the PLDs reduces power consumption, optimizes cost/performance, and eases design entry.

The Decode PLD (DPLD) is used to decode addresses and generate chip selects for the PSD813F internal memory and registers. The CPLD can implement user-defined logic functions. The DPLD has combinatorial outputs. The CPLD has 16 Output Micro \leftrightarrow Cells and 3 combinatorial outputs. The PSD813F also has 24 Input Micro \leftrightarrow Cells that can be configured as inputs to the PLDs. The PLDs receive their inputs from the PLD Input Bus and are differentiated by their output destinations, number of Product Terms, and Micro \leftrightarrow Cells.

The PLDs consume minimal power by using Zero-Power design techniques. The speed and power consumption of the PLD is controlled by the Turbo Bit (ZPSD only) in the PMMR0 register and other bits in the PMMR2 registers. These registers are set by the microcontroller at runtime. There is a slight penalty to PLD propagation time when invoking the ZPSD features.

Table 2. PLD I/O Table

<i>Name</i>	<i>Abbreviation</i>	<i>Inputs</i>	<i>Outputs</i>	<i>Product Terms</i>
Decode PLD	DPLD	73	17	42
Complex PLD	CPLD	73	19	140

PSD813F Architectural Overview (cont.)

5.4 I/O Ports

The PSD813F has 27 I/O pins divided among four ports (Port A, B, C, and D). Each I/O pin can be individually configured for different functions. Ports A, B, C and D can be configured as standard MCU I/O ports, PLD I/O, or latched address outputs for microcontrollers using multiplexed address/data busses.

The JTAG pins can be enabled on Port C for In-System Programming (ISP).

Ports A and B can also be configured as a data port for a non-multiplexed bus or multiplexed Address/Data buses for certain types of 16-bit microcontrollers.

5.5 Microcontroller Bus Interface

The PSD813F easily interfaces with most 8-bit microcontrollers that have either multiplexed or non-multiplexed address/data busses. The device is configured to respond to the microcontroller's control signals, which are also used as inputs to the PLDs. Where there is a requirement to use a 16-bit data bus to interface to a 16-bit microcontroller, two PSDs must be used. Section 9.3.5 contains microcontroller interface examples.

5.6 JTAG Port

In-System Programming can be performed through the JTAG pins on Port C. This serial interface allows complete programming of the entire PSD813F device. A blank device can be completely programmed. The JTAG signals (TMS, TCK, $\overline{\text{TSTAT}}$, $\overline{\text{TERR}}$, TDI, TDO) can be multiplexed with other functions on Port C. Table 3 indicates the JTAG signals pin assignments.

Table 3. JTAG Signals on Port C

Port C Pins	JTAG Signal
PC0	TMS
PC1	TCK
PC3	$\overline{\text{TSTAT}}$
PC4	$\overline{\text{TERR}}$
PC5	TDI
PC6	TDO

PSD813F Architectural Overview (cont.)

5.7 In-System Programming

Using the JTAG signals on Port C, the entire PSD813F device can be programmed or erased without the use of the microcontroller. The main Flash memory can also be programmed in-system by the microcontroller executing the programming algorithms out of the optional EEPROM, Flash Boot memory, or SRAM. The optional EEPROM or Flash Boot memory can be programmed the same way by executing out of the main Flash memory. The PLD logic or other PSD813F configuration can be programmed through the JTAG port or a device programmer. Table 4 indicates which programming methods can program different functional blocks of the PSD813F.

Table 4. Methods of Programming Different Functional Blocks of the PSD813F

Functional Block	JTAG Programming	Device Programmer	In-System Parallel Programming
Main Flash memory	Yes	Yes	Yes
Optional EEPROM/Flash Boot memory	Yes	Yes	Yes
PLD Array (DPLD and CPLD)	Yes	Yes	No
PSD Configuration	Yes	Yes	No
Optional OTP Row	No	Yes	Yes

5.8 Power Management Unit

The Power Management Unit (PMU) in the PSD813F gives the user control of the power consumption on selected functional blocks based on system requirements. The PMU includes an Automatic Power Down unit (APD) that will turn off device functions due to microcontroller inactivity. The APD unit has a Power Down Mode that helps reduce power consumption.

The ZPSD813F also has some bits that are configured at run-time by the MCU to reduce power consumption of the CPLD. The turbo bit in the PMMR0 register can be turned off and the CPLD will latch its outputs and go to sleep until the next transition on its inputs. Additionally, bits in the PMMR2 register can be set by the MCU to block signals from entering the CPLD to reduce power consumption. See section 9.5.

6.0 Development System

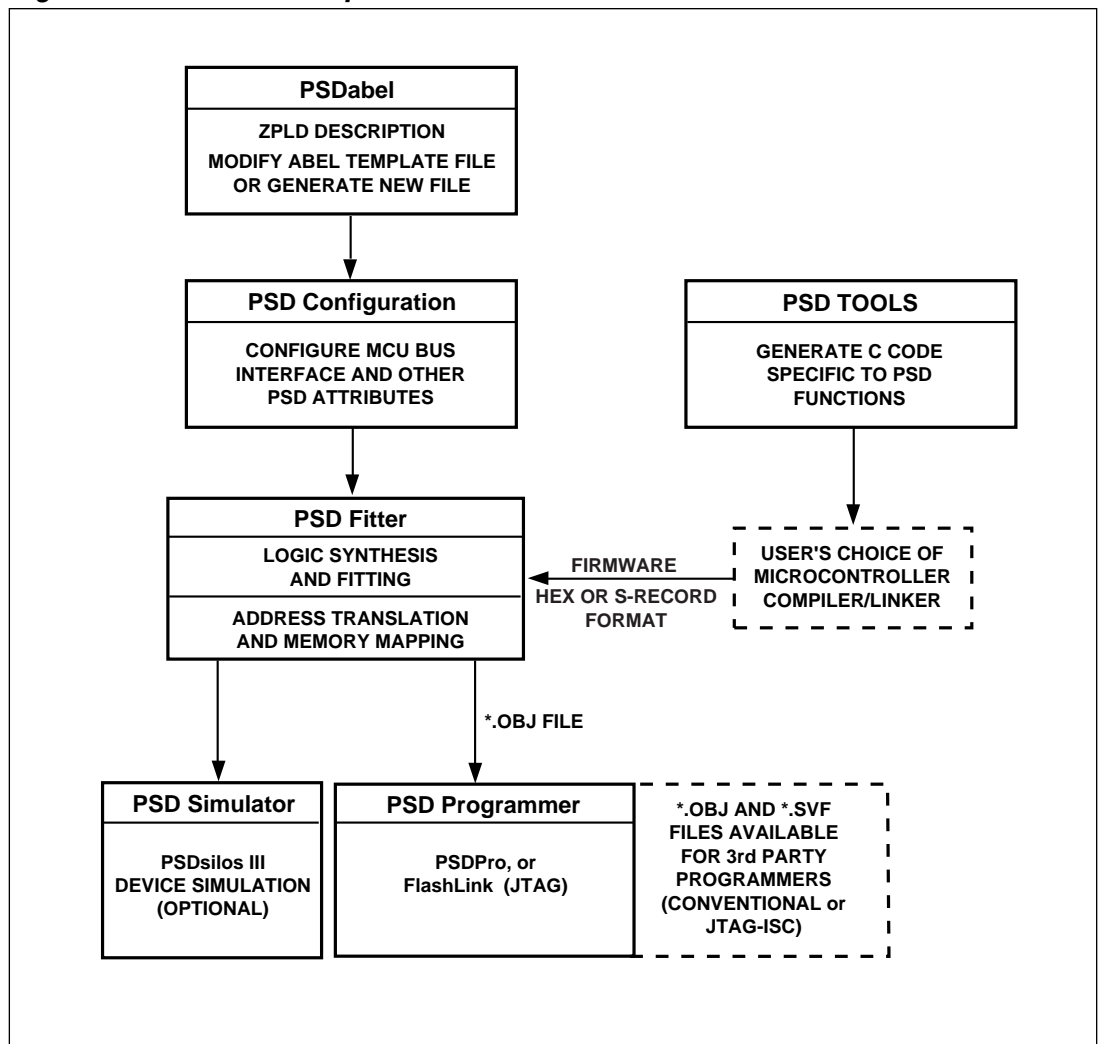
The PSD813F family is supported by the Windows-based PSDsoft Development System. The PSDsoft design flow is shown in Figure 2. The PLD design entry is done using PSDabel, which creates a minimized logic implementation, and provides logic simulation of the PLDs. The PSD813F MCU Bus Interface and I/O Port configuration are entered in PSD Configuration.

PSDsoft can generate ANSI C functions specific to the PSD. The user can merge these C functions with their own, and then compile and link it using any embedded C compiler on the market.

PSD Fitter is comprised of a fitter and address translator. It generates a programming data file (.obj) based on PSD configuration data, the PSDabel file, and the microcontroller firmware. The object file can be downloaded to a programmer or to PSD Simulator for device-level simulation.

PSDsoft offers direct support for three WSI device programmers, PSDpro, MagicPro III, and FlashLink (JTAG). PSDsoft makes available two types of files to support third party programmers. First, the *.obj file is in Intel hex format, and is compatible with conventional device programmers. Second, the *.svf file is a serial vector format file for JTAG-ISC device programmers.

Figure 2. PSDsoft Development Tools



7.0
Table 5.
PSD813F
Pin
Descriptions

The following table describes the pin names and pin functions of the PSD813F. Pins that have multiple names and/or functions are defined using PSD Configuration.

<i>Pin Name</i>	<i>Pin*</i>	<i>Type</i>	<i>Description</i>
ADIO0-7	30-37	I/O	This is the lower Address/Data port. Connect your MCU address or address/data bus according to the following rules: <ol style="list-style-type: none"> 1. If your MCU has a multiplexed address/data bus where the data is multiplexed with the lower address bits, connect AD[0:7] to this port. 2. If your MCU does not have a multiplexed address/data bus, or you are using an 80C251 in page mode, connect A[0:7] to this port. 3. If you are using an 80C51XA in burst mode, connect A4/D0 through A11/D7 to this port. ALE or AS latches the address. The PSD drives data out only if the read signal is active and one of the PSD functional blocks was selected. The addresses on this port are passed to the PLDs.
ADIO8-15	39-46	I/O	This is the upper Address/Data port. Connect your MCU address or address/data bus according to the following rules: <ol style="list-style-type: none"> 1. If your MCU has a multiplexed address/data bus where the data is multiplexed with the lower address bits, connect A[8:15] to this port. 2. If your MCU does not have a multiplexed address/data bus, connect A[8:15] to this port. 3. If you are using an 80C251 in page mode, connect AD[8:15] to this port. 4. If you are using an 80C51XA in burst mode, connect A12/D8 through A19/D15 to this port. ALE or AS latches the address. The PSD drives data out only if the read signal is active and one of the PSD functional blocks was selected. The addresses on this port are passed to the PLDs.
CNTL0	47	I	The following control signals can be connected to this port, based on your MCU: <ol style="list-style-type: none"> 1. \overline{WR} — active-low write input. 2. $R_{\overline{W}}$ — active-high read/active low write input. This port is connected to the PLDs. Therefore, these signals can be used in decode and other logic equations.
CNTL1	50	I	The following control signals can be connected to this port, based on your MCU: <ol style="list-style-type: none"> 1. \overline{RD} — active-low read input. 2. \overline{E} — E clock input. 3. \overline{DS} — active-low data strobe input. 4. \overline{PSEN} — connect PSEN to this port when it is being used as an active-low read signal. For example, when the 80C251 outputs more than 16 address bits, PSEN is actually the read signal. This port is connected to the PLDs. Therefore, these signals can be used in decode and other logic equations.

Table 5.
PSD813F
Pin
Descriptions
(cont.)

<i>Pin Name</i>	<i>Pin*</i>	<i>Type</i>	<i>Description</i>
CNTL2	49	I	This port can be used to input the $\overline{\text{PSEN}}$ (Program Select Enable) signal from any MCU that uses this signal for code exclusively. If your MCU does not output a Program Select Enable signal, this port can be used as a generic input. This port is connected to the PLDs.
$\overline{\text{Reset}}$	48	I	Active low reset input. Resets I/O Ports, PLD Micro \leftrightarrow Cells and some of the configuration registers. Must be active at power up.
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	29 28 27 25 24 23 22 21	I/O	<p>These pins make up Port A. These port pins are configurable and can have the following functions:</p> <ol style="list-style-type: none"> 1. MCU I/O — write to or read from a standard output or input port. 2. CPLD Micro\leftrightarrowCell (McellAB0-7) outputs. 3. Inputs to the PLDs. 4. Latched address outputs (see Table 6). 5. Address inputs. For example, PA0-3 could be used for A[0:3] when using an 80C51XA in burst mode. 6. As the data bus inputs D[0:7] for non-multiplexed address/data bus MCUs. 7. D0/A16-D3/A19 in M37702M2 mode. 8. Peripheral I/O mode. <p>Note: PA0-3 can only output CMOS signals with an option for high slew rate. However, PA4-7 can be configured as CMOS or Open Drain Outputs.</p>
PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7	7 6 5 4 3 2 52 51	I/O	<p>These pins make up Port B. These port pins are configurable and can have the following functions:</p> <ol style="list-style-type: none"> 1. MCU I/O — write to or read from a standard output or input port. 2. CPLD Micro\leftrightarrowCell (McellAB0-7 or McellBC0-7) outputs. 3. Inputs to the PLDs. 4. Latched address outputs (see Table 6). <p>Note: PB0-3 can only output CMOS signals with an option for high slew rate. However, PB4-7 can be configured as CMOS or Open Drain Outputs.</p>
PC0	20	I/O	<p>PC0 pin of Port C. This port pin can be configured to have the following functions:</p> <ol style="list-style-type: none"> 1. MCU I/O — write to or read from a standard output or input port. 2. CPLD Micro\leftrightarrowCell (McellBC0) output. 3. Input to the PLDs. 4. TMS Input** for the JTAG Interface. <p>This pin can be configured as a CMOS or Open Drain output.</p>
PC1	19	I/O	<p>PC1 pin of Port C. This port pin can be configured to have the following functions:</p> <ol style="list-style-type: none"> 1. MCU I/O — write to or read from a standard output or input port. 2. CPLD Micro\leftrightarrowCell (McellBC1) output. 3. Input to the PLDs. 4. TCK Input** for the JTAG Interface. <p>This pin can be configured as a CMOS or Open Drain output.</p>

Table 5.
PSD813F
Pin
Descriptions
(cont.)

<i>Pin Name</i>	<i>Pin*</i>	<i>Type</i>	<i>Description</i>
PC2	18	I/O	PC2 pin of Port C. This port pin can be configured to have the following functions: <ol style="list-style-type: none"> 1. MCU I/O — write to or read from a standard output or input port. 2. CPLD Micro↔Cell (McellBC2) output. 3. Input to the PLDs. 4. Vstby — SRAM standby voltage input for SRAM battery backup. This pin can be configured as a CMOS or Open Drain output.
PC3	17	I/O	PC3 pin of Port C. This port pin can be configured to have the following functions: <ol style="list-style-type: none"> 1. MCU I/O — write to or read from a standard output or input port. 2. CPLD Micro↔Cell (McellBC3) output. 3. Input to the PLDs. 4. \overline{TSTAT} output** for the JTAG interface. 5. Rdy/Bsy output for in-system parallel programming. This pin can be configured as a CMOS or Open Drain output.
PC4	14	I/O	PC4 pin of Port C. This port pin can be configured to have the following functions: <ol style="list-style-type: none"> 1. MCU I/O — write to or read from a standard output or input port. 2. CPLD Micro↔Cell (McellBC4) output. 3. Input to the PLDs. 4. \overline{TERR} output** for the JTAG interface. 5. Vbaton — battery backup indicator output. Goes high when power is being drawn from an external battery. This pin can be configured as a CMOS or Open Drain output.
PC5	13	I/O	PC5 pin of Port C. This port pin can be configured to have the following functions: <ol style="list-style-type: none"> 1. MCU I/O — write to or read from a standard output or input port. 2. CPLD Micro↔Cell (McellBC5) output. 3. Input to the PLDs. 4. TDI input** for the JTAG interface. This pin can be configured as a CMOS or Open Drain output.
PC6	12	I/O	PC6 pin of Port C. This port pin can be configured to have the following functions: <ol style="list-style-type: none"> 1. MCU I/O — write to or read from a standard output or input port. 2. CPLD Micro↔Cell (McellBC6) output. 3. Input to the PLDs. 4. TDO output** for the JTAG interface. This pin can be configured as a CMOS or Open Drain output.

Table 5.
PSD813F
Pin
Descriptions
(cont.)

<i>Pin Name</i>	<i>Pin*</i>	<i>Type</i>	<i>Description</i>
PC7	11	I/O	PC7 pin of Port C. This port pin can be configured to have the following functions: 1. MCU I/O — write to or read from a standard output or input port. 2. CPLD Micro \leftrightarrow Cell (McellBC7) output. 3. Input to the PLDs. 4. DBE — active-low Data Byte Enable input from 68HC912 type MCUs. This pin can be configured as a CMOS or Open Drain output.
PD0	10	I/O	PD0 pin of Port D. This port pin can be configured to have the following functions: 1. ALE/AS input latches address output from the MCU. 2. MCU I/O — write or read from a standard output or input port. 3. Input to the PLDs. 4. CPLD output (external chip select).
PD1	9	I/O	PD1 pin of Port D. This port pin can be configured to have the following functions: 1. MCU I/O — write to or read from a standard output or input port. 2. Input to the PLDs. 3. CPLD output (external chip select). 4. CLKIN — clock input to the CPLD Micro \leftrightarrow Cells, the automatic power-down unit's power-down counter, and the CPLD AND array.
PD2	8	I/O	PD2 pin of Port D. This port pin can be configured to have the following functions: 1. MCU I/O — write to or read from a standard output or input port. 2. Input to the PLDs. 3. CPLD output (external chip select). 4. CSI — chip select input. When low, the MCU can access the PSD memory and I/O. When high, the PSD memory blocks are disabled to conserve power.
V _{CC}	15, 38		Power pins
GND	1,16,26		Ground pins

*The pin numbers in this table are for the PLCC package only. See the package information section for pin numbers on other package types.

**These functions can be multiplexed with other functions.

Table 6. I/O Port Latched Address Output Assignments*

<i>Microcontroller</i>	<i>Port A</i>		<i>Port B</i>	
	<i>Port A (3:0)</i>	<i>Port A (7:4)</i>	<i>Port B (3:0)</i>	<i>Port B (7:4)</i>
8051XA (8-bit)	N/A	Address [7:4]	Address [11:8]	N/A
80C251 (page mode)	N/A	N/A	Address [11:8]	Address [15:12]
All other 8-bit multiplexed	Address [3:0]	Address [7:4]	Address [3:0]	Address [7:4]
8-bit non-multiplexed bus	N/A	N/A	Address [3:0]	Address [7:4]

N/A = Not Applicable

*Refer to the I/O Port Section on how to enable the Latched Address Output function.



8.0 PSD813F Register Description and Address Offset

Table 7 shows the offset addresses to the PSD813F registers relative to the CSIOP base address. The CSIOP space is the 256 bytes of address that is allocated by the user to the internal PSD813F registers. Table 7 provides brief descriptions of the registers in CSIOP space. For a more detailed description, refer to section 9.

Table 7. Register Address Offset

Register Name	Port A	Port B	Port C	Port D	Other *	Description
Data In	00	01	10	11		Reads Port pin as input, MCU I/O input mode
Control	02	03				Selects mode between MCU I/O or Address Out
Data Out	04	05	12	13		Stores data for output to Port pins, MCU I/O output mode
Direction	06	07	14	15		Configures Port pin as input or output
Drive Select	08	09	16	17		Configures Port pins as either CMOS or Open Drain on some pins, while selecting high slew rate on other pins.
Input Micro↔Cell	0A	0B	18			Reads Input Micro↔Cells
Enable Out	0C	0D	1A	1B		Reads the status of the output enable to the I/O Port driver
Output Micro↔Cells AB	20	20				Read – reads output of Micro↔Cells AB Write – loads Micro↔cell Flip-Flops
Output Micro↔Cells BC		21	21			Read – reads output of Micro↔Cells BC Write – loads Micro↔cell Flip-Flops
Mask Micro↔Cells AB	22	22				Blocks writing to the Output Micro↔Cells AB
Mask Micro↔Cells BC		23	23			Blocks writing to the Output Micro↔Cells BC
Flash Protection					C0	Read only – Flash Sector Protection
PSD/EE Protection					C2	Read only – PSD Security and EEPROM/Flash Boot Sector Protection
JTAG Enable					C7	Enables JTAG Port
PMMR0					B0	Power Management Register 0
PMMR2					B4	Power Management Register 2
Page					E0	Page Register
VM					E2	Places PSD memory areas in Program and/or Data space on an individual basis.

*Other registers that are not part of the I/O ports.

9.0 The PSD813F Functional Blocks

As shown in Figure 1, the PSD813F consists of six major types of functional blocks:

- Memory Blocks*
- PLD Blocks*
- Bus Interface*
- I/O Ports*
- Power Management Unit*
- JTAG Interface*

The functions of each block are described in the following sections. Many of the blocks perform multiple functions, and are user configurable.

9.1 Memory Blocks

The PSD813F has the following memory blocks:

- The main Flash memory
- Optional secondary EEPROM or Flash boot memory
- Optional SRAM.

The memory select signals for these blocks originate from the Decode PLD (DPLD) and are user-defined in PSDsoft.

Table 8 summarizes which versions of the PSD813F contain which memory blocks.

Table 8. Memory Blocks

<i>Device</i>	<i>Main Flash 128KB</i>	<i>EEPROM 32KB</i>	<i>Flash Boot Memory 32K</i>	<i>SRAM 2KB</i>
PSD813F1	Yes	Yes	No	Yes
PSD813F2	Yes	No	Yes	Yes
PSD813F3	Yes	No	No	Yes
PSD813F4	Yes	No	Yes	No
PSD813F5	Yes	No	No	No

9.1.1 Main Flash and Optional Secondary EEPROM or Flash Boot Memory Description

The 1 Mbit main Flash memory block is divided evenly into eight 16 Kbyte sectors. The optional EEPROM or Flash Boot memory is divided into four sectors of eight Kbytes each. Each sector of either memory can be separately protected from program and erase operations.

Flash memory may be erased on a sector-by-sector basis and programmed byte-by-byte. Flash sector erasure may be suspended while data is read from other sectors of memory and then resumed after reading.

EEPROM may be programmed byte-by-byte or sector-by-sector, and erasing is automatic and transparent. The integrity of the data can be secured with the help of Software Data Protection (SDP). Any write operation to the EEPROM is inhibited during the first five milliseconds following power-up.

During a program or erase of Flash, or during a write of the EEPROM, the status can be output on the Rdy/Bsy pin of Port C3. This pin is set up using PSDsoft Configuration.

The PSD813F Functional Blocks (cont.)

9.1.1.1 Memory Block Selects

The decode PLD in the PSD813F generates the chip selects for all the internal memory blocks (refer to the PLD section). Each of the eight Flash memory sectors have a Flash Select signal (FS0-FS7) which can contain up to three product terms. Each of the optional four EEPROM or Flash Boot memory sectors have a Select signal (EES0-3 or CSBOOT0-3) which can contain up to three product terms. Having three product terms for each sector select signal allows a given sector to be mapped in different areas of system memory. When using a microcontroller with separate Program and Data space, these flexible select signals allow dynamic re-mapping of sectors from one space to the other.

9.1.1.2 The Ready/Busy Pin (PC3)

Pin PC3 can be used to output the Ready/Busy status of the PSD813F. The output on the pin will be a '0' (Busy) when Flash or EEPROM memory blocks are being written to, **or** when the Flash memory block is being erased. The output will be a '1' (Ready) when no write or erase operation is in progress.

9.1.1.3 Memory Operation

The main Flash and optional EEPROM or Flash Boot memories are addressed through the microcontroller interface on the PSD813F device. The microcontroller can access these memories in one of two ways:

- The microcontroller can execute a typical bus write or read **operation** just as it would if accessing a RAM or ROM device using standard bus cycles.
- The microcontroller can execute a specific **instruction** that consists of several write and read operations. This involves writing specific data patterns to special addresses within the Flash or EEPROM to invoke an embedded algorithm. These instructions are summarized in Table 9.

Typically, Flash memory can be read by the microcontroller using read operations, just as it would read a ROM device. However, Flash memory can only be erased and programmed with specific instructions. For example, the microcontroller cannot write a single byte directly to Flash memory as one would write a byte to RAM. To program a byte into Flash memory, the microcontroller must execute a program instruction sequence, then test the status of the programming event. This status test is achieved by a read operation or polling the Rdy/Busy pin (PC3).

The Flash memory can also be read by using special instructions to retrieve particular Flash device information (sector protect status and ID).

The EEPROM is a bit different. Data can be written to EEPROM memory using write operations, like writing to a RAM device, but the status of each write event must be checked by the microcontroller. A write event can be one to 64 contiguous bytes. The status test is very similar to that used for Flash memory (read operation or Rdy/Busy). Optionally, the EEPROM memory may be put into a Software Data Protect (SDP) mode where it requires instructions, rather than operations, to alter its contents. SDP mode makes writing to EEPROM much like writing to Flash memory.

**The
PSD813F
Functional
Blocks**
(cont.)

9.1.1.3.1 Instructions

An instruction is defined as a sequence of specific operations. Each received byte is sequentially decoded by the PSD and not executed as a standard write operation. The instruction is executed when the correct number of bytes are properly received and the time between two consecutive bytes is shorter than the time-out value. Some instructions are structured to include read operations after the initial write operations.

The sequencing of any instruction must be followed exactly. Any invalid combination of instruction bytes or time-out between two consecutive bytes while addressing Flash memory will reset the device logic into a read array mode (Flash memory reads like a ROM device). An invalid combination or time-out while addressing the EEPROM block will cause the offending byte to be interpreted as a single operation.

The PSD813F supports these instructions (see Table 9):

Flash memory:

- Erase memory by chip or sector
- Suspend or resume sector erase
- Program a byte
- Reset to read array mode
- Read Flash Identifier value
- Read sector protection status

Optional EEPROM:

- Write data to OTP Row
- Read data from OTP Row
- Power down memory
- Enable Software Data Protect (SDP)
- Disable SDP
- Return from read OTP Row read mode or power down mode.

These instructions are detailed in Table 9. For efficient decoding of the instructions, the first two bytes of an instruction are the coded cycles and are followed by a command byte or confirmation byte. The coded cycles consist of writing the data AAh to address X555h during the first cycle and data 55h to address XAAAh during the second cycle. Address lines A15-A12 are don't cares during the instruction write cycles. However, the appropriate sector select signal (FSi, EESi, or CSBOOTi) must be selected.

**The
PSD813F
Functional
Blocks
(cont.)**

Table 9. Instructions

<i>Instruction</i>	<i>EEPROM Sector Select (EESi)</i>	<i>Flash Sector Select (FSi, CSBOOTi)</i> (Note 2)	<i>Cycle 1</i>	<i>Cycle 2</i>	<i>Cycle 3</i>	<i>Cycle 4</i>	<i>Cycle 5</i>	<i>Cycle 6</i>	<i>Cycle 7</i>
Read Flash Identifier (Note 3, 5)	0	1	AAh @X555h	55h @XAAAh	90h @X555h	Read identifier with (A6,A1,A0 at 0,0,1)			
Read OTP Row (Note 4)	1	0	AAh @X555h	55h @XAAAh	90h @X555h	Read byte 1	Read byte 2		Read byte N
Read Sector Protection Status (Notes 3, 5)	0	1	AAh @X555h	55h @XAAAh	90h @X555h	Read identifier with (A6,A1,A0 at 0,1,0)			
Program a Flash Byte (Note 5)	0	1	AAh @X555h	55h @XAAAh	A0h @X555h	Data @ address			
Erase one Flash Sector (Note 5)	0	1	AAh @X555h	55h @XAAAh	80h @X555h	AAh @X555h	55h @XAAAh	30h @ Sector address	30h @ Sector address(1)
Erase the whole Flash (Note 5)	0	1	AAh @X555h	55h @XAAAh	80h @X555h	AAh @X555h	55h @XAAAh	10h @X555h	
Suspend Sector Erase (Note 5)	0	1	B0h @ any address						
Resume Sector Erase (Note 5)	0	1	30h @ any address						
EEPROM Power Down (Note 4)	1	0	AAh @X555h	55h @XAAAh	30h @X555h				
SDP Enable/EEPROM Write (Note 4)	1	0	AAh @X555h	55h @XAAAh	A0h @X555h	Write byte 1	Write byte 2		Write byte N
SDP Disable (Note 4)	1	0	AAh @X555h	55h @XAAAh	80h @X555h	AAh @X555h	55h @XAAAh	20h @X555h	
Write in OTP Row (Notes 4, 6)	1	0	AAh @X555h	55h @XAAAh	B0h @X555h	Write byte 1	Write byte 2		Write byte N
Return (from OTP Read or EEPROM Power-Down) (Note 4)	1	0	F0h @ any address						
Reset (Notes 3, 5)	0	1	AAh @X555h	55h @XAAAh	F0h @ any address				
Reset (short instruction) (Note 5)	0	1	F0h @ any address						

- NOTES:**
1. Additional sectors to be erased must be entered within 80 μ s. A Sector Address is any address within the Sector.
 2. Flash and EEPROM Sector Selects are active high. Addresses A15-A12 are don't cares in Instruction Bus Cycles.
 3. The Reset instruction is required to return to the normal read array mode if DQ5 goes high or after reading the Flash Identifier or Protection status.
 4. The MCU cannot invoke these instructions while executing code from EEPROM. The MCU must be operating from some other memory when these instructions are performed.
 5. The MCU cannot invoke these instructions while executing code from the same Flash memory for which the instruction is intended. The MCU must operate from some other memory when these instructions are executed.
 6. Writing to OTP Row is allowed only when SDP mode is disabled.



**The
PSD813F
Functional
Blocks**
(cont.)

9.1.1.4 Power Down Instruction and Power Up Condition

9.1.1.4.1 EEPROM Power Down Instruction (PSD813F1 only)

The EEPROM can enter power down mode with the help of the EEPROM power down instruction (see Table 9). Once the EEPROM power down instruction is decoded, the EEPROM memory cannot be accessed unless a Return instruction (also in Table 9) is decoded. Alternately, this power down mode will automatically occur when the APD circuit is triggered (see section 9.5.1). Therefore, this instruction is not required if the APD circuit is used.

9.1.1.4.2 Power-Up Condition

The PSD813F internal logic is reset upon power-up to the read array mode. Any write operation to the EEPROM is inhibited during the first 5 msec following power-up. The FSi and EESi/CSBOOTi select signals, along with the write strobe signal, must be in the false state during power-up for maximum security of the data contents and to remove the possibility of a byte being written on the first edge of a write strobe signal. Any write cycle initiation is locked when V_{CC} is below VLKO.

9.1.1.5 Read

Under typical conditions, the microcontroller may read the Flash, EEPROM, or Flash Boot memories using read operations just as it would a ROM or RAM device. Alternately, the microcontroller may use read operations to obtain status information about a program or erase operation in progress. Lastly, the microcontroller may use instructions to read special data from these memories. The following sections describe these read functions.

9.1.1.5.1 Read the Contents of Memory

Main Flash and Flash Boot memories are placed in the read array mode after power-up, chip reset, or a Reset Flash instruction (see Table 9). The microcontroller can read the memory contents of main Flash, optional EEPROM, or optional Flash Boot by using read operations any time the read operation is not part of an instruction sequence.

9.1.1.5.2 Read the Main Flash Memory Identifier

The main Flash memory identifier is read with an instruction composed of 4 operations: 3 specific write operations and a read operation (see Table 9). During the read operation, address bits A6, A1, and A0 must be 0,0,1, respectively, and the appropriate sector select signal (FSi) must be active. See section 9.1.1.9.3 for information on how to use the Flash Memory Identifier.

9.1.1.5.3 Read the Main Flash Memory Sector Protection Status

The main Flash memory sector protection status is read with an instruction composed of 4 operations: 3 specific write operations and a read operation (see Table 9). During the read operation, address bits A6, A1, and A0 must be 0,1,0, respectively, while the chip select FSi designates the Flash sector whose protection has to be verified. The read operation will produce 01h if the Flash sector is protected, or 00h if the sector is not protected.

The sector protection status for all NVM blocks (main Flash, EEPROM, or Boot Flash) can be read by the microcontroller accessing the Flash Protection and PSD/EE Protection registers in PSD I/O space. See section 9.1.1.9.1 for register definitions.

**The
PSD813F
Functional
Blocks**
(cont.)

9.1.1.5.4 Read the OTP Row (PSD813F1 only)

There are 64 bytes of One-Time-Programmable (OTP) memory that reside in EEPROM. These 64 bytes are in addition to the 32 Kbytes of EEPROM memory. A read of the OTP row is done with an instruction composed of at least 4 operations: 3 specific write operations and one to 64 read operations (see Table 9). During the read operation(s), address bit A6 must be zero, while address bits A5-A0 define the OTP Row byte to be read while any EEPROM sector select signal (EESi) is active. After reading the last byte, an EEPROM Return instruction must be executed (see Table 9).

9.1.1.5.5 Read the Erase/Program Status Bits

The PSD813F provides several status bits to be used by the microcontroller to confirm the completion of an erase or programming instruction of Flash memory. Bits are also available to show the status of writes to EEPROM. These status bits minimize the time that the microcontroller spends performing these tasks and are defined in Table 10. The status bits can be read as many times as needed.

Table 10. Status Bit

	<i>FSi/ CSBOOTi</i>	<i>EESi</i>	<i>DQ7</i>	<i>DQ6</i>	<i>DQ5</i>	<i>DQ4</i>	<i>DQ3</i>	<i>DQ2</i>	<i>DQ1</i>	<i>DQ0</i>
Flash	V _{IH}	V _{IL}	Data Polling	Toggle Flag	Error Flag	X	Erase Time- out	X	X	X
EEPROM	V _{IL}	V _{IH}	Data Polling	Toggle Flag	X	X	X	X	X	X

NOTES: 1. X = Not guaranteed value, can be read either 1 or 0.
2. DQ7-DQ0 represent the Data Bus bits, D7-D0.
3. FSi/CSBOOTi and EESi are active high.

For Flash memory, the microcontroller can perform a read operation to obtain these status bits while an erase or program instruction is being executed by the embedded algorithm. See section 9.1.1.7 for details.

For EEPROM not in SDP mode, the microcontroller can perform a read operation to obtain these status bits just after a data write operation. The microcontroller may write one to 64 bytes before reading the status bits. See section 9.1.1.6 for details.

For EEPROM in SDP mode, the microcontroller will perform a read operation to obtain these status bits while an SDP write instruction is being executed by the embedded algorithm. See section 9.1.1.3 for details.

**The
PSD813F
Functional
Blocks**
(cont.)

9.1.1.5.6 Data Polling Flag DQ7

When Erasing or Programming the Flash memory (or when Writing into the EEPROM memory), bit DQ7 outputs the complement of the bit being entered for Programming/Writing on DQ7. Once the Program instruction or the Write operation is completed, the true logic value is read on DQ7 (in a Read operation). Flash memory specific features:

- Data Polling is effective after the fourth Write pulse (for programming) or after the sixth Write pulse (for Erase). It must be performed at the address being programmed or at an address within the Flash sector being erased.
- During an Erase instruction, DQ7 outputs a '0'. After completion of the instruction, DQ7 will output the last bit programmed (it is a '1' after erasing).
- If the byte to be programmed is in a protected Flash sector, the instruction is ignored.
- If all the Flash sectors to be erased are protected, DQ7 will be set to '0' for about 100 μ s, and then return to the previous addressed byte. No erasure will be performed.

9.1.1.5.7 Toggle Flag DQ6

The PSD813F offers another way for determining when the EEPROM write or the Flash memory Program instruction is completed. During the internal Write operation and when either the FSi or EESi/CSBOOTi is true, the DQ6 will toggle from '0' to '1' and '1' to '0' on subsequent attempts to read any byte of the memory.

When the internal cycle is complete, the toggling will stop and the data read on the Data Bus D0-7 is the addressed memory byte. The device is now accessible for a new Read or Write operation. The operation is finished when two successive reads yield the same output data. Flash memory specific features:

- The Toggle bit is effective after the fourth Write pulse (for programming) or after the sixth Write pulse (for Erase).
- If the byte to be programmed belongs to a protected Flash sector, the instruction is ignored.
- If all the Flash sectors selected for erasure are protected, DQ6 will toggle to '0' for about 100 μ s and then return to the previous addressed byte.

9.1.1.5.8 Error Flag DQ5

During a correct Program or Erase, the Error bit will set to '0'. This bit is set to '1' when there is a failure during Flash byte programming, Sector erase, or Bulk Erase.

In the case of Flash programming, the Error Bit indicates the attempt to program a Flash bit(s) from the programmed state (0) to the erased state (1), which is not a valid operation. The Error bit may also indicate a timeout condition while attempting to program a byte.

In case of an error in Flash sector erase or byte program, the Flash sector in which the error occurred or to which the programmed byte belongs must no longer be used. Other Flash sectors may still be used. The Error bit resets after the Reset instruction.

9.1.1.5.9 Erase Time-out Flag DQ3 (Flash Memory only)

The Erase Timer bit reflects the time-out period allowed between two consecutive Sector Erase instructions. The Erase timer bit is set to '0' after a Sector Erase instruction for a time period of 100 μ s + 20% unless an additional Sector Erase instruction is decoded. After this time period or when the additional Sector Erase instruction is decoded, DQ3 is set to '1'.

**The
PSD813F
Functional
Blocks**
(cont.)

9.1.1.6 Writing to the Optional EEPROM

Data may be written a byte at a time to the EEPROM using simple write operations, much like writing to an SRAM. Unlike SRAM though, the completion of each byte write must be checked before the next byte is written. To speed up this process, the PSD813F offers a Page write feature to allow writing of several bytes before checking status.

To prevent inadvertent writes to EEPROM, the PSD813F offers a Software Data Protect (SDP) mode. Once enabled, SDP forces the MCU to “unlock” the EEPROM before altering its contents, much like Flash memory programming.

9.1.1.6.1 Write a Byte to EEPROM

A write operation is initiated when an EEPROM select signal (EESi) is true and the write strobe signal (wr) into the PSD813F is true. If the PSD813F detects no additional writes within 120 μ sec, an internal storage operation is initiated. Internal storage to EEPROM memory technology typically takes a few milliseconds to complete.

The status of the write operation is obtained by the MCU reading the Data Polling or Toggle bits (as detailed in section 9.1.1.5), or the Ready/Busy output pin (section 9.1.1.2).

Keep in mind that the MCU does not need to erase a location in EEPROM before writing it. Erasure is performed automatically as an internal process.

9.1.1.6.2 Write a Page to EEPROM

Writing data to EEPROM using page mode is more efficient than writing one byte at a time. The PSD813F EEPROM has a 64 byte volatile buffer that the MCU may fill before an internal EEPROM storage operation is initiated. Page mode timing approaches a 64:1 advantage over the time it takes to write individual bytes.

To invoke page mode, the MCU must write to EEPROM locations within a single page, with no more than 120 μ sec between individual byte writes. A single page means that address lines A14 to A6 must remain constant. The MCU may write to the 64 locations on a page in any order, which is determined by address lines A5 to A0. As soon as 120 μ sec have expired after the last page write, the internal EEPROM storage process begins and the MCU checks programming status. Status is checked the same way it is for byte writes, described above.

Note: be aware that if the upper address bits (A14 to A6) change during page write operations, loss of data may occur. Ensure that all bytes for a given page have been successfully stored in the EEPROM before proceeding to the next page. Correct management of MCU interrupts during EEPROM page write operations is essential.

9.1.1.6.3 EEPROM Software Data Protect (SDP)

The SDP feature is useful for protecting the contents of EEPROM from inadvertent write cycles that may occur during uncontrolled MCU bus conditions. These may happen if the application software gets lost or when V_{CC} is not within normal operating range.

Instructions from the MCU are used to enable and disable SDP mode (see Table 9). Once enabled, the MCU must write an instruction sequence to EEPROM before writing data (much like writing to Flash memory). SDP mode can be used for both byte and page writes to EEPROM. The device will remain in SDP mode until the MCU issues a valid SDP disable instruction.

PSD813F devices are shipped with SDP mode disabled. However, within PSDsoft, SDP mode may be enabled as part of programming the device with a device programmer (PSDpro).

**The
PSD813F
Functional
Blocks
(cont.)**

9.1.1.6.3 EEPROM Software Data Protect (SDP) (cont.)

To enable SDP mode at run time, the MCU must write three specific data bytes at three specific memory locations, as shown in Figure 3. Any further writes to EEPROM when SDP is set will require this same sequence, followed by the byte(s) to write. The first SDP enable sequence can be followed directly by the byte(s) to be written.

To disable SDP mode, the MCU must write specific bytes to six specific locations, as shown in Figure 4.

The MCU must not be executing code from EEPROM when these instructions are invoked. The MCU must be operating from some other memory when enabling or disabling SDP mode.

The state of SDP mode is not changed by power on/off sequences (nonvolatile). When either the SDP enable or SDP disable instructions are issued from the MCU, the MCU must use the Toggle bit (status bit DQ6) or the Ready/Busy output pin to check programming status. The Ready/Busy output is driven low from the first write of AAh @ 555h until the completion of the internal storage sequence. Data Polling (status bit DQ7) is not supported when issuing the SDP enable or SDP disable commands.

Note: Using the SDP sequence (enabling, disabling, or writing data) is initiated when specific bytes are written to addresses on specific “pages” of EEPROM memory, with no more than 120 μsec between writes. The addresses 555h and AAAh are located on different pages of EEPROM. This is how the PSD813F distinguishes these instruction sequences from ordinary writes to EEPROM, which are expected to be within a single EEPROM page.

Figure 3. EEPROM SDP Enable Flowcharts

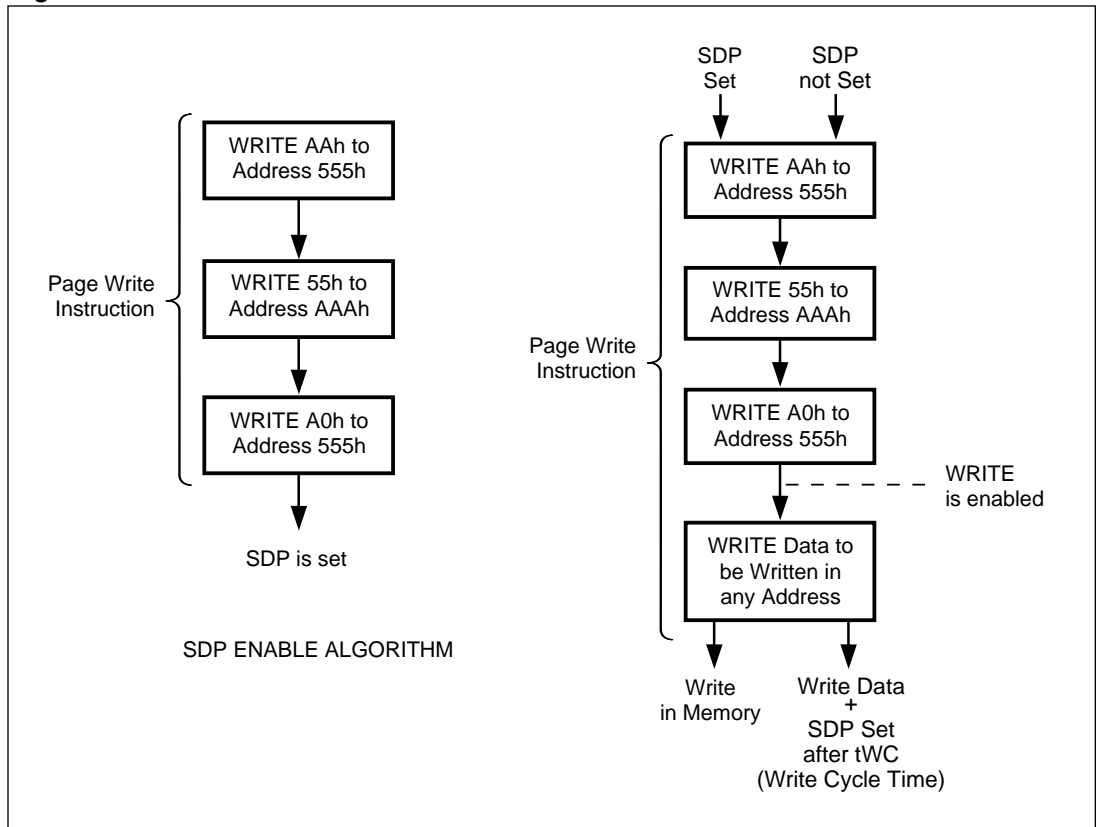
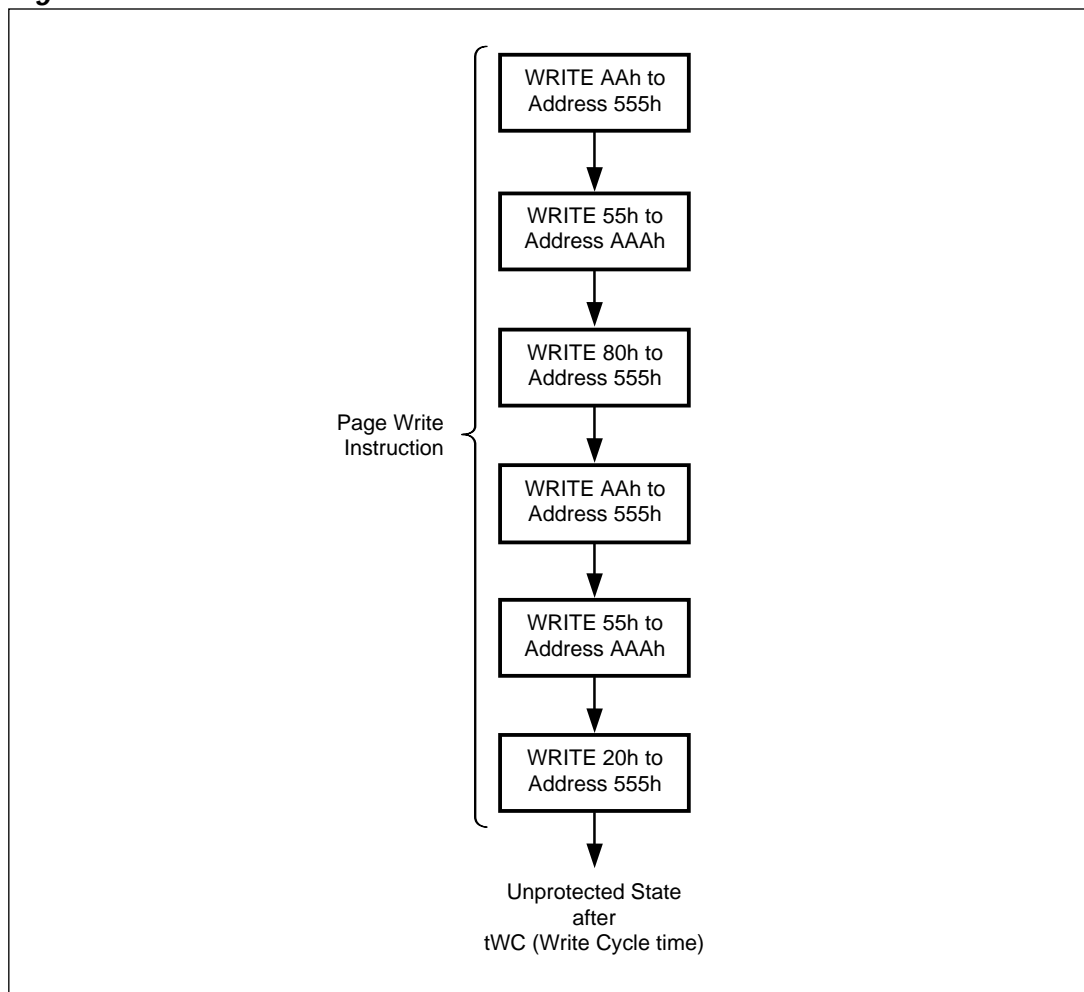


Figure 4. Software Data Protection Disable Flow Chart



9.1.1.6.4 Write OTP Row

Writing to the OTP row (64 bytes) can only be done once per byte, and is enabled by an instruction. This instruction is composed of three specific Write operations of data bytes at three specific memory locations followed by the data to be stored in the OTP row (refer to Table 9). During the write operations, address bit A6 must be zero, while address bits A5-A0 define the OTP Row byte to be written while any EEPROM Sector Select signal (EESi) is active. Writing the OTP Row is allowed only when SDP mode is not enabled.

9.1.1.7 Programming Flash Memory

Flash memory must be erased prior to being programmed. The MCU may erase Flash memory all at once or by-sector, but not byte-by-byte. A byte of Flash memory erases to all logic ones (FF hex), and its bits are programmed to logic zeros. Although erasing Flash memory occurs on a sector basis, programming Flash memory occurs on a byte basis.

The PSD813F main Flash and optional boot Flash require the MCU to send an instruction to program a byte or perform an erase function (see Table 9). This differs from EEPROM, which can be programmed with simple MCU bus write operations (unless EEPROM SDP mode is enabled).

Once the MCU issues a Flash memory program or erase instruction, it must check for the status of completion. The embedded algorithms that are invoked inside the PSD813F support several means to provide status to the MCU. Status may be checked using any of three methods: Data Polling, Data Toggle, or the Ready/Busy output pin.

**The
PSD813F
Functional
Blocks**
(cont.)

9.1.1.7.1 Data Polling

Polling on DQ7 is a method of checking whether a Program or Erase instruction is in progress or has completed. Figure 5 shows the Data Polling algorithm.

When the MCU issues a programming instruction, the embedded algorithm within the PSD813F begins. The MCU then reads the location of the byte to be programmed in Flash to check status. Data bit DQ7 of this location becomes the compliment of data bit 7 of the original data byte to be programmed. The MCU continues to poll this location, comparing DQ7 and monitoring the Error bit on DQ5. When the DQ7 matches data bit 7 of the original data, and the Error bit at DQ5 remains '0', then the embedded algorithm is complete. If the Error bit at DQ5 is '1', the MCU should test DQ7 again since DQ7 may have changed simultaneously with DQ5 (see Figure 5).

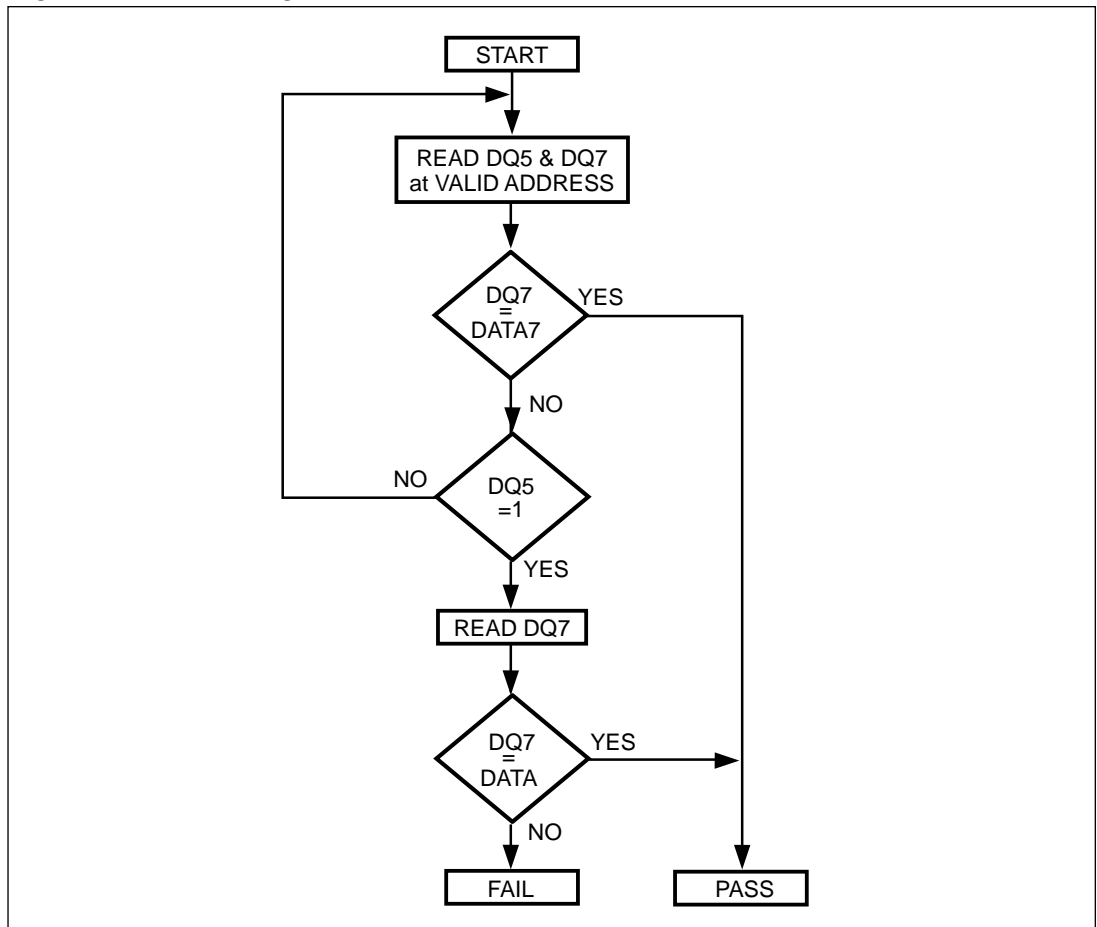
The Error bit at DQ5 will be set if either an internal timeout occurred while the embedded algorithm attempted to program the byte or if the MCU attempted to program a '1' to a bit that was not erased (not erased is logic '0').

It is suggested (as with all Flash memories) to read the location again after the embedded programming algorithm has completed to compare the byte that was written to Flash with the byte that was intended to be written.

When using the Data Polling method after an erase instruction, Figure 5 still applies. However, DQ7 will be '0' until the erase operation is complete. A '1' on DQ5 will indicate a timeout failure of the erase operation, a '0' indicates no error. The MCU can read any location within the sector being erased to get DQ7 and DQ5.

PSDsoft will generate ANSI C code functions which implement these Data Polling algorithms.

Figure 5. Data Polling Flow Chart



**The
PSD813F
Functional
Blocks**
(cont.)

9.1.1.7.2 Data Toggle

Checking the Data Toggle bit on DQ6 is a method of determining whether a Program or Erase instruction is in progress or has completed. Figure 6 shows the Data Toggle algorithm.

When the MCU issues a programming instruction, the embedded algorithm within the PSD813F begins. The MCU then reads the location of the byte to be programmed in Flash to check status. Data bit DQ6 of this location will toggle each time the MCU reads this location until the embedded algorithm is complete. The MCU continues to read this location, checking DQ6 and monitoring the Error bit on DQ5. When DQ6 stops toggling (two consecutive reads yield the same value), and the Error bit on DQ5 remains '0', then the embedded algorithm is complete. If the Error bit on DQ5 is '1', the MCU should test DQ6 again, since DQ6 may have changed simultaneously with DQ5 (see Figure 6).

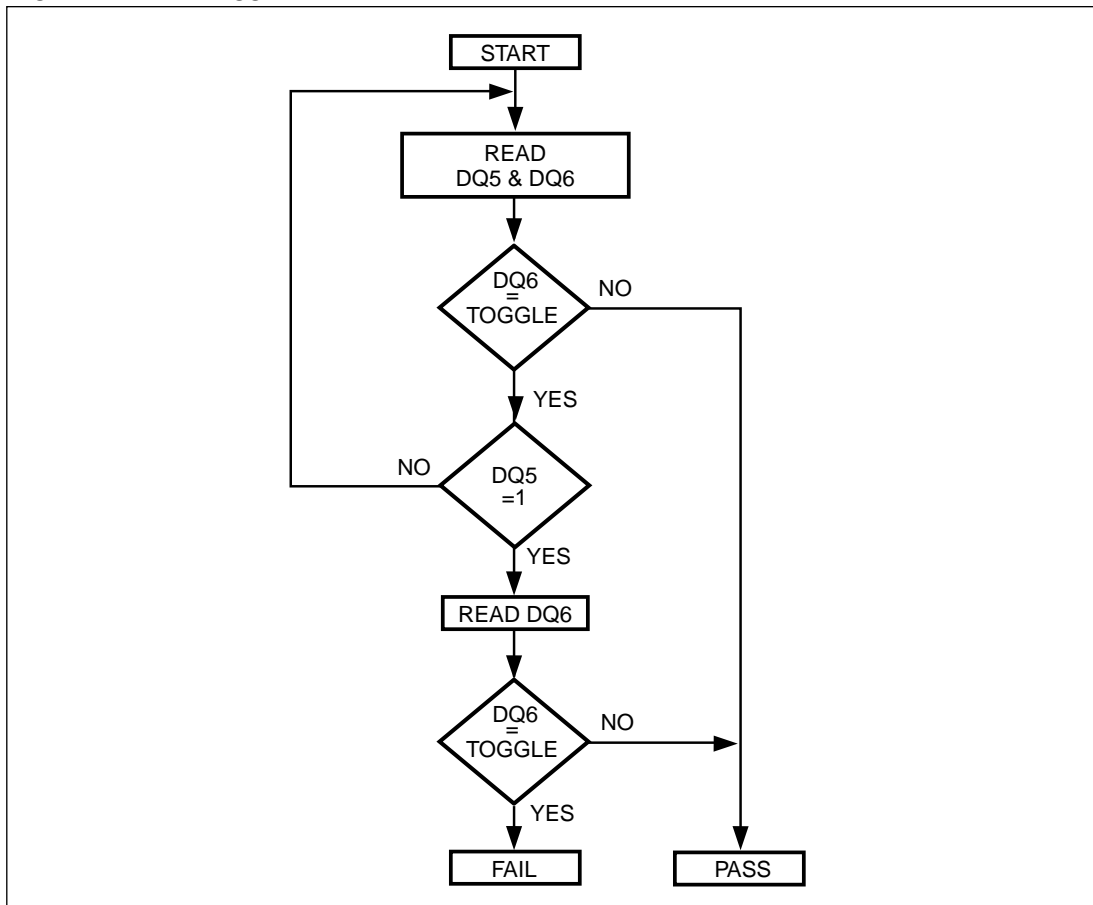
The Error bit at DQ5 will be set if either an internal timeout occurred while the embedded algorithm attempted to program the byte, or if the MCU attempted to program a '1' to a bit that was not erased (not erased is logic '0').

It is suggested (as with all Flash memories) to read the location again after the embedded programming algorithm has completed to compare the byte that was written to Flash with the byte that was intended to be written.

When using the Data Toggle method after an erase instruction, Figure 6 still applies. DQ6 will toggle until the erase operation is complete. A '1' on DQ5 will indicate a timeout failure of the erase operation, a '0' indicates no error. The MCU can read any location within the sector being erased to get DQ6 and DQ5.

PSDsoft will generate ANSI C code functions which implement these Data Toggling algorithms.

Figure 6. Data Toggle Flow Chart



**The
PSD813F
Functional
Blocks**
(cont.)

9.1.1.8 Erasing Flash Memory

9.1.1.8.1. Flash Bulk Erase Instruction

The Flash Bulk Erase instruction uses six write operations followed by a Read operation of the status register, as described in Table 9. If any byte of the Bulk Erase instruction is wrong, the Bulk Erase instruction aborts and the device is reset to the Read Flash memory status.

During a Bulk Erase, the memory status may be checked by reading status bits DQ5, DQ6, and DQ7, as detailed in section 9.1.1.7. The Error bit (DQ5) returns a '1' if there has been an Erase Failure (maximum number of erase cycles have been executed).

It is not necessary to program the array with 00h because the PSD813F will automatically do this before erasing to 0FFh.

During execution of the Bulk Erase instruction, the Flash memory will not accept any instructions.

9.1.1.8.2 Flash Sector Erase Instruction

The Sector Erase instruction uses six write operations, as described in Table 9. Additional Flash Sector Erase confirm commands and Flash sector addresses can be written subsequently to erase other Flash sectors in parallel, without further coded cycles, if the additional instruction is transmitted in a shorter time than the timeout period of about 100 μ s. The input of a new Sector Erase instruction will restart the time-out period.

The status of the internal timer can be monitored through the level of DQ3 (Erase time-out bit). If DQ3 is '0', the Sector Erase instruction has been received and the timeout is counting. If DQ3 is '1', the timeout has expired and the PSD813F is busy erasing the Flash sector(s). Before and during Erase timeout, any instruction other than Erase suspend and Erase Resume will abort the instruction and reset the device to Read Array mode. It is not necessary to program the Flash sector with 00h as the PSD813F1 will do this automatically before erasing (byte=FFh).

During a Sector Erase, the memory status may be checked by reading status bits DQ5, DQ6, and DQ7, as detailed in section 9.1.1.7.

During execution of the erase instruction, the Flash block logic accepts only Reset and Erase Suspend instructions. Erasure of one Flash sector may be suspended, in order to read data from another Flash sector, and then resumed.

**The
PSD813F
Functional
Blocks**
(cont.)

9.1.1.8.3 Flash Erase Suspend Instruction

When a Flash Sector Erase operation is in progress, the Erase Suspend instruction will suspend the operation by writing 0B0h to any address when an appropriate Chip Select (FSi or CSBOOTi) is true. (See Table 9). This allows reading of data from another Flash sector after the Erase operation has been suspended. Erase suspend is accepted only during the Flash Sector Erase instruction execution and defaults to read array mode. An Erase Suspend instruction executed during an Erase timeout will, in addition to suspending the erase, terminate the time out.

The Toggle Bit DQ6 stops toggling when the PSD813F internal logic is suspended. The toggle Bit status must be monitored at an address within the Flash sector being erased. The Toggle Bit will stop toggling between 0.1 μ s and 15 μ s after the Erase Suspend instruction has been executed. The PSD813F will then automatically be set to Read Flash Block Memory Array mode.

If an Erase Suspend instruction was executed, the following rules apply:

- Attempting to read from a Flash sector that was being erased will output invalid data.
- Reading from a Flash sector that was **not** being erased is valid.
- The Flash memory **cannot** be programmed, and will only respond to Erase Resume and Reset instructions (read is an operation and is OK).
- If a Reset instruction is received, data in the Flash sector that was being erased will be invalid.

9.1.1.8.4 Flash Erase Resume Instruction

If an Erase Suspend instruction was previously executed, the erase operation may be resumed by this instruction. The Erase Resume instruction consists of writing 030h to any address while an appropriate Chip Select (FSi or CSBOOTi) is true. (See Table 9.)

9.1.1.9 Flash and EEPROM Memory Specific Features

9.1.1.9.1 Flash and EEPROM Sector Protect

Each Flash and EEPROM sector can be separately protected against Program and Erase functions. Sector Protection provides additional data security because it disables all program or erase operations. This mode can be activated through the JTAG Port or a Device Programmer.

Sector protection can be selected for each sector using the PSDsoft Configuration program. This will automatically protect selected sectors when the device is programmed through the JTAG Port or a Device Programmer. Flash and EEPROM sectors can be unprotected to allow updating of their contents using the JTAG Port or a Device Programmer. The microcontroller can read (but cannot change) the sector protection bits.

Any attempt to program or erase a protected Flash or EEPROM sector will be ignored by the device. The Verify operation will result in a read of the protected data. This allows a guarantee of the retention of the Protection status.

The sector protection status can be read by the MCU through the Flash protection and PSD/EE protection registers (CSIOP). See Table 11.

**The
PSD813F
Functional
Blocks
(cont.)**

Table 11. Sector Protection/Security Bit Definition

Flash Protection Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sec7_Prot	Sec6_Prot	Sec5_Prot	Sec4_Prot	Sec3_Prot	Sec2_Prot	Sec1_Prot	Sec0_Prot

Bit Definitions:

Sec<i>_Prot 1 = Flash or Flash Boot Sector <i> is write protected.

Sec<i>_Prot 0 = Flash or Flash Boot Sector <i> is not write protected.

PSD/EE Protection Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Security_Bit	*	*	*	Sec3_Prot	Sec2_Prot	Sec1_Prot	Sec0_Prot

*: Not used.

Bit Definitions:

Sec<i>_Prot 1 = EEPROM or Flash Boot Sector <i> is write protected.

Sec<i>_Prot 0 = EEPROM or Flash Boot Sector <i> is not write protected.

Security_Bit 0 = Security Bit in device has not been set.

1 = Security Bit in device has been set.

9.1.1.9.2 Reset Instruction

The Reset instruction resets the internal memory logic state machine in a few milliseconds. Reset is an instruction of either one write operation or three write operations (refer to Table 9).

9.1.1.9.3 Programming and Erasing the Boot Blocks in PSD813F2 and PSD813F4

There are two different algorithms for programming and erasing the Boot Blocks in the PSD813F2 and F4 (Boot Blocks are selected by CSBOOTi). The selection of the correct algorithm is based on the internal die of the PSD device, which can be identified based on the Flash Memory Identifier read by the MCU. Using the Read Flash Identifier instruction (Table 9), the MCU will read one of two IDs for the PSD813F2 and PSD813F4, as shown in Table 12.

Table 12. Flash Memory ID Values for PSD813F2 and F4

Device	Flash ID	Boot Block Algorithm
PSD813F2 and F4	E3h	EEPROM Algorithm (See Section 9.1.1.6)
PSD813F2 and F4	E4h	Flash Algorithm (See Section 9.1.1.7)

For users of the PSD813F2 and F4, the MCU system software must make both algorithms available. Within the routine that programs or erases the Boot Block area, the MCU should use the Flash Memory Identifier first to select the appropriate algorithm. If the Identifier is E4h, then it should treat the Boot Block area as Flash memory. If the Identifier is E3h, then the MCU should treat the Boot Block area as EEPROM. This will ensure compatibility with all future PSD813F2 and F4 devices.

Note: The MCU must not operate out of Main Flash while reading the Flash Memory Identifier. It can execute the Flash Memory Identifier command from some other memory, and store the ID value for later use.

This algorithm selection method only applies to the PSD813F2 and F4. The PSD813F1 will always use the EEPROM algorithm for the Boot Block area. The PSD813F3 and F5 have no Boot Block area.

Note that this algorithm selection method is not required when programming or erasing the main Flash memory. It only applies to programming or erasing the Boot Block area. Main Flash will always require the Flash algorithm defined in section 9.1.1.7, regardless of internal die composition.

**The
PSD813F
Functional
Blocks**
(cont.)

9.1.2 SRAM

The SRAM is a 16 Kbit (2K x 8) memory. The SRAM is enabled when RS0—the SRAM chip select output from the DPLD—is high. RS0 can contain up to two product terms, allowing flexible memory mapping.

The SRAM can be backed up using an external battery. The external battery should be connected to the Vstby pin (PC2). If you have an external battery connected to the PSD813F, the contents of the SRAM will be retained in the event of a power loss. The contents of the SRAM will be retained so long as the battery voltage remains at 2V or greater. If the supply voltage falls below the battery voltage, an internal power switchover to the battery occurs.

Pin PC4 can be configured as an output that indicates when power is being drawn from the external battery. This Vbaton signal will be high with the supply voltage falls below the battery voltage and the battery on PC2 is supplying power to the internal SRAM.

The chip select signal (RS0) for the SRAM, Vstby, and Vbaton are all configured using PSDsoft Configuration.

9.1.3 Memory Select Signals

The main Flash (FSi), optional EEPROM or Flash Boot (EESi/CSBOOTi), and SRAM (RS0) memory select signals are all outputs of the DPLD. They are setup by writing equations for them in PSDabel. The following rules apply to the equations for the internal chip select signals:

1. Flash memory and EEPROM or Flash Boot memory sector select signals must **not** be larger than the physical sector size.
2. Any main Flash memory sector must **not** be mapped in the same memory space as another Flash sector.
3. An EEPROM/Flash Boot memory sector must **not** be mapped in the same memory space as another EEPROM/Flash Boot sector.
4. SRAM, I/O, and Peripheral I/O spaces must **not** overlap.
5. An EEPROM/Flash Boot memory sector **may** overlap a main Flash memory sector. In case of overlap, priority will be given to the EEPROM/Flash Boot sector.
6. SRAM, I/O, and Peripheral I/O spaces **may** overlap any other memory sector. Priority will be given to the SRAM, I/O, or Peripheral I/O.

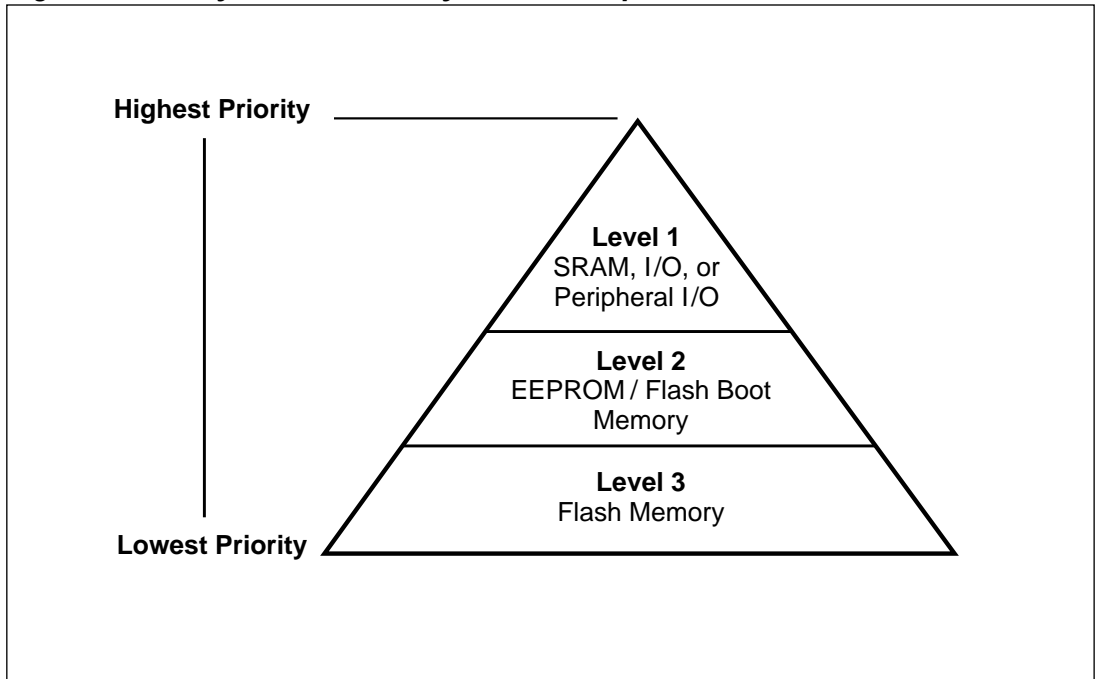
Example

FS0 is valid when the address is in the range of 8000h to BFFFh, EES0 is valid from 8000h to 9FFFh, and RS0 is valid from 8000h to 87FFh. Any address in the range of RS0 will always access the SRAM. Any address in the range of EES0 greater than 87FFh (and less than 9FFFh) will automatically address EEPROM memory segment 0. Any address greater than 9FFFh will access the Flash memory segment 0. You can see that half of the Flash memory segment 0 and one-fourth of EEPROM segment 0 can not be accessed in this example. Also note that an equation that defined FS1 to anywhere in the range of 8000h to BFFFh would **not** be valid.

Figure 7 shows the priority levels for all memory components. Any component on a higher level can overlap and has priority over any component on a lower level. Components on the same level must **not** overlap. Level one has the highest priority and level 3 has the lowest.

**The
PSD813F
Functional
Blocks
(cont.)**

Figure 7. Priority Level of Memory and I/O Components



9.1.3.1. Memory Select Configuration for MCUs with Separate Program and Data Spaces

The 8031 and compatible family of microcontrollers, which includes the 80C51, 80C151, 80C251, and 80C51XA, have separate address spaces for code memory (selected using PSEN) and data memory (selected using RD). Any of the memories within the PSD813F can reside in either space or both spaces. This is controlled through manipulation of the VM register that resides in the PSD’s CSIOP space.

The VM register is set using PSDsoft to have an initial value. It can subsequently be changed by the microcontroller so that memory mapping can be changed on-the-fly. For example, I may wish to have SRAM and Flash in Data Space at boot, and EEPROM in Program Space at boot, and later swap EEPROM and Flash. This is easily done with the VM register by using PSDsoft Configuration to configure it for boot up and having the microcontroller change it when desired.

Table 13 describes the VM Register.

Table 13. VM Register

Bit 7 PIO_EN	Bit 6*	Bit 5*	Bit 4 FL_Data	Bit 3 EE_Data	Bit 2 FL_Code	Bit 1 EE_Code	Bit 0 SRAM_Code
0 = disable PIO mode	*	*	0 = RD can't access Flash	0 = RD can't access EEPROM/ Boot Flash	0 = PSEN can't access Flash	0 = PSEN can't access EEPROM/ Boot Flash	0 = PSEN can't access SRAM
1 = enable PIO mode	*	*	1 = RD access Flash	1 = RD access EEPROM/ Boot Flash	1 = PSEN access Flash	1 = PSEN access EEPROM/ Boot Flash	1 = PSEN access SRAM

NOTE: Bits 6-5 are not used.

**The
PSD813F
Functional
Blocks
(cont.)**

9.1.3.2 Configuration Modes for MCUs with Separate Program and Data Spaces

9.1.3.2.1 Separate Space Modes

Code memory space is separated from data memory space. For example, the PSEN signal is used to access the program code from the Flash Memory, while the RD signal is used to access data from the EEPROM, SRAM and I/O Ports. This configuration requires the VM register to be set to 0Ch.

9.1.3.2.2 Combined Space Modes

The program and data memory spaces are combined into one space that allows the main Flash Memory, EEPROM, and SRAM to be accessed by either PSEN or RD. For example, to configure the main Flash memory in combined space mode, bits 2 and 4 of the VM register are set to "1".

9.1.3.2.3 Mixed Modes

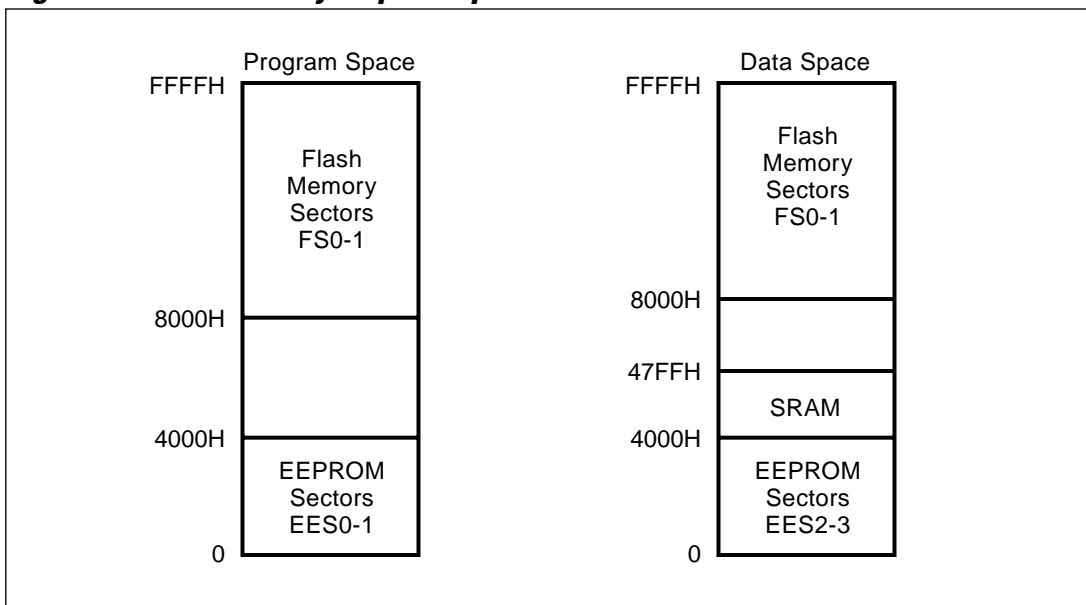
This allows individual Flash memory or EEPROM sectors with overlapping addresses to be configured in either Data Space or Program Space. Flash memory or EEPROM sector select signals must be qualified with the RD or PSEN input in the FS0-FS7 or EES0-EES3 equations. An active RD or PSEN will select memory sectors in the Data Space or in the Program Space. For memory sectors that reside in Data Space or Program Space, the access time is calculated from RD or PSEN valid to data valid.

9.1.3.5 80C31 Memory Map Example

In this example, the PSD Memory will be configured as shown in Figure 8.

**The
PSD813F
Functional
Blocks
(cont.)**

Figure 8. 80C31 Memory Map Example



- Flash Memory Sectors FS0-1 will be mapped from 8000-FFFFH in the Combined Space Mode (in both Program Space and Data Space). Bits 2 and 4 of the VM Register are set to 1.
- EEPROM Sectors EES0-1 will be mapped in the Program Space from 0000H-3FFFH. EEPROM Sectors EES2-3 will be mapped in the Data Space from 0000H-3FFFH. Bits 1 and 3 of the VM Register are set to 1.
- SRAM will be mapped in the Data Space from 4000-47FFH. Bit 0 of the VM Register is set to 0.

The Abel equations in PSDsoft will be as followed:

```

FS0 = (Address >= ^h8000) & (Address <= ^hBFFF);
FS1 = (Address >= ^hC000) & (Address <= ^hFFFF);
EES0 = (Address >= ^h0000) & (Address <= ^h1FFF) & !PSEN;
EES1 = (Address >= ^h2000) & (Address <= ^h3FFF) & !PSEN;
EES2 = (Address >= ^h0000) & (Address <= ^h1FFF) & PSEN;
EES3 = (Address >= ^h2000) & (Address <= ^h3FFF) & PSEN;
RS0 = (Address >= ^h4000) & (Address <= ^h47FF);
    
```

When the microcontroller reads the VM register, the contents read back are shown in Table 14. The VM Register content at power up is specified in PSDsoft.

Table 14. VM Register Contents in the 80C31 Memory Map Example

Bit 7 PIO_EN	Bit 6*	Bit 5*	Bit 4	Bit 3	Bit 2	Bit 1 RD_EN	Bit 0 PSEN_EN
0 = disable PIO mode	*	*	1 = RD can access Flash	1 = RD can access EEPROM/ Boot Flash	1 = PSEN can access Flash	1 = PSEN can access EEPROM/ Boot Flash	0 = PSEN can not access SRAM

NOTE: Bits 6-5 are not used.



The
PSD813F
Functional
Blocks
(cont.)

Figure 9. 8031 Memory Modes – Separate Space Mode

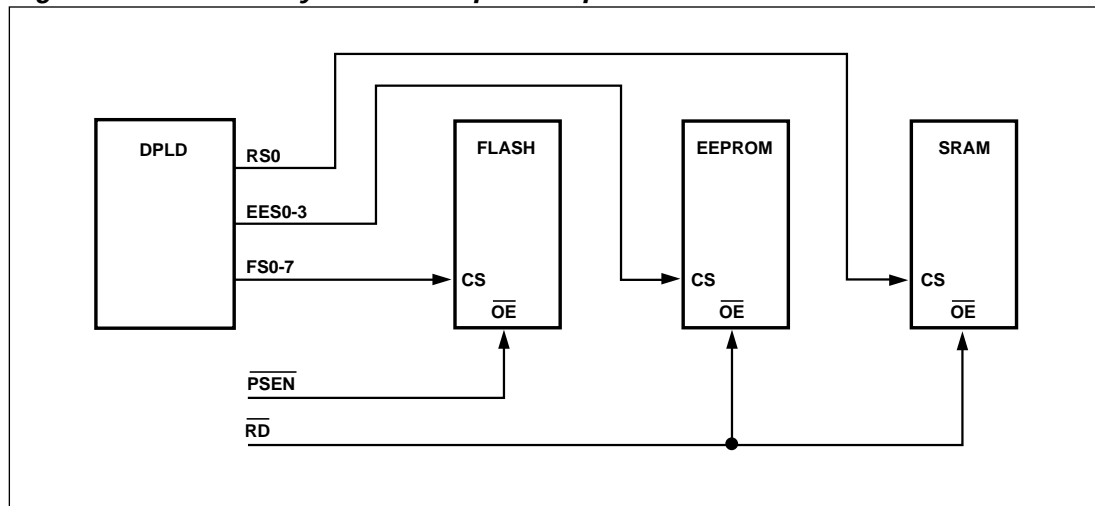
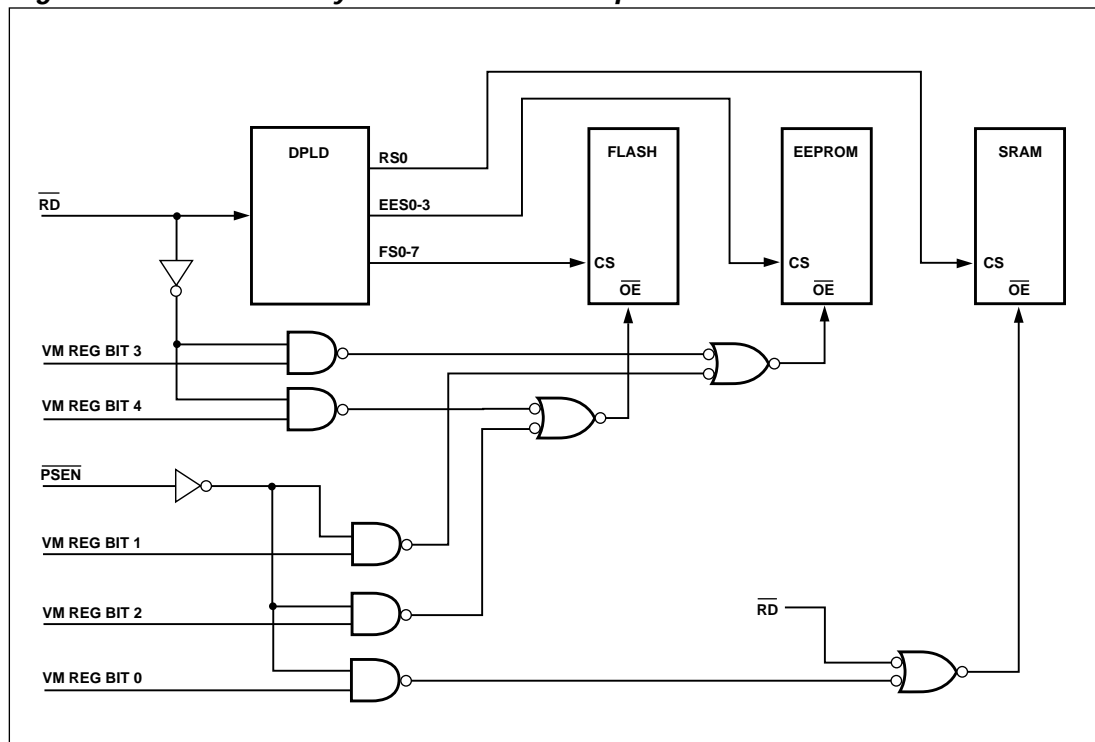


Figure 10. 80C31 Memory Mode – Combined Space Mode



**The
PSD813F
Functional
Blocks
(cont.)**

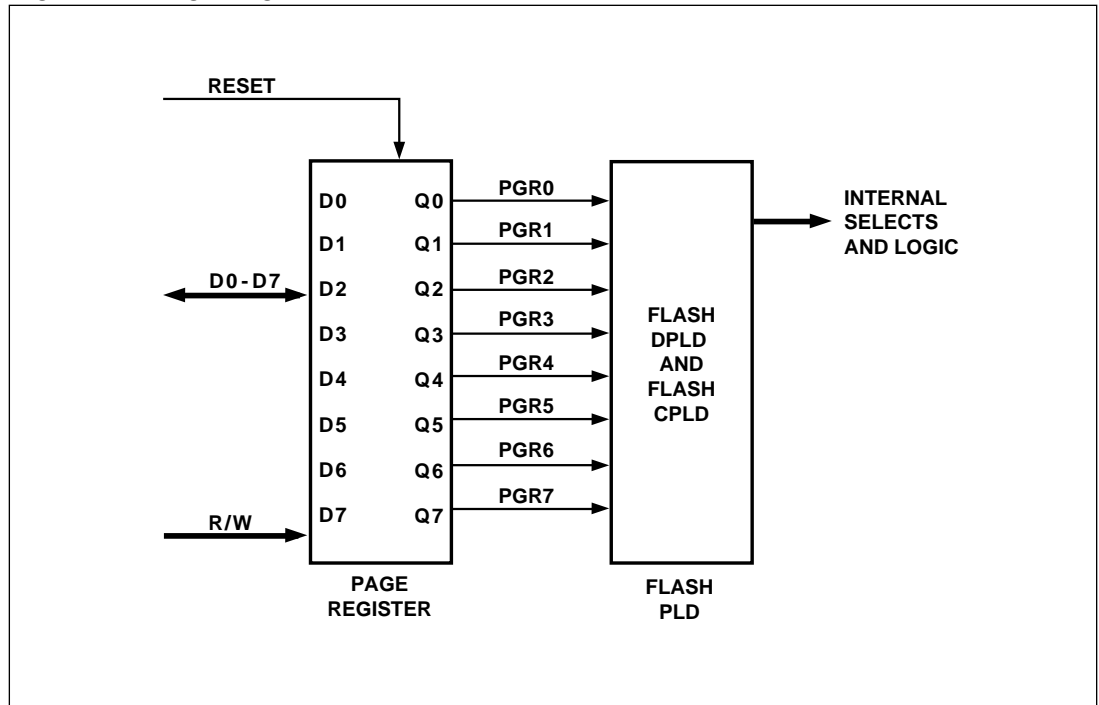
9.1.4 Page Register

The eight bit Page Register increases the addressing capability of the microcontroller by a factor of up to 256. The contents of the register can also be read by the microcontroller. The outputs of the Page Register (PGR0-PGR7) are inputs to the DPLD decoder and can be included in the Flash Memory, EEPROM, and SRAM chip select equations.

If memory paging is not needed, or if not all 8 page register bits are needed for memory paging, then these bits may be used in the CPLD for general logic. See Application Note 57.

Figure 11 shows the Page Register. The eight flip flops in the register are connected to the internal data bus D0-D7. The microcontroller can write to or read from the Page Register. The Page Register can be accessed at address location CSIOP + E0h.

Figure 11. Page Register



**The
PSD813F
Functional
Blocks**
(cont.)

9.2 PLDs

The PLDs bring programmable logic functionality to the PSD813F. After specifying the logic for the PLDs using the PSDabel tool in PSDsoft, the logic is programmed into the device and available upon power-up.

The PSD813F contains two PLDs: the Decode PLD (DPLD), and the Complex PLD (CPLD). The PLDs are briefly discussed in the next few paragraphs, and in more detail in sections 9.2.1 and 9.2.2. Figure 12 shows the configuration of the PLDs.

The DPLD performs address decoding for internal and external components, such as memory, registers, and I/O port selects.

The CPLD can be used for logic functions, such as loadable counters and shift registers, state machines, and encoding and decoding logic. These logic functions can be constructed using the 16 Output Micro↔Cells (OMCs), 24 Input Micro↔Cells (IMCs), and the AND array. The CPLD can also be used to generate external chip selects.

The AND array is used to form product terms. These product terms are specified using PSDabel. An Input Bus consisting of 73 signals is connected to the PLDs. The signals are shown in Table 15.

Table 15. DPLD and CPLD Inputs

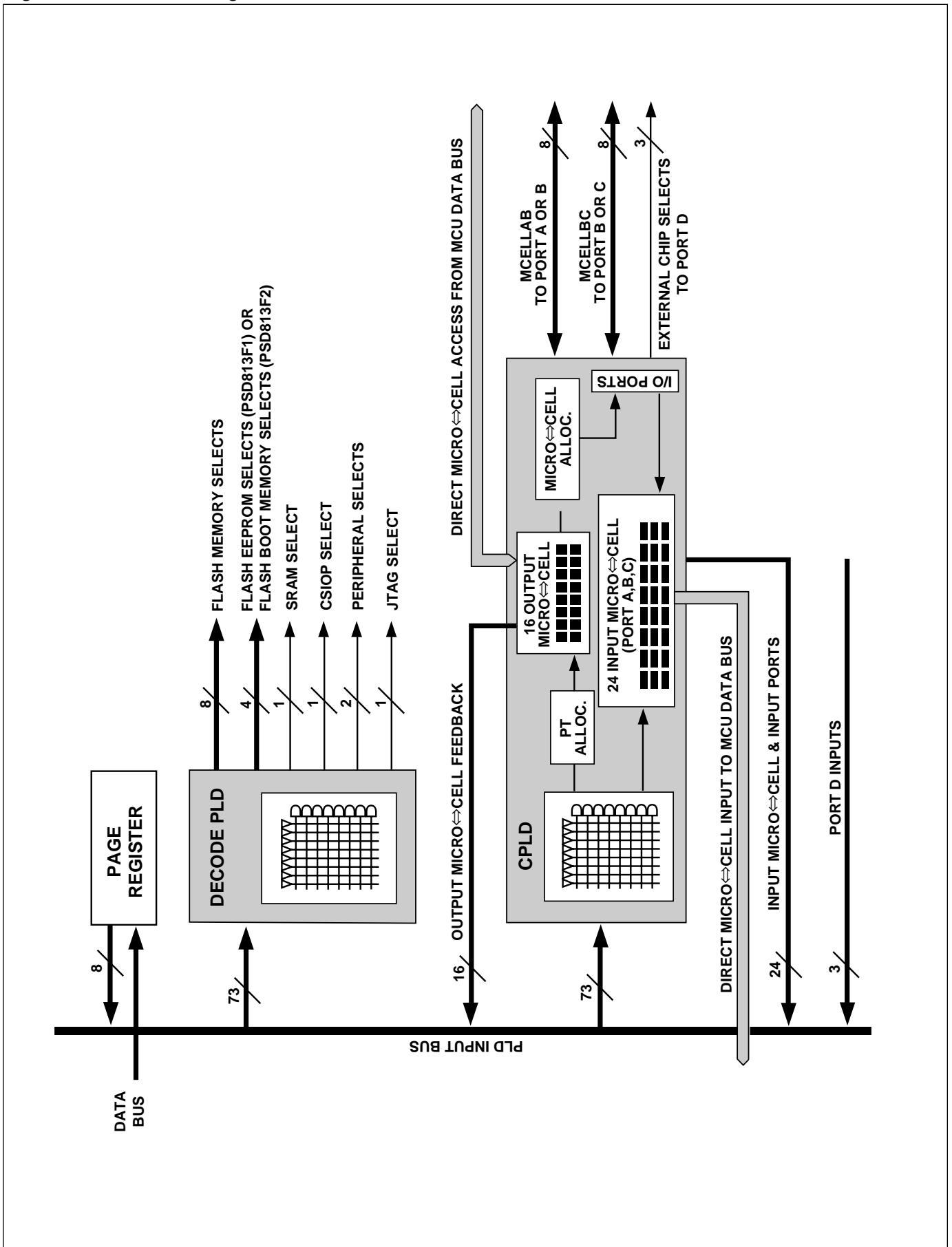
<i>Input Source</i>	<i>Input Name</i>	<i>Number of Signals</i>
MCU Address Bus	A[15:0]*	16
MCU Control Signals	CNTL[2:0]	3
Reset	RST	1
Power Down	PDN	1
Port A Input Micro↔Cells	PA[7-0]	8
Port B Input Micro↔Cells	PB[7-0]	8
Port C Input Micro↔Cells	PC[7-0]	8
Port D Inputs	PD[2:0]	3
Page Register	PGR(7:0)	8
Micro↔Cell AB Feedback	MCELLAB.FB[7:0]	8
Micro↔Cell BC Feedback	MCELLBC.FB[7:0]	8
EEPROM/Boot Flash Programming Status Bit	Rdy/Bsy	1

NOTE: The address inputs are A[19:4] in 80C51XA mode.

The Turbo Bit in ZPSD813F

The PLDs in the ZPSD813F can minimize power consumption by switching off when inputs remain unchanged for an extended time of about 70 ns. Setting the Turbo mode bit to off (Bit 3 of the PMMR0 register) automatically places the PLDs into standby if no inputs are changing. Turbo-off mode increases propagation delays while reducing power consumption. Refer to the Power Management Unit section on how to set the Turbo Bit. Additionally, five bits are available in the PMMR2 register to block MCU control signals from entering the PLDs. This reduces power consumption and can be used only when these MCU control signals are not used in PLD logic equations.

Figure 12. PLD Block Diagram



The PSD813F Functional Blocks (cont.)

Each of the two PLDs has unique characteristics suited for its applications. They are described in the following sections.

9.2.1 Decode PLD (DPLD)

The DPLD, shown in Figure 13, is used for decoding the address for internal and external components. The DPLD can generate the following decode signals:

- 8 sector selects for the main Flash memory (three product terms each)
- 4 sector selects for the optional EEPROM or Flash Boot memory (three product terms each)
- 1 internal SRAM select signal (two product terms)
- 1 internal CSIOP (PSD configuration register) select signal
- 1 JTAG select signal (enables JTAG on Port C)
- 2 internal peripheral select signals (peripheral I/O mode).

9.2.2 Complex PLD (CPLD)

The CPLD can be used to implement system logic functions, such as loadable counters and shift registers, system mailboxes, handshaking protocols, state machines, and random logic. The CPLD can also be used to generate 3 external chip selects, routed to Port D. Although external chip selects can be produced by any Output Micro↔Cell, these three external chip selects on Port D do not consume any Output Micro↔Cells.

As shown in Figure 12, the CPLD has the following blocks:

- 24 Input Micro↔Cells (IMCs)
- 16 Output Micro↔Cells (OMCs)
- Micro↔Cell Allocator
- Product Term Allocator
- AND array capable of generating up to 137 product terms
- Four I/O ports.

Each of the blocks are described in the subsections that follow.

The Input and Output Micro↔Cells are connected to the PSD813F internal data bus and can be directly accessed by the microcontroller. This enables the MCU software to load data into the Output Micro↔Cells or read data from both the Input and Output Micro↔Cells. This feature allows efficient implementation of system logic and eliminates the need to connect the data bus to the AND logic array as required in most standard PLD macrocell architectures.

Figure 13. DPLD Logic Array

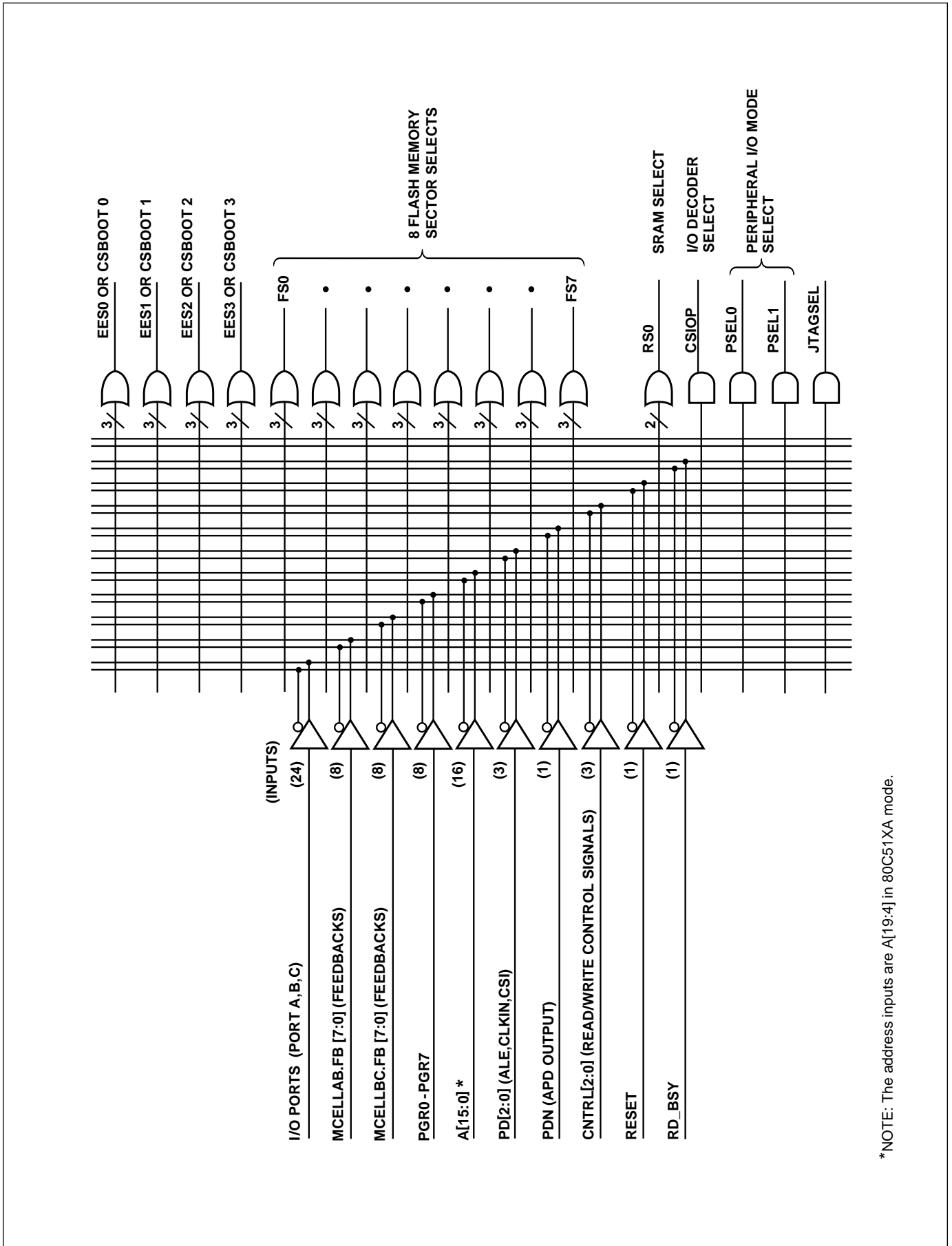
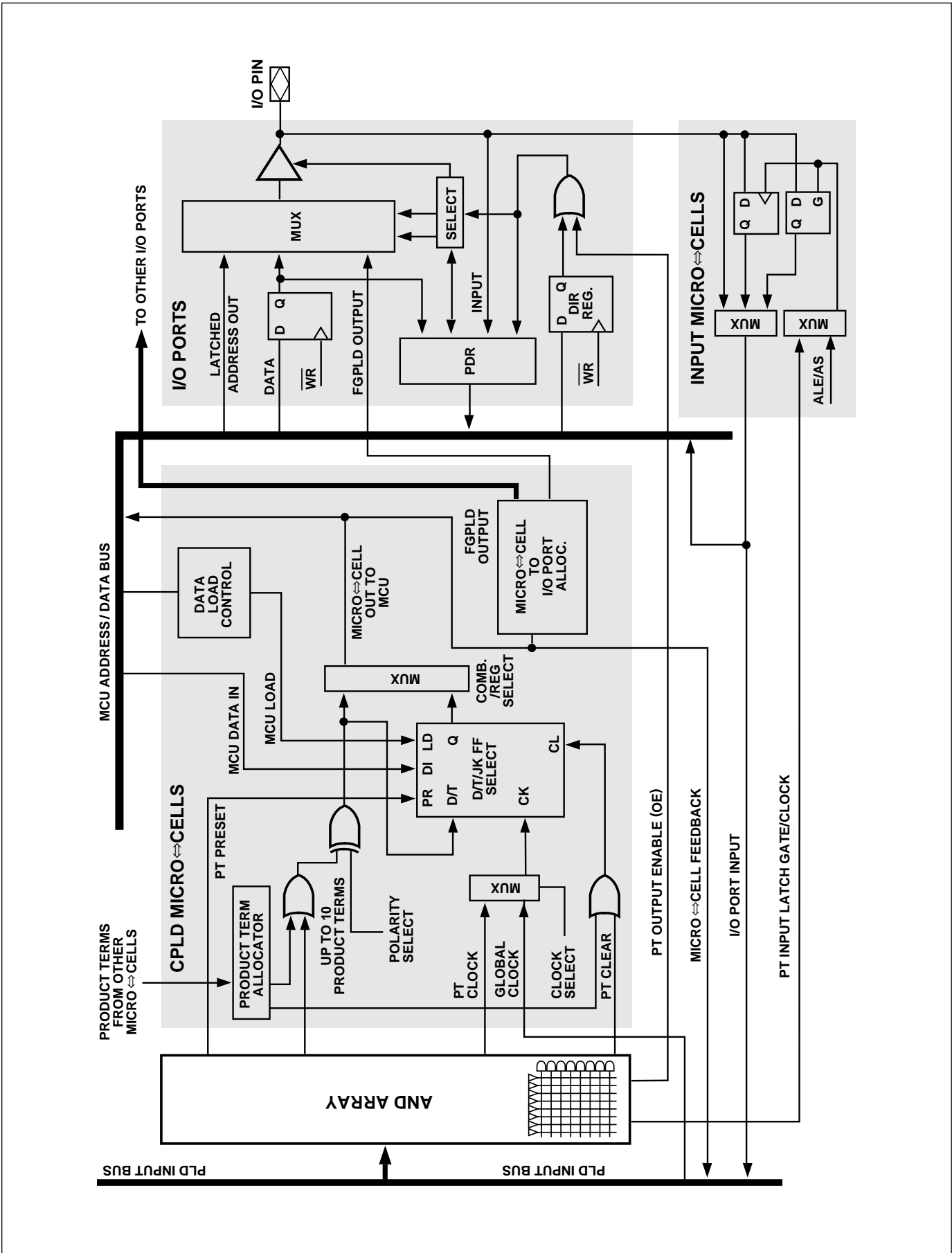


Figure 14. The Micro \leftrightarrow Cell and I/O Port



**The
PSD813F
Functional
Blocks
(cont.)**

9.2.2.1 Output Micro \leftrightarrow Cell

Eight of the Output Micro \leftrightarrow Cells are connected to Ports A and B pins and are named as McellAB0-7. The other eight Micro \leftrightarrow Cells are connected to Ports B and C pins and are named as McellBC0-7. If an McellAB output is not assigned to a specific pin in PSDabel, the Micro \leftrightarrow Cell Allocator will assign it to either Port A or B. The same is true for a McellBC output on Port B or C. Table 16 shows the Micro \leftrightarrow Cells and Port assignment.

Table 16. Output Micro \leftrightarrow Cell Port and Data Bit Assignments

Output Micro\leftrightarrowCell	Port Assignment	Native Product Terms	Maximum Borrowed Product Terms	Data Bit for Loading or Reading
McellAB0	Port A0, B0	3	6	D0
McellAB1	Port A1, B1	3	6	D1
McellAB2	Port A2, B2	3	6	D2
McellAB3	Port A3, B3	3	6	D3
McellAB4	Port A4, B4	3	6	D4
McellAB5	Port A5, B5	3	6	D5
McellAB6	Port A6, B6	3	6	D6
McellAB7	Port A7, B7	3	6	D7
McellBC0	Port B0, C0	4	5	D0
McellBC1	Port B1, C1	4	5	D1
McellBC2	Port B2, C2	4	5	D2
McellBC3	Port B3, C3	4	5	D3
McellBC4	Port B4, C4	4	6	D4
McellBC5	Port B5, C5	4	6	D5
McellBC6	Port B6, C6	4	6	D6
McellBC7	Port B7, C7	4	6	D7

The Output Micro \leftrightarrow Cell (OMC) architecture is shown in Figure 15. As shown in the figure, there are native product terms available from the AND array, and borrowed product terms available (if unused) from other OMCs. The polarity of the product term is controlled by the XOR gate. The OMC can implement either sequential logic, using the flip-flop element, or combinatorial logic. The multiplexer selects between the sequential or combinatorial logic outputs. The multiplexer output can drive a Port pin and has a feedback path to the AND array inputs.

The flip-flop in the OMC can be configured as a D, T, JK, or SR type in the PSDabel program. The flip-flop's clock, preset, and clear inputs may be driven from a product term of the AND array. Alternatively, the external CLKIN signal can be used for the clock input to the flip-flop. The flip-flop is clocked on the rising edge of the clock input. The preset and clear are active-high inputs. Each clear input can use up to two product terms.

**The
PSD813F
Functional
Blocks**
(cont.)

9.2.2.2 The Product Term Allocator

The CPLD has a Product Term Allocator. The PSDabel compiler uses the Allocator to borrow and place product terms from one Micro \leftrightarrow Cell to another. The following list summarizes how product terms are allocated:

- McellAB0-7 all have three native product terms and may borrow up to six more
- McellBC0-3 all have four native product terms and may borrow up to five more
- McellBC4-7 all have four native product terms and may borrow up to six more.

Each Micro \leftrightarrow Cell may only borrow product terms from certain other Micro \leftrightarrow Cells. Product terms already in use by one Micro \leftrightarrow Cell will not be available for a different Micro \leftrightarrow Cell.

If an equation requires more product terms than what is available to it, then “external” product terms will be required, which will consume other OMCs. If external product terms are used, extra delay will be added for the equation that required the extra product terms. This is called product term expansion. PSDsoft will perform this expansion as needed.

9.2.2.3 Loading and Reading the Output Micro \leftrightarrow Cells (OMCs)

The OMCs occupy a memory location in the MCU address space, as defined by the CSIOP (refer to the I/O section). The flip-flops in each of the 16 OMCs can be loaded from the data bus by a microcontroller. Loading the OMCs with data from the MCU takes priority over internal functions. As such, the preset, clear, and clock inputs to the flip-flop can be overridden by the MCU. The ability to load the flip-flops and read them back is useful in such applications as loadable counters and shift registers, mailboxes, and handshaking protocols.

Data can be loaded to the OMCs on the trailing edge of the WR signal (edge loading) or during the time that the WR signal is active (level loading). The method of loading is specified in PSDsoft Configuration.

9.2.2.4 The OMC Mask Register

There is one Mask Register for each of the two groups of eight OMCs. The Mask Registers can be used to block the loading of data to individual OMCs. The default value for the Mask Registers is 00h, which allows loading of the OMCs. When a given bit in a Mask Register is set to a ‘1’, the MCU will be blocked from writing to the associated OMC. For example, suppose McellAB0-3 are being used for a state machine. You would not want a MCU write to McellAB to overwrite the state machine registers. Therefore, you would want to load the Mask Register for McellAB (Mask Micro \leftrightarrow Cell AB) with the value 0Fh.

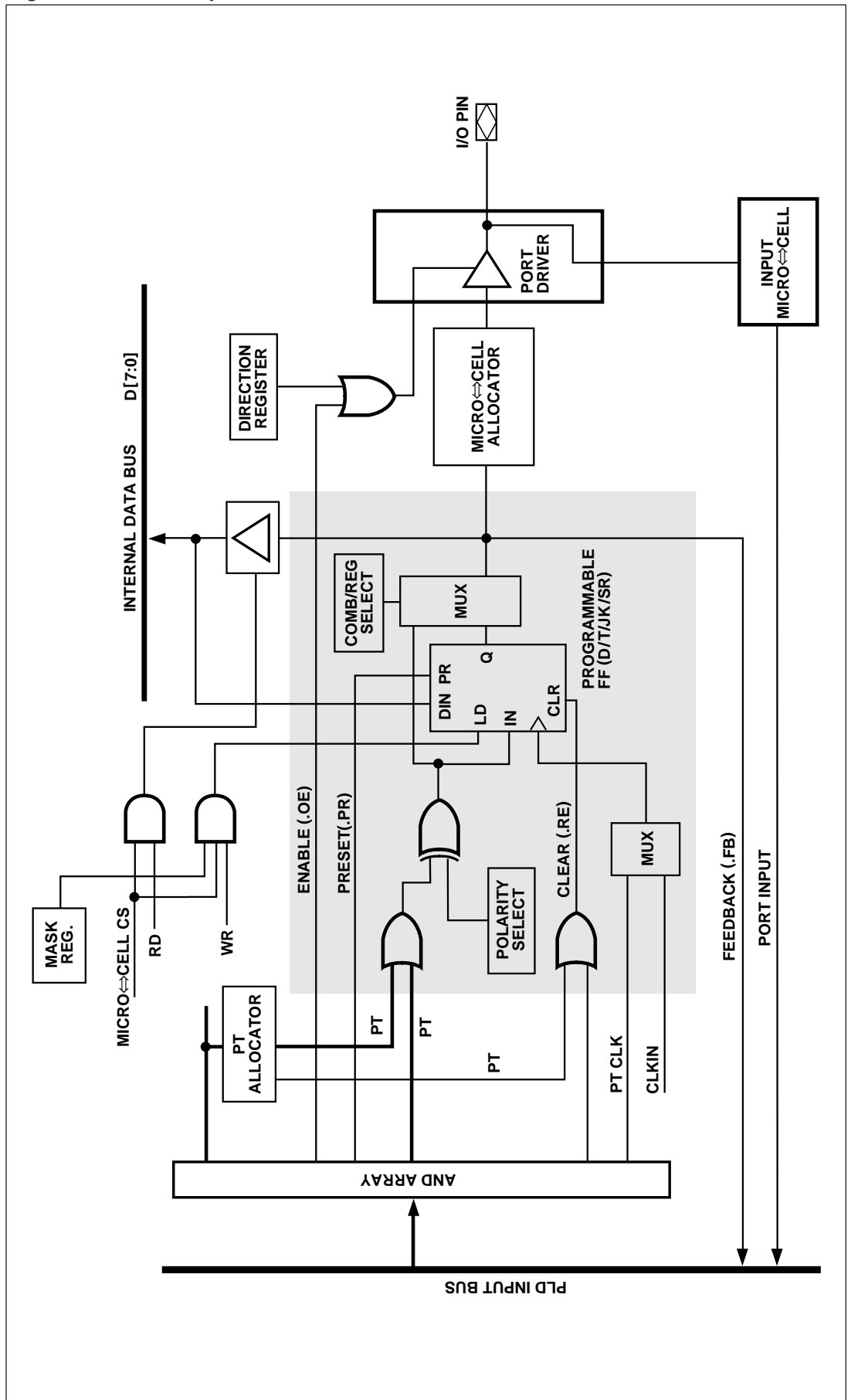
9.2.2.5 The Output Enable of the OMC

The OMC can be connected to an I/O port pin as a PLD output. The output enable of each Port pin driver is controlled by a single product term from the AND array, ORed with the Direction Register output. The pin is enabled upon power up if no output enable equation is defined and if the pin is declared as a PLD output in PSDsoft.

If the OMC output is declared as an internal node and not as a Port pin output in the PSDabel file, then the Port pin can be used for other I/O functions. The internal node feedback can be routed as an input to the AND array.

The
PSD813F
Functional
Blocks
(cont.)

Figure 15. CPLD Output Micro \leftrightarrow Cell



**The
PSD813F
Functional
Blocks**
(cont.)

9.2.2.6 Input Micro \leftrightarrow Cells (IMCs)

The CPLD has 24 IMCs, one for each pin on Ports A, B, and C. The architecture of the IMC is shown in Figure 16. The IMCs are individually configurable, and can be used as a latch, register, or to pass incoming Port signals prior to driving them onto the PLD input bus. The outputs of the IMCs can be read by the microcontroller through the internal data bus.

The enable for the latch and clock for the register are driven by a multiplexer whose inputs are a product term from the CPLD AND array or the MCU address strobe (ALE/AS). Each product term output is used to latch or clock four IMCs. Port inputs 3-0 can be controlled by one product term and 7-4 by another.

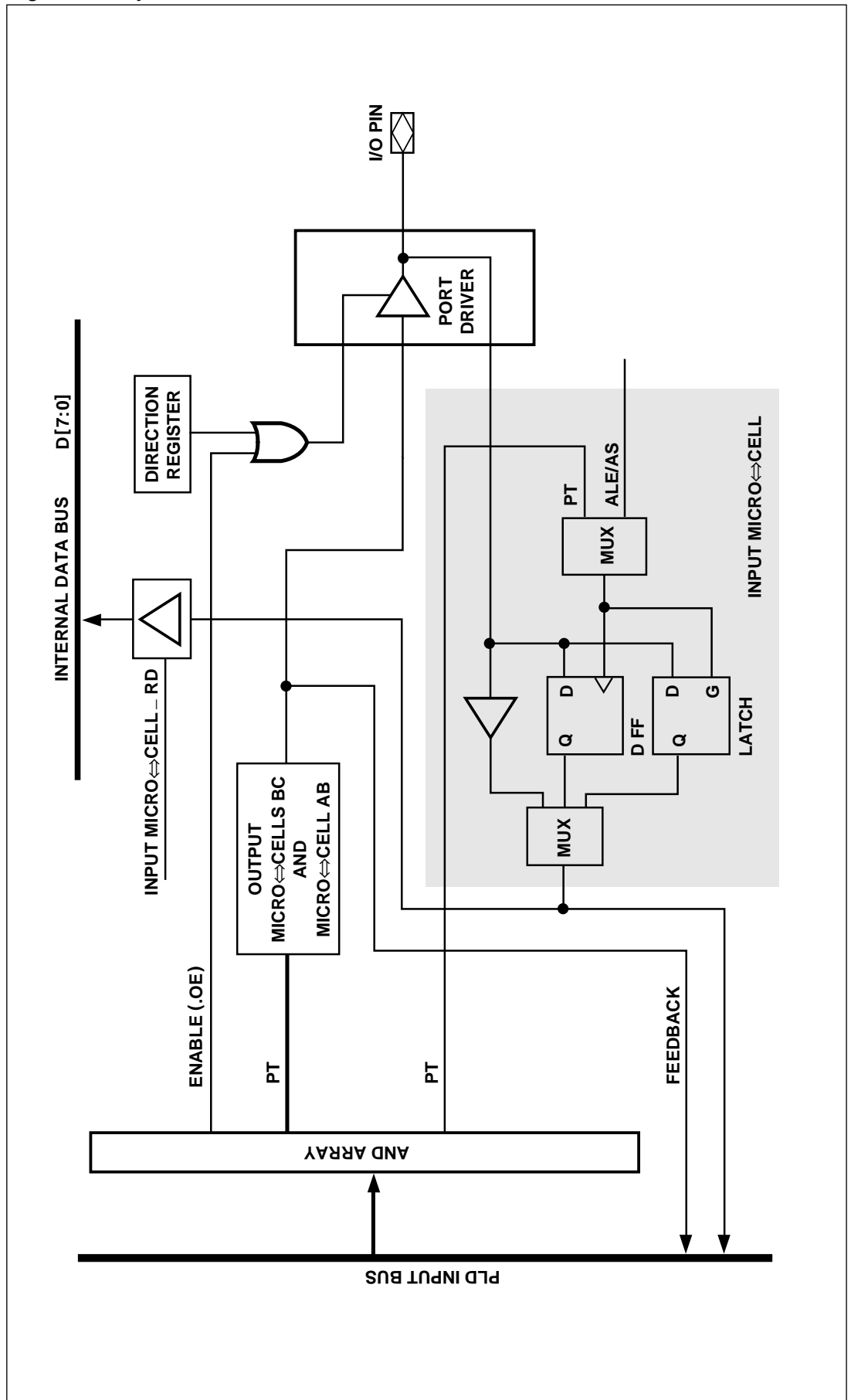
Configurations for the IMCs are specified by equations written in PSDLabel (see Application Note 55). Outputs of the IMCs can be read by the MCU via the IMC buffer. See the I/O Port section on how to read the IMCs.

IMCs can use the address strobe to latch address bits higher than A15. Any latched addresses are routed to the PLDs as inputs.

IMCs are particularly useful with handshaking communication applications where two processors pass data back and forth through a common mailbox. Figure 17 shows a typical configuration where the Master MCU writes to the Port A Data Out Register. This, in turn, can be read by the Slave MCU via the activation of the "Slave-Read" output enable product term. The Slave can also write to the Port A IMCs and the Master can then read the IMCs directly. Note that the "Slave-Read" and "Slave-Wr" signals are product terms that are derived from the Slave MCU inputs RD, WR, and Slave_CS.

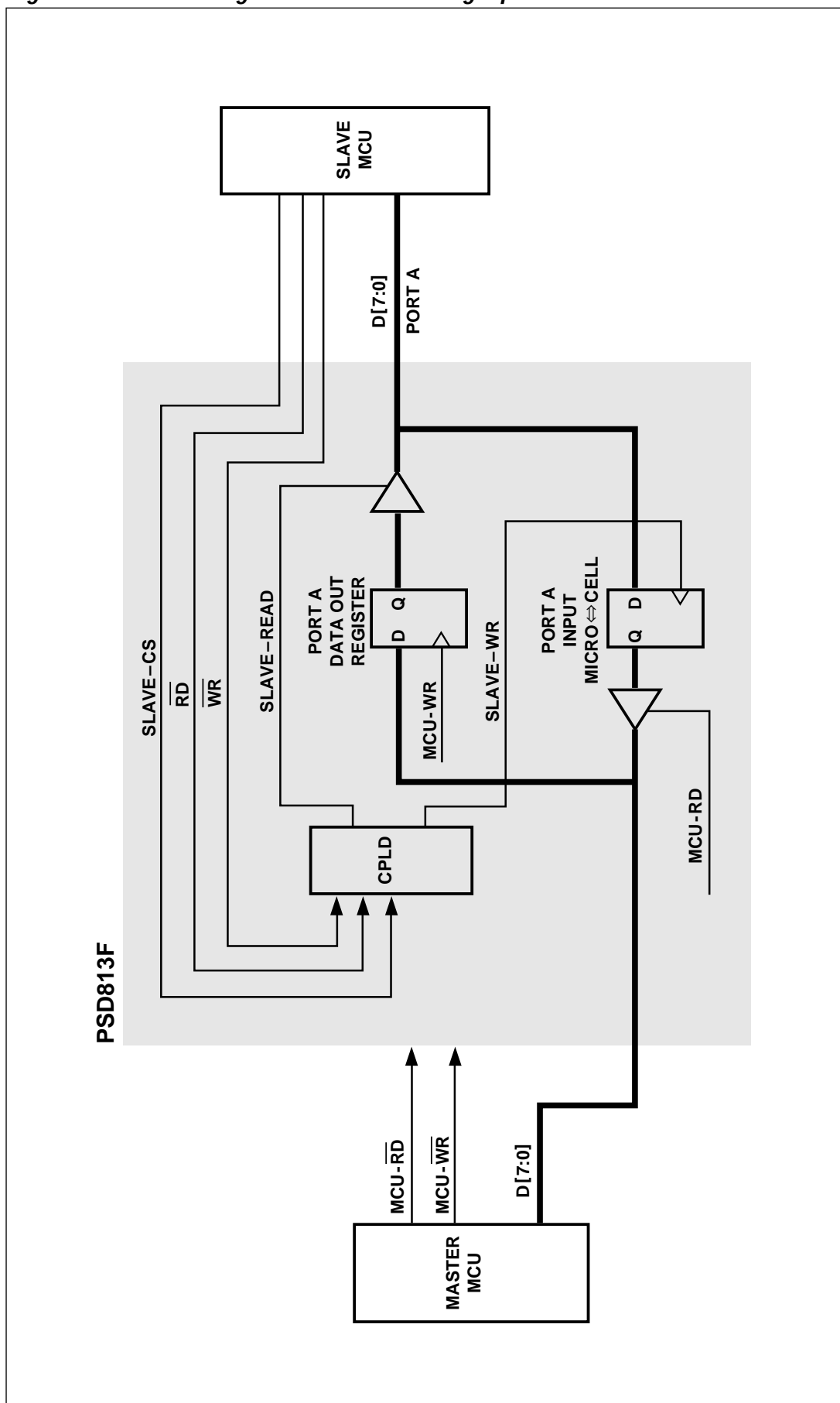
The
PSD813F
Functional
Blocks
(cont.)

Figure 16. Input Micro⇔Cell



The
PSD813F
Functional
Blocks
(cont.)

Figure 17. Handshaking Communication Using Input Micro⇔Cells



**The
PSD813F
Functional
Blocks**
(cont.)

9.3 Microcontroller Bus Interface

The “no-glue logic” PSD813F Microcontroller Bus Interface can be directly connected to most popular microcontrollers and their control signals. Key 8-bit microcontrollers with their bus types and control signals are shown in Table 17. The interface type is specified using the PSDsoft Configuration.

Table 17. Microcontrollers and their Control Signals

MCU	Data Bus Width	CNTL0	CNTL1	CNTL2	PC7	PD0**	ADIO0	PA3-PA0	PA7-PA3
8031	8	\overline{WR}	\overline{RD}	\overline{PSEN}	*	ALE	A0	*	*
80C51XA	8	\overline{WR}	\overline{RD}	\overline{PSEN}	*	ALE	A4	A3-A0	*
80C251	8	\overline{WR}	\overline{PSEN}	*	*	ALE	A0	*	*
80C251	8	\overline{WR}	\overline{RD}	\overline{PSEN}	*	ALE	A0	*	*
80198	8	\overline{WR}	\overline{RD}	*	*	ALE	A0	*	*
68HC11	8	R/\overline{W}	E	*	*	AS	A0	*	*
68HC912	8	R/\overline{W}	E	*	\overline{DBE}	AS	A0	*	*
Z80	8	\overline{WR}	\overline{RD}	*	*	*	A0	D3-D0	D7-D4
NEURON 3150 CHIP	8	R/\overline{W}	\overline{E}	*	*	*	A0	D3-D0	D7-D4
Z8	8	R/\overline{W}	\overline{DS}	*	*	\overline{AS}	A0	*	*
68330	8	R/\overline{W}	\overline{DS}	*	*	AS	A0	*	*
M37702M2	8	R/\overline{W}	\overline{E}	*	*	ALE	A0	D3-D0	D7-D4

*Unused CNTL2 pin can be configured as CPLD input. Other unused pins (PC7, PD0, PA3-0) can be configured for other I/O functions.

**ALE/AS input is optional for microcontrollers with a non-multiplexed bus

9.3.1. Interfacing 16-bit MCUs with Two PSD813F Devices.

The PSD813F has an internal 8-bit data bus. Users of 16-bit data bus MCUs can connect two PSD813F devices in parallel such that one is tied to the upper data byte (D15-D8) and the other is connected to the lower data byte (D7-D0). Refer to PSD813F Application Notes on the configuration of two PSD813F to 16-bit MCUs.

9.3.2. PSD813F Interface to a Multiplexed 8-Bit Bus

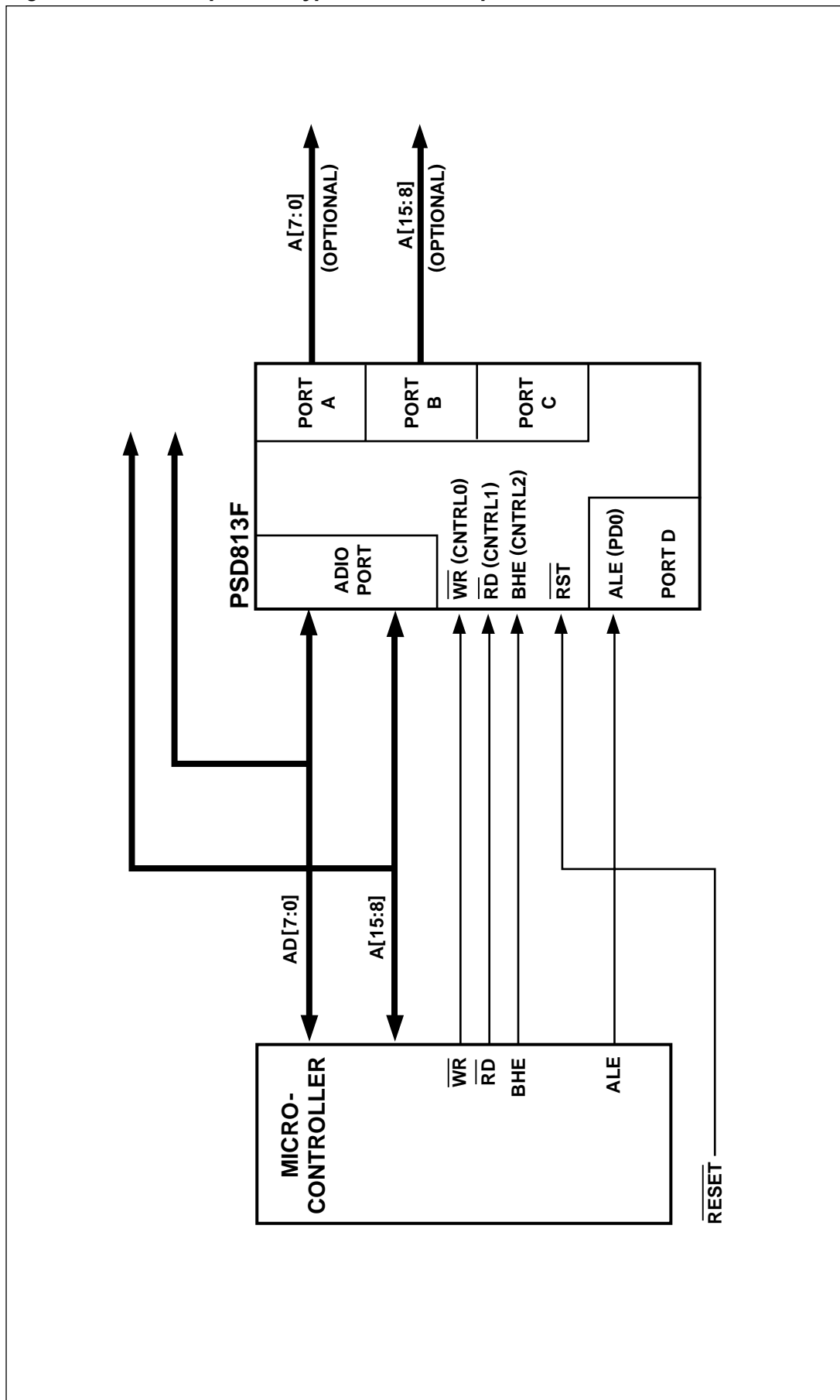
Figure 18 shows an example of a system using a microcontroller with an 8-bit multiplexed bus and a PSD813F. The ADIO port on the PSD813F is connected directly to the microcontroller address/data bus. ALE latches the address lines internally. Latched addresses can be brought out to Port A or B. The PSD813F drives the ADIO data bus only when one of its internal resources is accessed and the RD input is active. Should the system address bus exceed sixteen bits, Ports A, B, C, or D may be used as additional address inputs.

9.3.3. PSD813F Interface to a Non-Multiplexed 8-Bit Bus

Figure 19 shows an example of a system using a microcontroller with an 8-bit non-multiplexed bus and a PSD813F. The address bus is connected to the ADIO Port, and the data bus is connected to Port A. Port A is in tri-state mode when the PSD813F is not accessed by the microcontroller. Should the system address bus exceed sixteen bits, Ports B, C, or D may be used for additional address inputs.

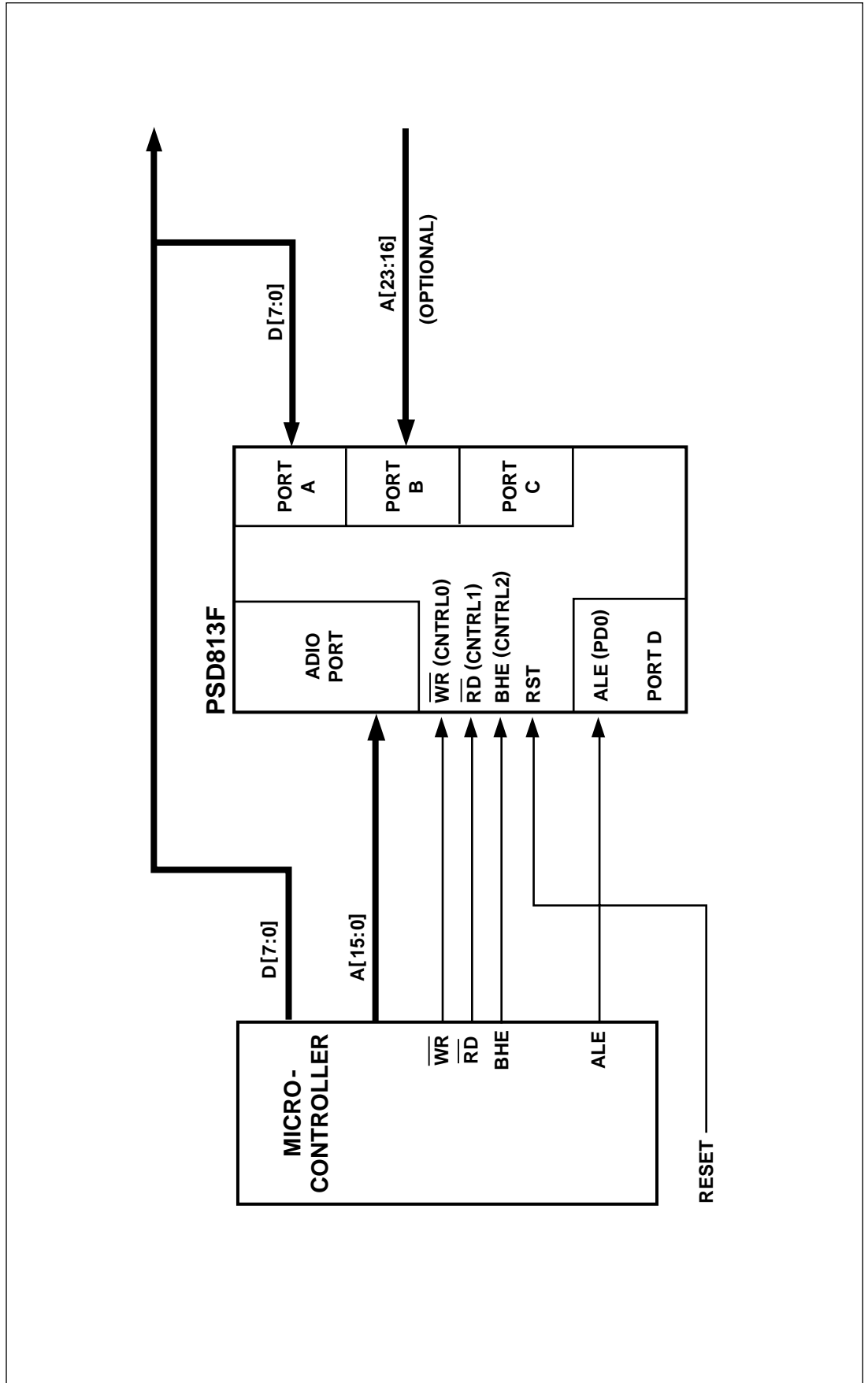
The
PSD813F
Functional
Blocks
(cont.)

Figure 18. An Example of a Typical 8-Bit Multiplexed Bus Interface



The PSD813F Functional Blocks (cont.)

Figure 19. An Example of a Typical 8-Bit Non-Multiplexed Bus Interface



**The
PSD813F
Functional
Blocks**
(cont.)

9.3.4 Data Byte Enable Reference

Microcontrollers have different data byte orientations. The following table shows how the PSD813F interprets byte/word operations in different bus write configurations. Even-byte refers to locations with address A0 equal to zero and odd byte as locations with A0 equal to one.

Table 18. Eight-Bit Data Bus

BHE	A0	D7-D0
X	0	Even Byte
X	1	Odd Byte

9.3.5 Microcontroller Interface Examples

Figures 20 through 24 show examples of the basic connections between the PSD813F and some popular microcontrollers. The PSD813F Control input pins are labeled as to the microcontroller function for which they are configured. The MCU interface is specified using the PSDsoft Configuration.

9.3.5.1 80C31

Figure 20 shows the interface to the 80C31, which has an 8-bit multiplexed address/data bus. The lower address byte is multiplexed with the data bus. The microcontroller control signals PSEN, RD, and WR may be used for accessing the internal memory components and I/O Ports. The ALE input (pin PD0) latches the address.

9.3.5.2 80C251

The Intel 80C251 microcontroller features a user-configurable bus interface with four possible bus configurations, as shown in Table 19.

Configuration 1 is 80C31 compatible, and the bus interface to the PSD813F is identical to that shown in Figure 20. Configurations 2 and 3 have the same bus connection as shown in Figure 21. There is only one read input (PSEN) connected to the Cnt11 pin on the PSD813F. The A16 connection to the PA0 pin allows for a larger address input to the PSD813F. Configuration 4 is shown in Figure 22. The RD signal is connected to Cnt11 and the PSEN signal is connected to the CNTL2.

The 80C251 has two major operating modes: Page Mode and Non-Page Mode. In Non-Page Mode, the data is multiplexed with the lower address byte, and ALE is active in every bus cycle. In Page Mode, data D[7:0] is multiplexed with address A[15:8]. In a bus cycle where there is a Page hit, the ALE signal is not active and only addresses A[7:0] are changing. The PSD813F supports both modes. In Page Mode, the PSD bus timing is identical to Non-Page Mode except the address hold time and setup time with respect to ALE is not required. The PSD access time is measured from address A[7:0] valid to data in valid.

**The
PSD813F
Functional
Blocks
(cont.)**

Table 19. 80C251 Configurations

Configuration	80C251 Read/Write Pins	Connecting to PSD813F Pins	Page Mode
1	\overline{WR} \overline{RD} \overline{PSEN}	CNTL0 CNTL1 CNTL2	Non-Page Mode, 80C31 compatible A[7:0] multiplex with D[7:0]
2	\overline{WR} \overline{PSEN} only	CNTL0 CNTL1	Non-Page Mode A[7:0] multiplex with D[7:0]
3	\overline{WR} \overline{PSEN} only	CNTL0 CNTL1	Page Mode A[15:8] multiplex with D[7:0]
4	\overline{WR} \overline{RD} \overline{PSEN}	CNTL0 CNTL1 CNTL2	Page Mode A[15:8] multiplex with D[7:0]

9.3.5.3 80C51XA

The Philips 80C51XA microcontroller family supports an 8- or 16-bit multiplexed bus that can have burst cycles. Address bits A[3:0] are not multiplexed, while A[19:4] are multiplexed with data bits D[15:0] in 16-bit mode. In 8-bit mode, A[11:4] are multiplexed with data bits D[7:0].

The 80C51XA can be configured to operate in eight-bit data mode. (shown in Figure 23). The 80C51XA improves bus throughput and performance by executing Burst cycles for code fetches. In Burst Mode, address A19-4 are latched internally by the PSD813F, while the 80C51XA changes the A3-0 lines to fetch up to 16 bytes of code. The PSD access time is then measured from address A3-A0 valid to data in valid. The PSD bus timing requirement in Burst Mode is identical to the normal bus cycle, except the address setup and hold time with respect to ALE does not apply.

9.3.5.4 68HC11

Figure 24 shows an interface to a 68HC11 where the PSD813F1 is configured in 8-bit multiplexed mode with \overline{E} and R/W settings. The DPLD can generate the READ and WR signals for external devices.

Figure 20. Interfacing the PSD813F with an 80C31

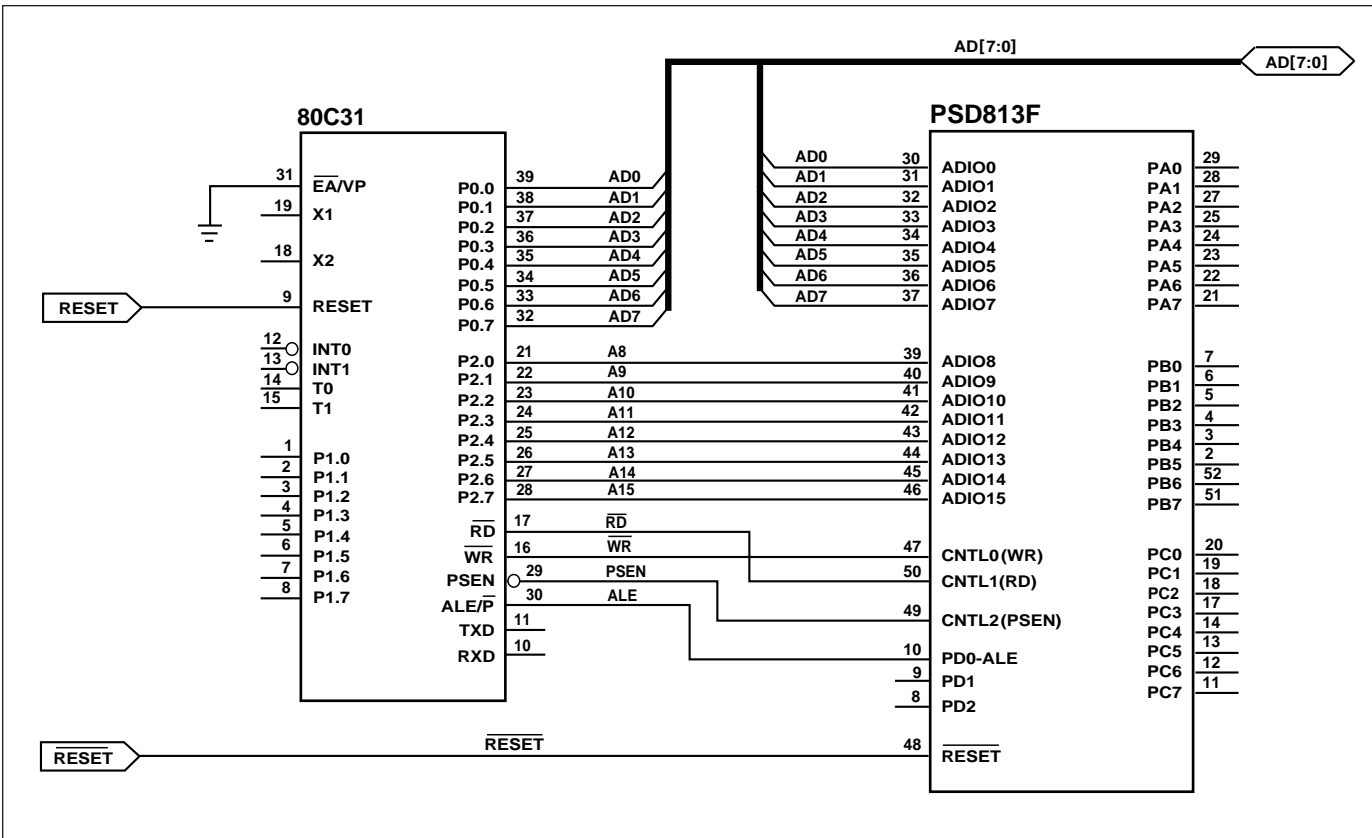


Figure 21. Interfacing the PSD813F to the 80C251, with One Read Input

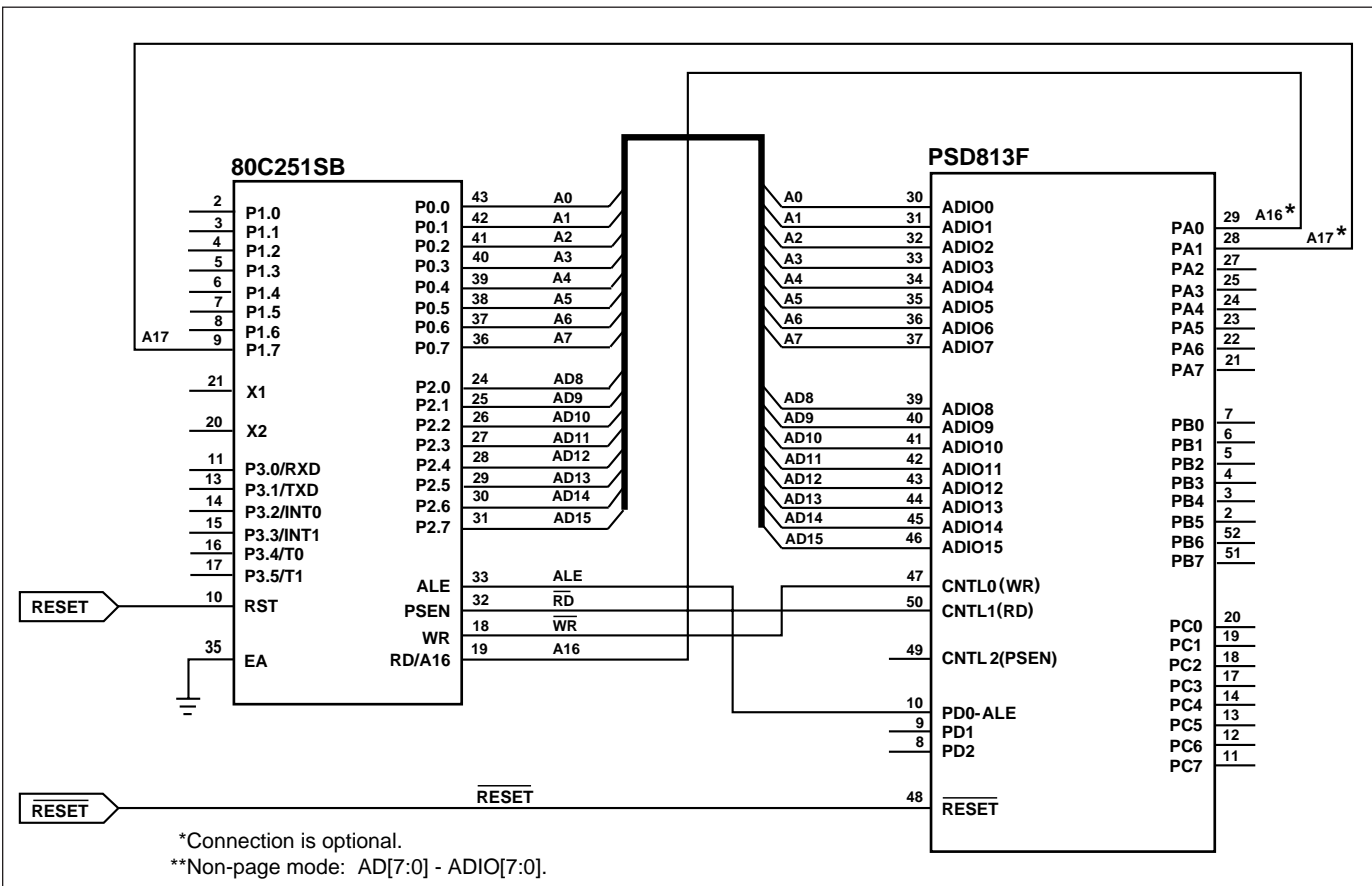


Figure 22. Interfacing the PSD813F to the 80C251, with Read and PSEN Inputs

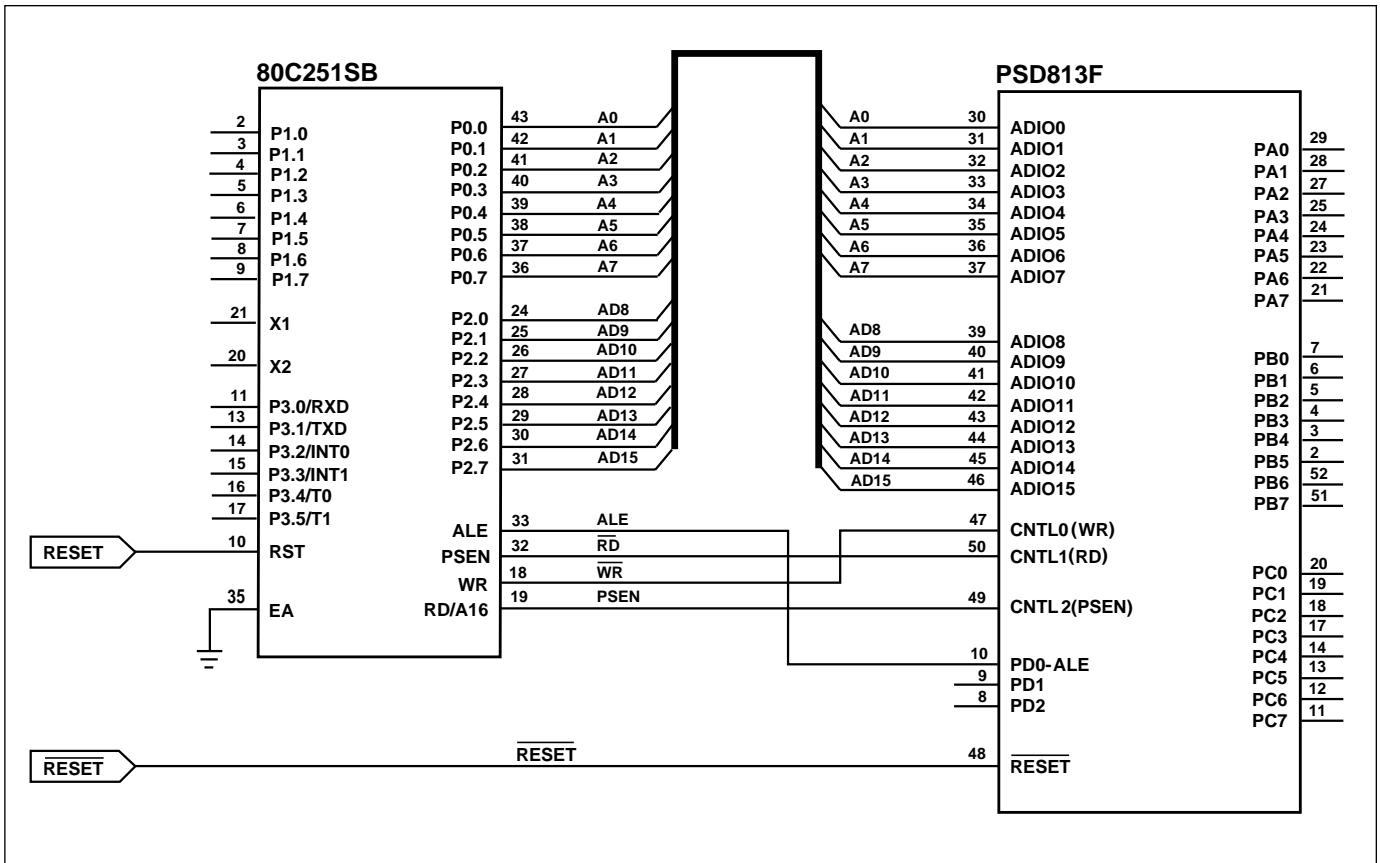


Figure 23. Interfacing the PSD813F to the 80C51XA, 8-Bit Data Bus

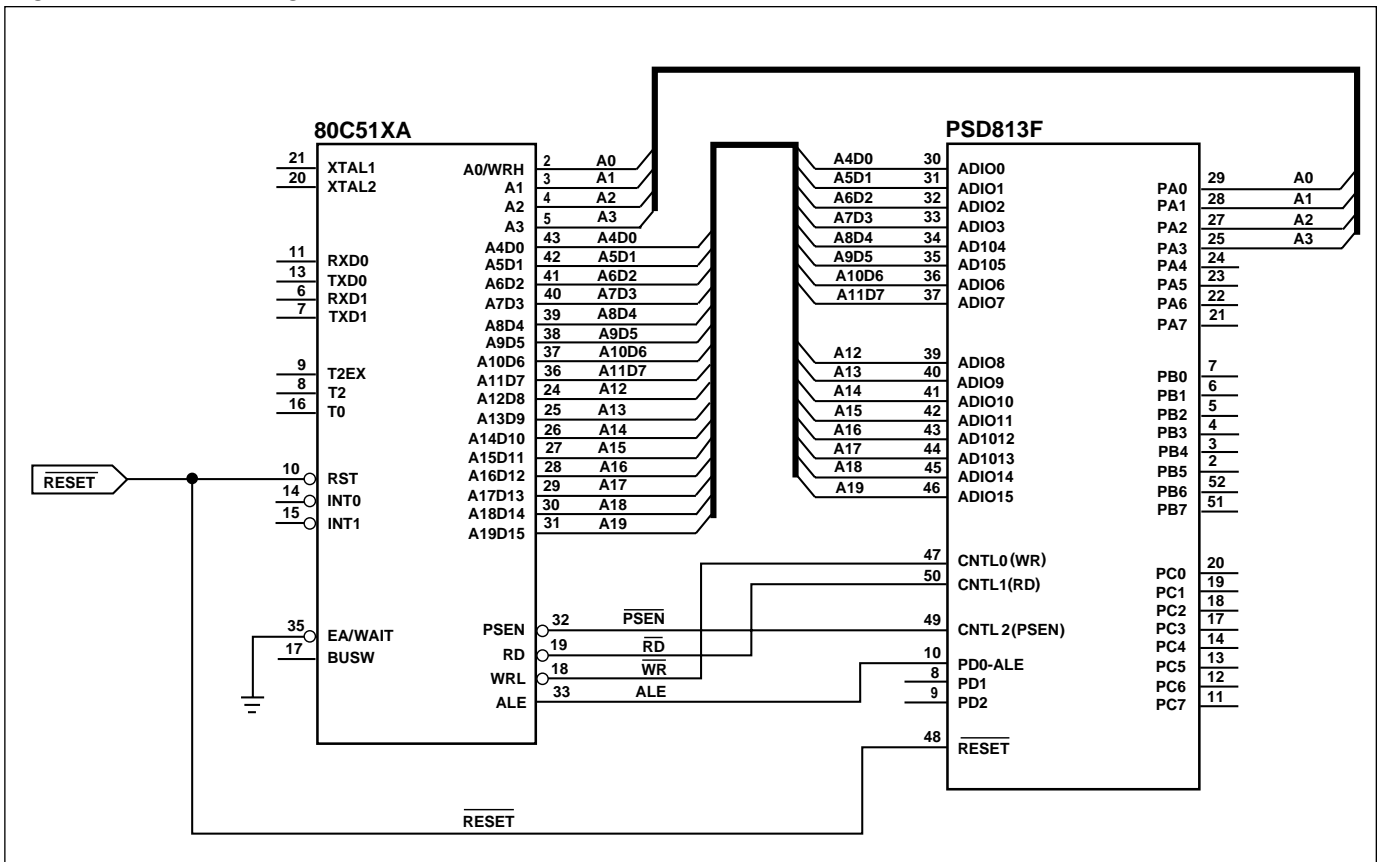
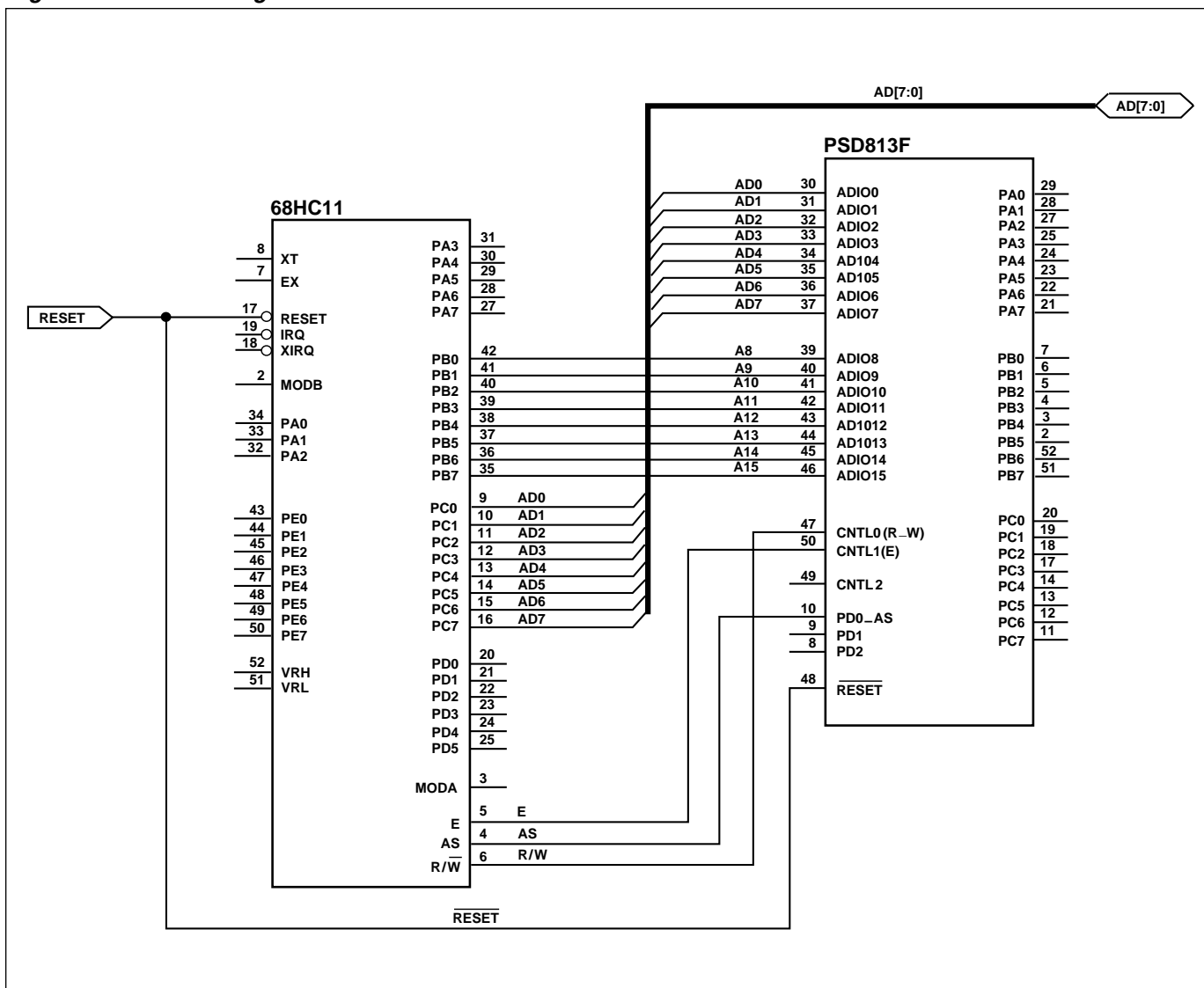


Figure 24. Interfacing the PSD813F with a 68HC11



**The
PSD813F
Functional
Blocks**
(cont.)

9.4 I/O Ports

There are four programmable I/O ports: Ports A, B, C, and D. Each of the ports is eight bits except Port D, which is 3 bits. Each port pin is individually user configurable, thus allowing multiple functions per port. The ports are configured using PSDsoft Configuration or by the microcontroller writing to on-chip registers in the CSIOP address space.

The topics discussed in this section are:

- General Port Architecture
- Port Operating Modes
- Port Configuration Registers
- Port Data Registers
- Individual Port Functionality.

9.4.1 General Port Architecture

The general architecture of the I/O Port is shown in Figure 25. Individual Port architectures are shown in Figures 27 through 30. In general, once the purpose for a port pin has been defined, that pin will no longer be available for other purposes. Exceptions will be noted.

As shown in Figure 25, the ports contain an output multiplexer whose selects are driven by the configuration bits in the Control Registers (Ports A and B only) and PSDsoft Configuration. Inputs to the multiplexer include the following:

- Output data from the Data Out Register
- Latched address outputs
- CPLD Micro \leftrightarrow Cell output
- External Chip Select from CPLD.

The Port Data Buffer (PDB) is a tri-state buffer that allows only one source at a time to be read. The PDB is connected to the Internal Data Bus for feedback and can be read by the microcontroller. The Data Out and Micro \leftrightarrow Cell outputs, Direction and Control Registers, and port pin input are all connected to the PDB.

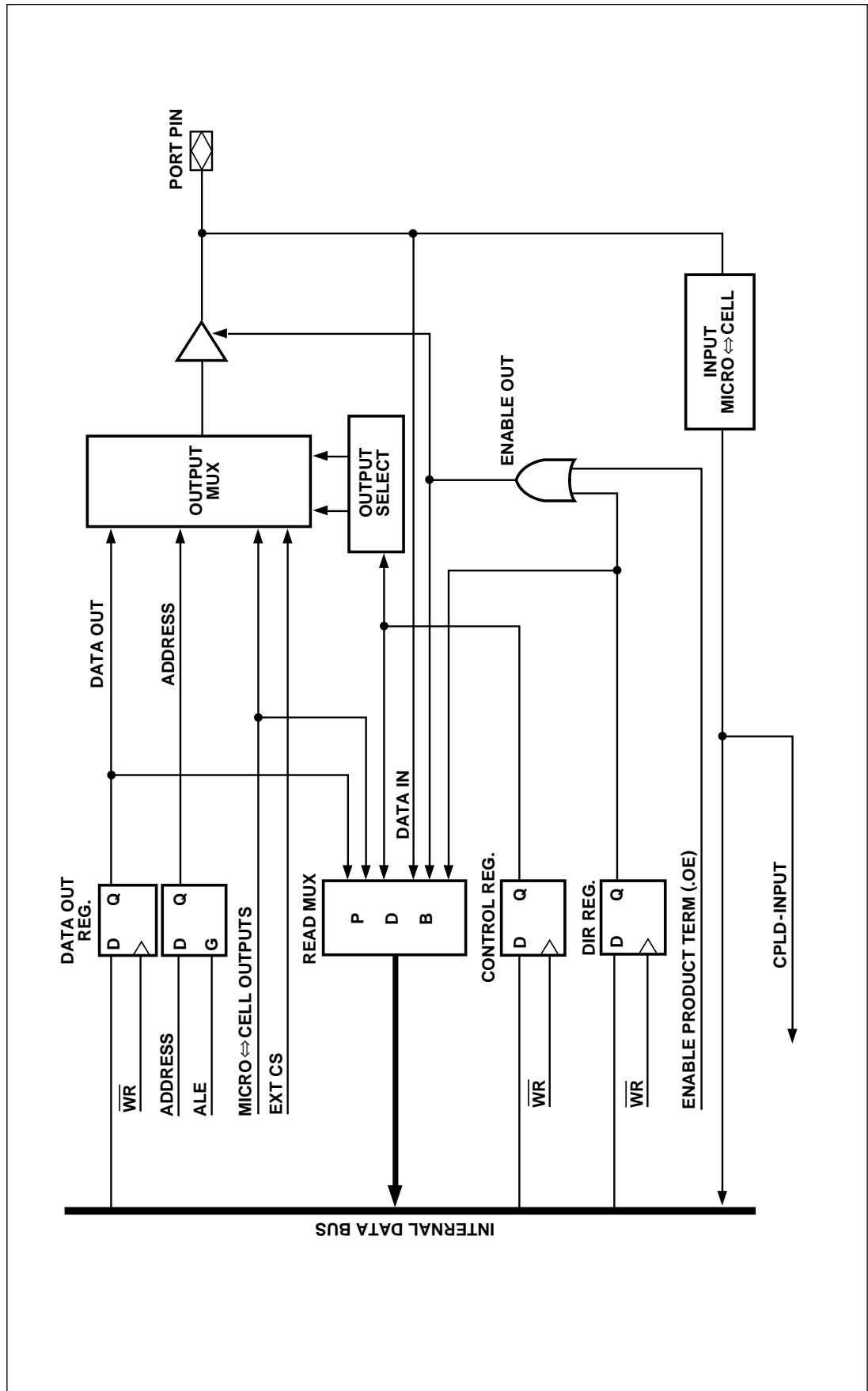
The Port pin's tri-state output driver enable is controlled by a two input OR gate whose inputs come from the CPLD AND array enable product term and the Direction Register. If the enable product term of any of the array outputs are not defined and that port pin is not defined as a CPLD output in the PSDabel file, then the Direction Register has sole control of the buffer that drives the port pin.

The contents of these registers can be altered by the microcontroller. The PDB feedback path allows the microcontroller to check the contents of the registers.

Ports A, B, and C have embedded Input Micro \leftrightarrow Cells (IMCs). The IMCs can be configured as latches, registers, or direct inputs to the PLDs. The latches and registers are clocked by the address strobe (AS/ALE) or a product term from the PLD AND array. The outputs from the IMCs drive the PLD input bus and can be read by the microcontroller. Refer to the IMC subsection of the PLD section.

The
PSD813F
Functional
Blocks
(cont.)

Figure 25. General I/O Port Architecture



**The
PSD813F
Functional
Blocks**
(cont.)

9.4.2 Port Operating Modes

The I/O Ports have several modes of operation. Some modes can be defined using PSDabel, some by the microcontroller writing to the Control Registers in CSIOP space, and some by both. The modes that can only be defined using PSDsoft must be programmed into the device and cannot be changed unless the device is reprogrammed. The modes that can be changed by the microcontroller can be done so dynamically at run-time. The PLD I/O, Data Port, Address Input, and Peripheral I/O modes are the only modes that must be defined before programming the device. All other modes can be changed by the microcontroller at run-time. See Application Note 55 for more detail.

Table 20 summarizes which modes are available on each port. Table 23 shows how and where the different modes are configured. Each of the port operating modes are described in the following subsections.

Table 20. Port Operating Modes

Port Mode	Port A	Port B	Port C	Port D
MCU I/O	Yes	Yes	Yes	Yes
PLD I/O				
McellAB Outputs	Yes	Yes	No	No
McellBC Outputs	No	Yes	Yes	No
Additional Ext. CS Outputs	No	No	No	Yes
PLD Inputs	Yes	Yes	Yes	Yes
Address Out	Yes (A7–0)	Yes (A7–0) or A15–8)	No	No
Address In	Yes	Yes	Yes	Yes
Data Port	Yes (D7–0)	No	No	No
Peripheral I/O	Yes	No	No	No
JTAG ISP	No	No	Yes*	No

*Can be multiplexed with other I/O functions.

**The
PSD813F
Functional
Blocks**
(cont.)

Table 21. Port Operating Mode Settings

Mode	Defined In PSDabel	Defined In PSDconfiguration	Control Register Setting	Direction Register Setting	VM Register Setting	JTAG Enable
MCU I/O	Declare pins only	NA*	0	1 = output, 0 = input (Note 1)	NA	NA
PLD I/O	Logic equations	NA	NA	(Note 1)	NA	NA
Data Port (Port A)	NA	Specify bus type	NA	NA	NA	NA
Address Out (Port A,B)	Declare pins only	NA	1	1 (Note 1)	NA	NA
Address In (Port A,B,C,D)	Logic equation for Input Micro \leftrightarrow Cells	NA	NA	NA	NA	NA
Peripheral I/O (Port A)	Logic equations (PSEL0 & 1)	NA	NA	NA	PIO bit = 1	NA
JTAG ISP (Note 2)	JTAGSEL	JTAG Configuration	NA	NA	NA	JTAG_Enabled

*NA = Not Applicable

NOTE: 1. The direction of the Port A,B,C, and D pins are controlled by the Direction Register ORed with the individual output enable product term (.oe) from the CPLD AND array.
2. Any of these three methods will enable JTAG pins on Port C.

9.4.2.1 MCU I/O Mode

In the MCU I/O Mode, the microcontroller uses the PSD813F ports to expand its own I/O ports. By setting up the CSIOP space, the ports on the PSD813F are mapped into the microcontroller address space. The addresses of the ports are listed in Table 7.

A port pin can be put into MCU I/O mode by writing a '0' to the corresponding bit in the Control Register. The MCU I/O direction may be changed by writing to the corresponding bit in the Direction Register, or by the output enable product term. See the subsection on the Direction Register in the "Port Registers" section. When the pin is configured as an output, the content of the Data Out Register drives the pin. When configured as an input, the microcontroller can read the port input through the Data In buffer. See Figure 25.

Ports C and D do not have Control Registers, and are in MCU I/O mode by default. They can be used for PLD I/O if equation are written for them in PSDabel.

9.4.2.2 PLD I/O Mode

The PLD I/O Mode uses a port as an input to the CPLD's Input Micro \leftrightarrow Cells, and/or as an output from the CPLD's Output Micro \leftrightarrow Cells. The output can be tri-stated with a control signal. This output enable control signal can be defined by a product term from the PLD, or by setting the corresponding bit in the Direction Register to '0'. The corresponding bit in the Direction Register must not be set to '1' if the pin is defined as a PLD input pin in PSDabel. The PLD I/O Mode is specified in PSDabel by declaring the port pins, and then writing an equation assigning the PLD I/O to a port.

**The
PSD813F
Functional
Blocks**
(cont.)

9.4.2.3 Address Out Mode

For microcontrollers with a multiplexed address/data bus, Address Out Mode can be used to drive latched addresses onto the port pins. These port pins can, in turn, drive external devices. Either the output enable or the corresponding bits of both the Direction Register and Control Register must be set to a '1' for pins to use Address Out Mode. This must be done by the MCU at run-time. See Table 22 for the address output pin assignments on Ports A and B for various MCUs.

For non-multiplexed 8 bit bus mode, address lines A[7:0] are available to Port B in Address Out Mode.

Note: do not drive address lines with Address Out Mode to an external memory device if it is intended for the MCU to boot from the external device. The MCU must first boot from PSD memory so the Direction and Control register bits can be set.

Table 22. I/O Port Latched Address Output Assignments

<i>Microcontroller</i>	<i>Port A (3:0)</i>	<i>Port A (7:4)</i>	<i>Port B (3:0)</i>	<i>Port B (7:4)</i>
8051XA (8-Bit)	N/A*	Address (7:4)	Address (11:8)	N/A
80C251 (Page Mode)	N/A	N/A	Address (11:8)	Address (15:12)
All Other 8-Bit Multiplexed	Address (3:0)	Address (7:4)	Address (3:0)	Address (7:4)
8-Bit Non-Multiplexed Bus	N/A	N/A	Address [3:0]	Address [7:4]

N/A = Not Applicable.

9.4.2.4 Address In Mode

For microcontrollers that have more than 16 address lines, the higher addresses can be connected to Port A, B, C, and D. The address input can be latched in the Input Micro \leftrightarrow Cell by the address strobe (ALE/AS). Any input that is included in the DPLD equations for the PLD's Flash, EEPROM, or SRAM is considered to be an address input.

9.4.2.5 Data Port Mode

Port A can be used as a data bus port for a microcontroller with a non-multiplexed address/data bus. The Data Port is connected to the data bus of the microcontroller. The general I/O functions are disabled in Port A if the port is configured as a Data Port.

9.4.2.6 Peripheral I/O Mode

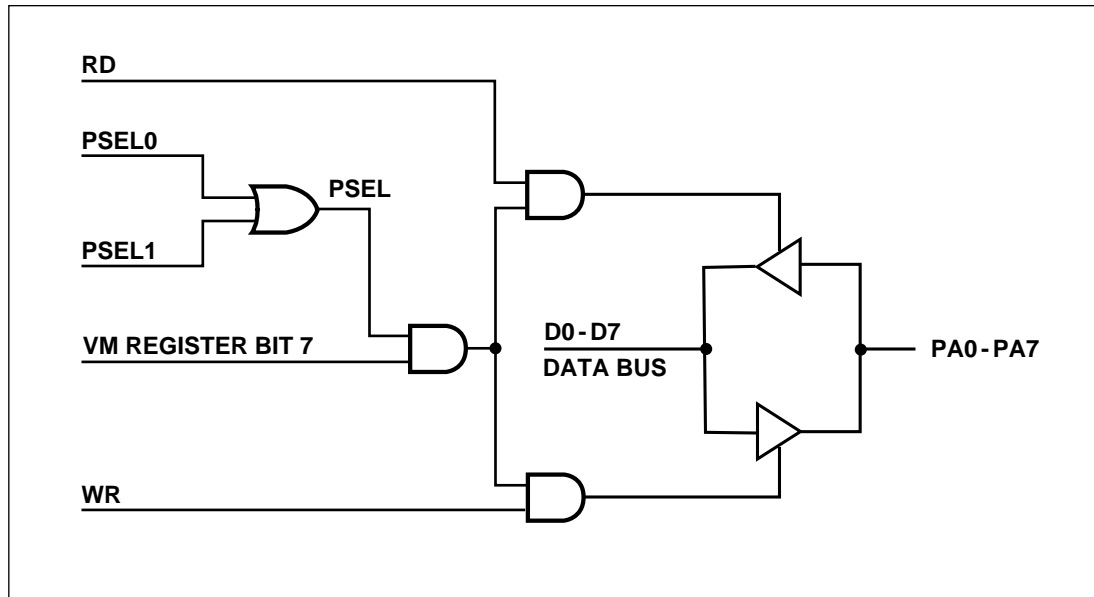
Peripheral I/O Mode can be used to interface with external peripherals. In this mode, all of Port A serves as a tri-stateable, bi-directional data buffer for the microcontroller. Peripheral I/O Mode is enabled by setting Bit 7 of the VM Register to a '1'. Figure 26 shows how Port A acts as a bi-directional buffer for the microcontroller data bus if Peripheral I/O Mode is enabled. An equation for PSEL0 and/or PSEL1 must be written in PSDlabel. The buffer is tri-stated when PSEL 0 or 1 is not active.

9.4.2.7 JTAG ISP

Port C is JTAG compliant, and can be used for In-System Programming (ISP). You can multiplex JTAG operations with other functions on Port C because ISP is not performed during normal system operation. For more information on the JTAG Port, refer to section 9.6.

**The
PSD813F
Functional
Blocks
(cont.)**

Figure 26. Peripheral I/O Mode



9.4.3 Port Configuration Registers (PCRs)

Each port has a set of PCRs used for configuration. The contents of the registers can be accessed by the microcontroller through normal read/write bus cycles at the addresses given in Table 7. The addresses in Table 7 are the offsets in hex from the base of the CSIOP register.

The pins of a port are individually configurable and each bit in the register controls its respective pin. For example, Bit 0 in a register refers to Bit 0 of its port. The three PCRs, shown in Table 23, are used for setting the port configurations. The default power-up state for each register in Table 23 is 00h.

Table 23. Port Configuration Registers

<i>Register Name</i>	<i>Port</i>	<i>MCU Access</i>
Control	A,B	Write/Read
Direction	A,B,C,D	Write/Read
Drive Select*	A,B,C,D	Write/Read

*NOTE: See Table 27 for Drive Register bit definition.



**The
PSD813F
Functional
Blocks**
(cont.)

9.4.3.1 Control Register

Any bit set to '0' in the Control Register sets the corresponding Port pin to MCU I/O Mode, and a '1' sets it to Address Out Mode. The default mode is MCU I/O. Only Ports A and B have an associated Control Register.

9.4.3.2 Direction Register

The Direction Register, in conjunction with the output enable (except for Port D), controls the direction of data flow in the I/O Ports. Any bit set to '1' in the Direction Register will cause the corresponding pin to be an output, and any bit set to '0' will cause it to be an input. The default mode for all port pins is input.

Figures 27 and 29 show the Port Architecture diagrams for Ports A/B and C, respectively. The direction of data flow for Ports A, B, and C are controlled not only by the direction register, but also by the output enable product term from the PLD AND array. If the output enable product term is not active, the Direction Register has sole control of a given pin's direction.

An example of a configuration for a port with the three least significant bits set to output and the remainder set to input is shown in Table 26. Since Port D only contains three pins, the Direction Register for Port D has only the three least significant bits active.

Table 24. Port Pin Direction Control, Output Enable P.T. Not Defined

<i>Direction Register Bit</i>	<i>Port Pin Mode</i>
0	Input
1	Output

Table 25. Port Pin Direction Control, Output Enable P.T. Defined

<i>Direction Register Bit</i>	<i>Output Enable P.T.</i>	<i>Port Pin Mode</i>
0	0	Input
0	1	Output
1	0	Output
1	1	Output

Table 26. Port Direction Assignment Example

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	1	1	1

The PSD813F Functional Blocks

(cont.)

9.4.3.3 Drive Select Register

The Drive Select Register configures the pin driver as Open Drain or CMOS for some port pins, and controls the slew rate for the other port pins. An external pull-up resistor should be used for pins configured as Open Drain.

A pin can be configured as Open Drain if its corresponding bit in the Drive Select Register is set to a '1'. The default pin drive is CMOS.

Aside: the slew rate is a measurement of the rise and fall times of an output. A higher slew rate means a faster output response and may create more electrical noise. A pin operates in a high slew rate when the corresponding bit in the Drive Register is set to '1'. The default rate is slow slew.

Table 27 shows the Drive Register for Ports A, B, C, and D. It summarizes which pins can be configured as Open Drain outputs and which pins the slew rate can be set for.

Table 27. Drive Register Pin Assignment

Drive Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port A	Open Drain	Open Drain	Open Drain	Open Drain	Slew Rate	Slew Rate	Slew Rate	Slew Rate
Port B	Open Drain	Open Drain	Open Drain	Open Drain	Slew Rate	Slew Rate	Slew Rate	Slew Rate
Port C	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain
Port D	NA	NA	NA	NA	NA	Slew Rate	Slew Rate	Slew Rate

NOTE: NA = Not Applicable.

**The
PSD813F
Functional
Blocks**
(cont.)

9.4.4 Port Data Registers

The Port Data Registers, shown in Table 28, are used by the microcontroller to write data to or read data from the ports. Table 28 shows the register name, the ports having each register type, and microcontroller access for each register type. The registers are described below.

9.4.4.1 Data In

Port pins are connected directly to the Data In buffer. In MCU I/O input mode, the pin input is read through the Data In buffer.

9.4.4.2 Data Out Register

Stores output data written by the MCU in the MCU I/O output mode. The contents of the Register are driven out to the pins if the Direction Register or the output enable product term is set to "1". The contents of the register can also be read back by the microcontroller.

9.4.4.3 Output Micro \leftrightarrow Cells (OMCs)

The CPLD OMCs occupy a location in the microcontroller's address space. The microcontroller can read the output of the OMCs. If the Mask Micro \leftrightarrow Cell Register bits are not set, writing to the Micro \leftrightarrow Cell loads data to the Micro \leftrightarrow Cell flip flops. Refer to the PLD section for more details.

9.4.4.4 Mask Micro \leftrightarrow Cell Register

Each Mask Register bit corresponds to an OMC flip flop. When the Mask Register bit is set to a "1", loading data into the OMC flip flop is blocked. The default value is "0" or unblocked.

9.4.4.5 Input Micro \leftrightarrow Cells (IMCs)

The IMCs can be used to latch or store external inputs. The outputs of the IMCs are routed to the PLD input bus, and can be read by the microcontroller. Refer to the PLD section for a detailed description.

9.4.4.6 Enable Out

The Enable Out register can be read by the microcontroller. It contains the output enable values for a given port. A "1" indicates the driver is in output mode. A "0" indicates the driver is in tri-state and the pin is in input mode.

Table 28. Port Data Registers

Register Name	Port	MCU Access
Data In	A,B,C,D	Read – input on pin
Data Out	A,B,C,D	Write/Read
Output Micro \leftrightarrow Cell	A,B,C	Read – outputs of Micro \leftrightarrow Cells Write – loading Micro \leftrightarrow Cells Flip-Flop
Mask Micro \leftrightarrow Cell	A,B,C	Write/Read – prevents loading into a given Micro \leftrightarrow Cell
Input Micro \leftrightarrow Cell	A,B,C	Read – outputs of the Input Micro \leftrightarrow Cells
Enable Out	A,B,C	Read – the output enable control of the port driver

**The
PSD813F
Functional
Blocks**
(cont.)

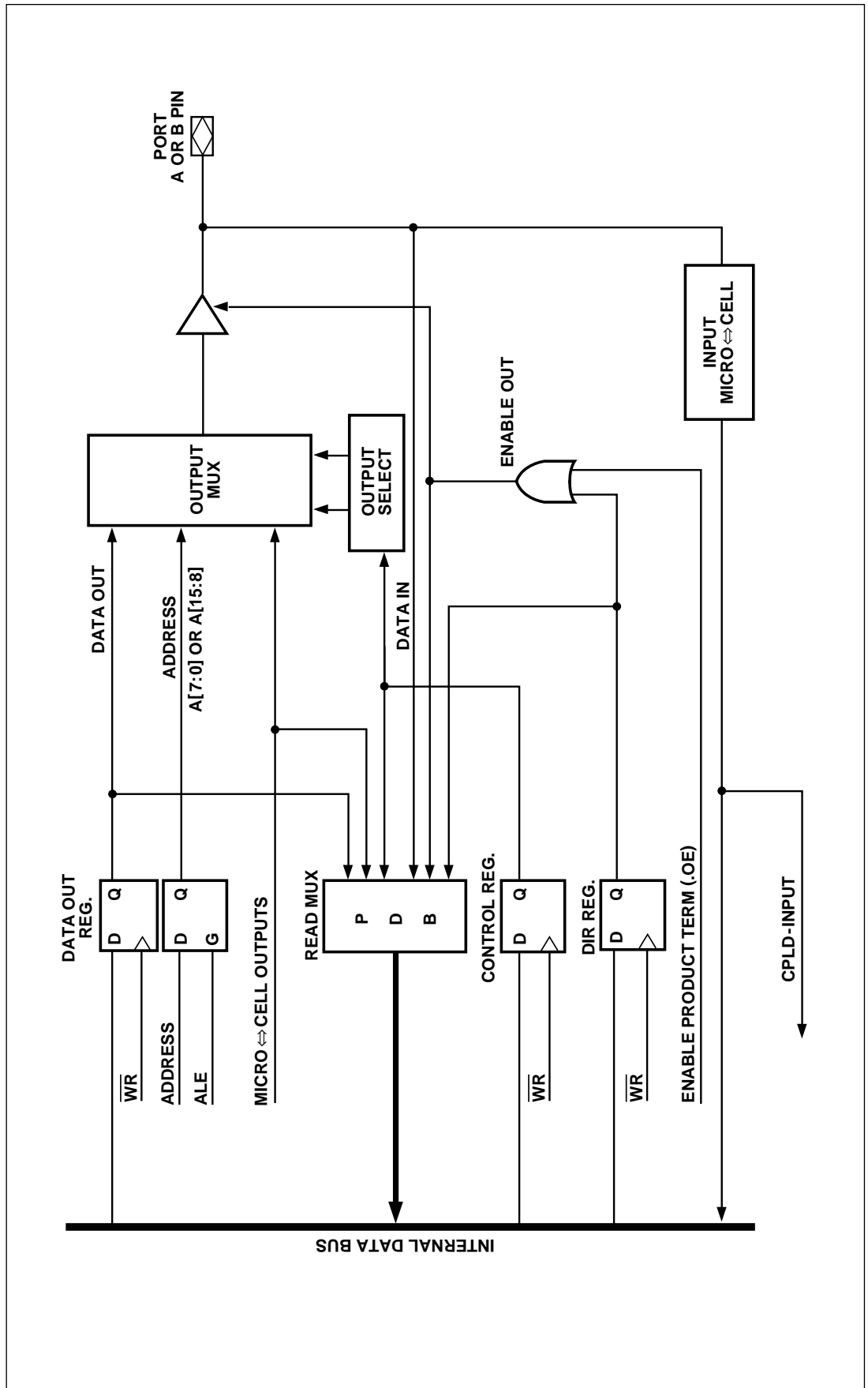
9.4.5 Ports A and B – Functionality and Structure

Ports A and B have similar functionality and structure, as shown in Figure 27. The two ports can be configured to perform one or more of the following functions:

- MCU I/O Mode
- CPLD Output – Micro \leftrightarrow Cells McellAB[7:0] can be connected to Port A or Port B. McellBC[7:0] can be connected to Port B or Port C.
- CPLD Input – Via the input Micro \leftrightarrow Cells.
- Latched Address output – Provide latched address output per Table 30.
- Address In – Additional high address inputs using the Input Micro \leftrightarrow Cells.
- Open Drain/Slew Rate – pins PA[3:0] and PB[3:0] can be configured to fast slew rate, pins PA[7:4] and PB[7:4] can be configured to Open Drain Mode.
- Data Port – Port A to D[7:0] for 8 bit non-multiplexed bus
- Multiplexed Address/Data port for certain types of microcontroller interfaces.
- Peripheral Mode – Port A only

The
PSD813F
Functional
Blocks
(cont.)

Figure 27. Ports A and B Structure



**The
PSD813F
Functional
Blocks**
(cont.)

9.4.6 Port C – Functionality and Structure

Port C can be configured to perform one or more of the following functions (see Figure 29):

- MCU I/O Mode
- CPLD Output – McellBC[7:0] outputs can be connected to Port B or Port C.
- CPLD Input – via the Input Micro↔Cells
- Address In – Additional high address inputs using the Input Micro↔Cells.
- In-System Programming – JTAG port can be enabled for programming/erase of the PSD813F device. (See Section 9.6 for more information on JTAG programming.)
- Open Drain – Port C pins can be configured in Open Drain Mode
- Battery Backup features – PC2 can be configured as a Battery Input (Vstby) pin.
PC4 can be configured as a Battery On Indicator output pin, indicating when Vcc is less than Vbat.

Port C does not support Address Out mode, and therefore no Control Register is required. Pin PC7 may be configured as the DBE input in certain microcontroller interfaces.

9.4.7 Port D – Functionality and Structure

Port D has three I/O pins. See Figure 30. This port does not support Address Out mode, and therefore no Control Register is required. Port D can be configured to perform one or more of the following functions:

- MCU I/O Mode
- CPLD Output – (external chip select)
- CPLD Input – direct input to CPLD, no Input Micro↔Cells
- Slew rate – pins can be set up for fast slew rate

Port D pins can be configured in PSDsoft as input pins for other dedicated functions:

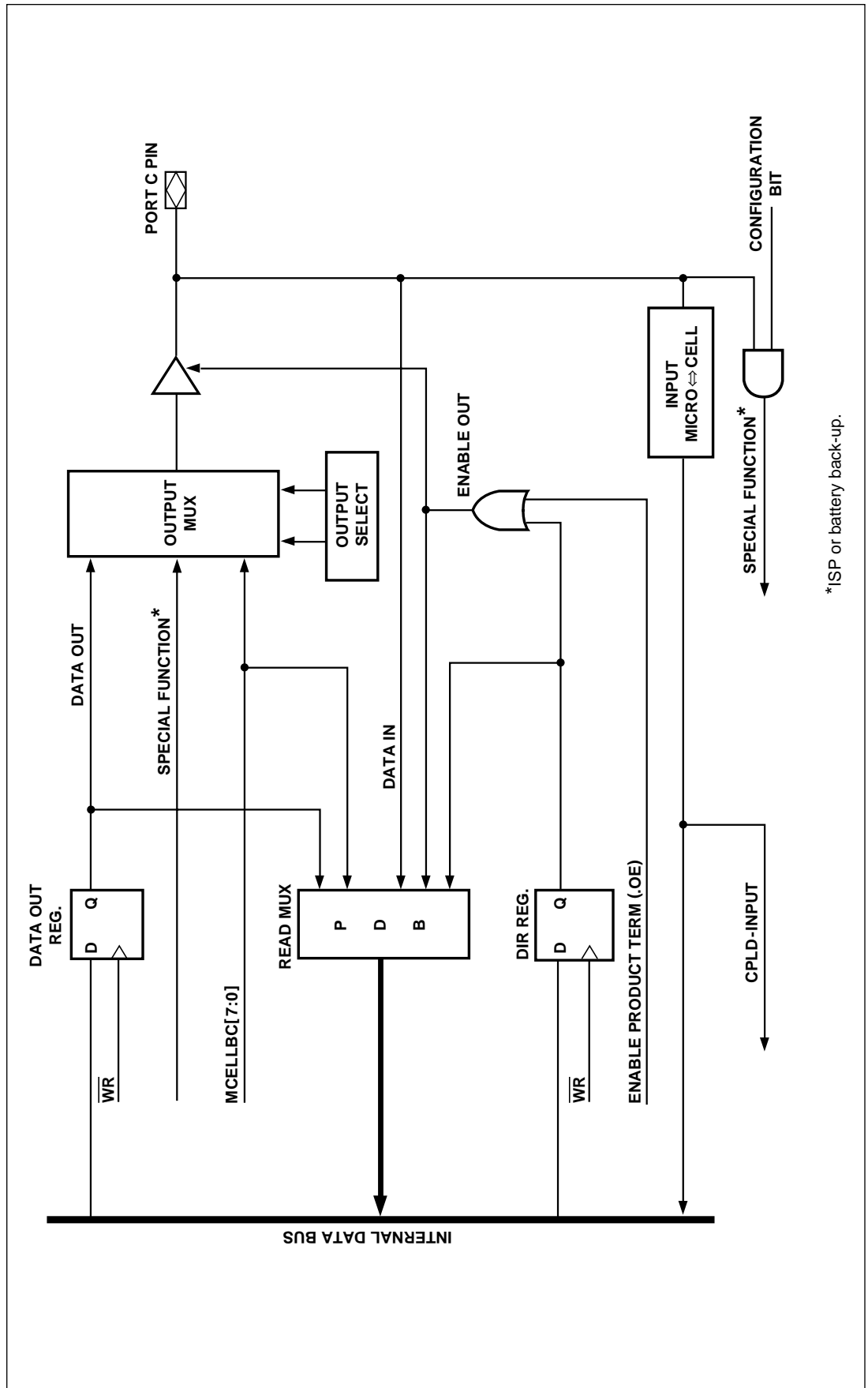
- PD0 – ALE, as address strobe input
- PD1 – CLKIN, as clock input to the Micro↔Cells Flip Flops and APD counter
- PD2 – CSI, as active low chip select input. A high input will disable the Flash/EEPROM/SRAM and CSIOP.

9.4.7.1 External Chip Select

The CPLD also provides three chip select outputs on Port D pins that can be used to select external devices. Each chip select (ECS0-2) consists of one product term that can be configured active high or low. The output enable of the pin is controlled by either the output enable product term or the Direction Register. (See Figure 30.)

The
PSD813F
Functional
Blocks
(cont.)

Figure 28. Port C Structure

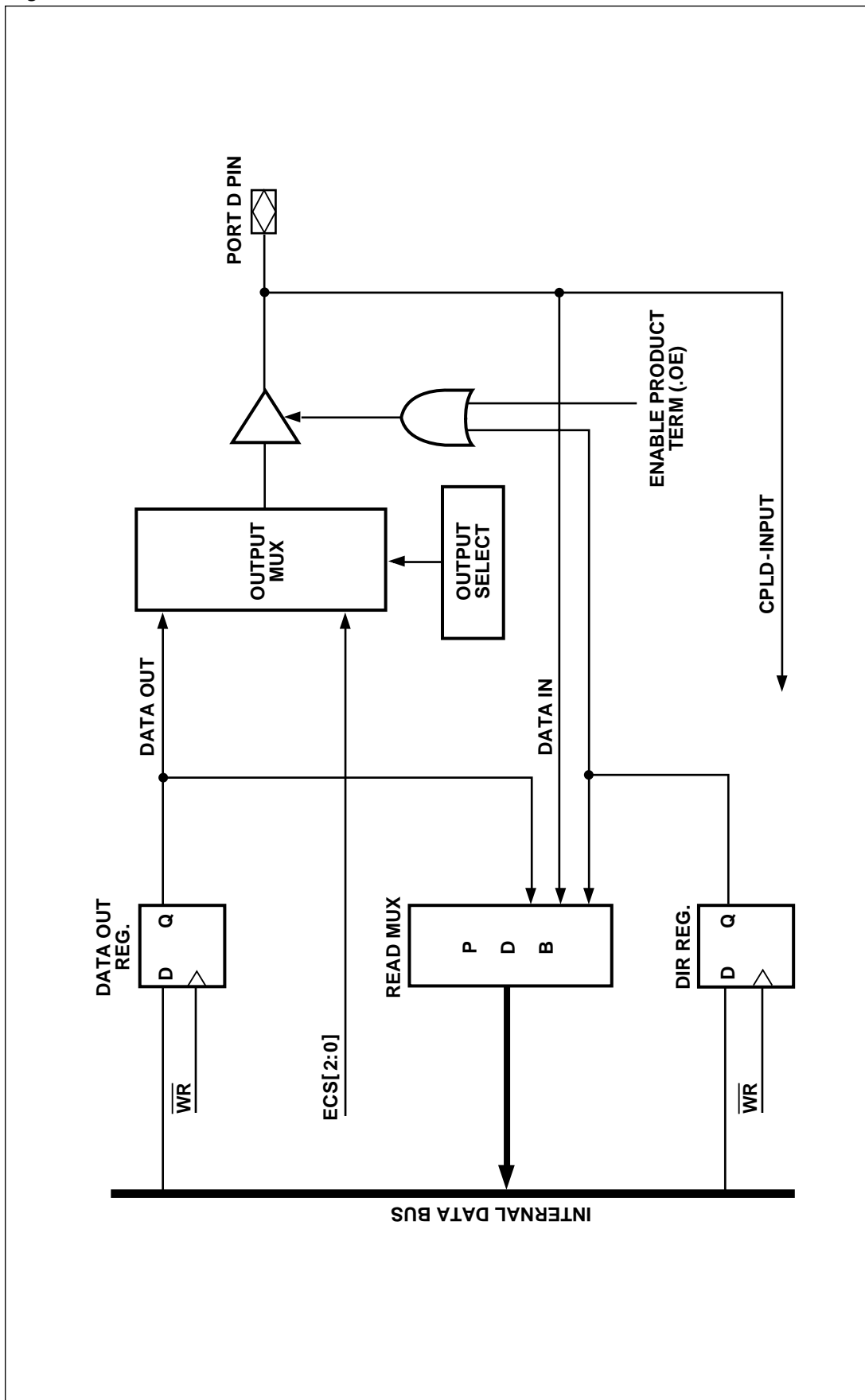


*ISP or battery back-up.



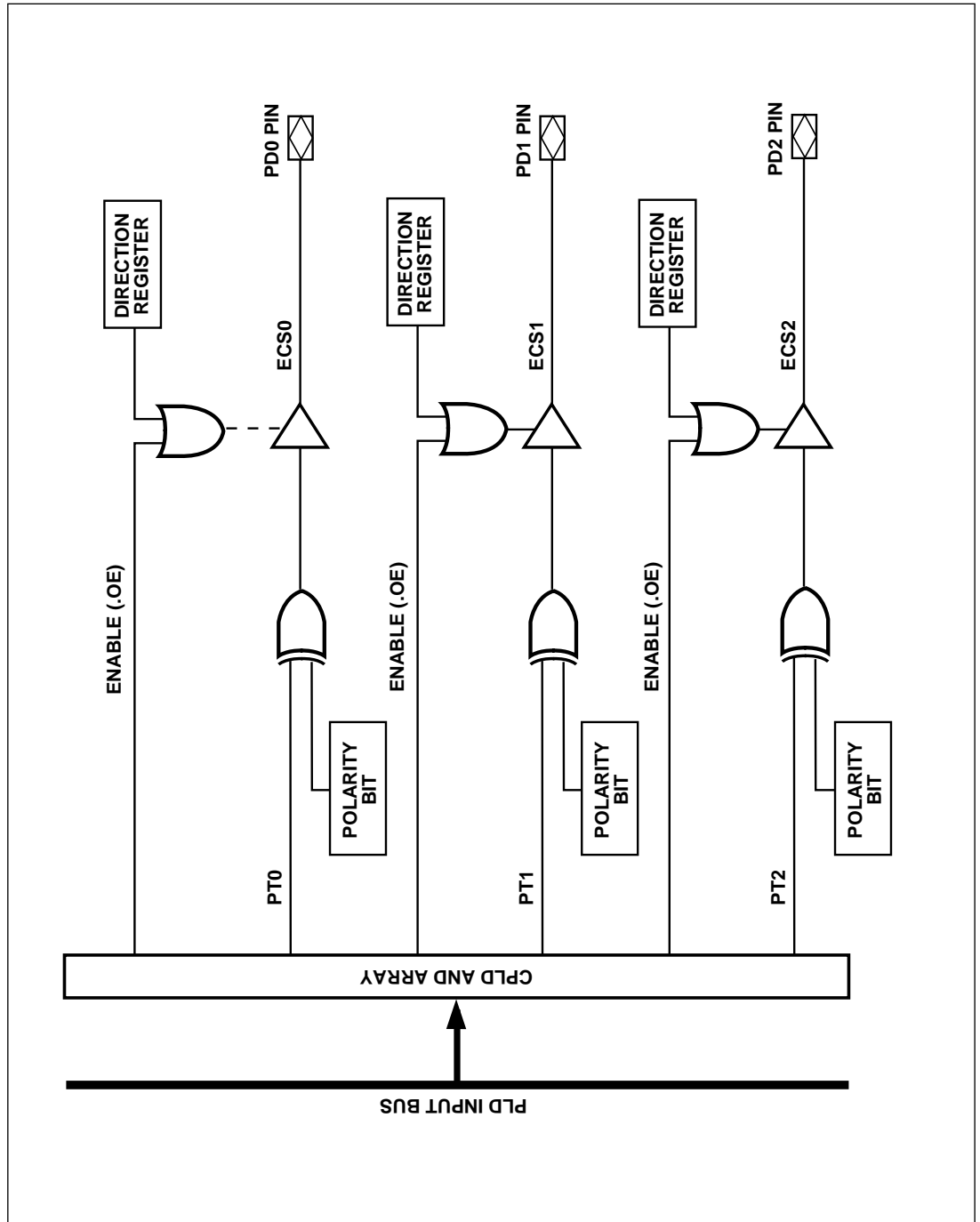
The PSD813F Functional Blocks (cont.)

Figure 29. Port D Structure



The
PSD813F
Functional
Blocks
(cont.)

Figure 30. Port D External Chip Selects



**The
PSD813F
Functional
Blocks**
(cont.)

9.5 Power Management

All three device families, the PSD813F, ZPSD813F, and ZPSD813FV offer configurable power saving options. These options may be used individually or in combinations, as follows:

- All memory types in a PSD (Flash, EEPROM, and SRAM) are built with Zero-Power technology. In addition to using special silicon design methodology, Zero-Power technology puts the memories into standby mode when address/data inputs are not changing (zero DC current). As soon as a transition occurs on an input, the affected memory “wakes up”, changes and latches its outputs, then goes back to standby. The designer does **not** have to do anything special to achieve memory standby mode when no inputs are changing—it happens automatically.

When using ZPSD family devices, the PLD sections can also achieve standby mode when its inputs are not changing.

- Like the Zero-Power feature, the Automatic Power Down (APD) logic allows the PSD to reduce to standby current automatically. The APD will block MCU address/data signals from reaching the memories and PLDs. This feature is available on all three PSD813F families. The APD unit is described in more detail in section 9.5.1.

Built in logic will monitor the address strobe of the MCU for activity. If there is no activity for a certain time period (MCU is asleep), the APD logic initiates Power Down Mode (if enabled). Once in Power Down Mode, all address/data signals are blocked from reaching PSD memories and PLDs, and the memories are deselected internally. This allows the memories and PLDs to remain in standby mode even if the address/data lines are changing state externally (noise, other devices on the MCU bus, etc.). Keep in mind that any unblocked PLD input signals that are changing states keeps the PLD out of standby mode, but not the memories.

- The PSD Chip Select Input (CSI) on all families can be used to disable the internal memories, placing them in standby mode even if inputs are changing. This feature does not block any internal signals or disable the PLDs. This is a good alternative to using the APD logic, especially if your MCU has a chip select output. There is a slight penalty in memory access time when the CSI signal makes its initial transition from deselected to selected.
- The PMMR registers can be written by the MCU at run-time to manage power. All three families support “blocking bits” in these registers that are set to block designated signals from reaching both PLDs. Current consumption of the PLDs is directly related to the composite frequency of the changes on their inputs (see Figures 34 and 34a). Significant power savings can be achieved by blocking signals that are not used in DPLD or CPLD logic equations.

Unique to the ZPSD813F and ZPSD813FV families is the Turbo Bit in the PMMR0 register. This bit can be set to disable the Turbo Mode feature (default is Turbo Mode on). While Turbo Mode is disabled, the PLDs can achieve standby current when no PLD inputs are changing (zero DC current). Even when inputs do change, significant power can be saved at lower frequencies (AC current), compared to when Turbo Mode is enabled. When the Turbo Mode is enabled, there is a significant DC current component and the AC component is higher.

9.5.1 Automatic Power Down (APD) Unit and Power Down Mode

The APD Unit, shown in Figure 31, puts the PSD into Power Down Mode by monitoring the activity of the address strobe (ALE/AS). If the APD unit is enabled, as soon as activity on the address strobe stops, a four bit counter starts counting. If the address strobe remains inactive for fifteen clock periods of the CLKIN signal, the Power Down (PDN) signal becomes active, and the PSD will enter into Power Down Mode, discussed next.

**The
PSD813F
Functional
Blocks
(cont.)**

9.5.1 Automatic Power Down (APD) Unit and Power Down Mode (cont.)

Power Down Mode

By default, if you enable the PSD APD unit, Power Down Mode is automatically enabled. The device will enter Power Down Mode if the address strobe (ALE/AS) remains inactive for fifteen CLKIN (pin PD1) clock periods.

The following should be kept in mind when the PSD is in Power Down Mode:

- If the address strobe starts pulsing again, the PSD will return to normal operation. The PSD will also return to normal operation if either the CSI input returns low or the Reset input returns high.
- The MCU address/data bus is blocked from all memories and PLDs.
- Various signals can be blocked (prior to Power Down Mode) from entering the PLDs by setting the appropriate bits in the PMMR registers. The blocked signals include MCU control signals and the common clock (CLKIN). Note that blocking CLKIN from the PLDs will not block CLKIN from the APD unit.
- All PSD memories enter Standby Mode and are drawing standby current. However, the PLDs and I/O ports do **not** go into Standby Mode because you don't want to have to wait for the logic and I/O to "wake-up" before their outputs can change. See table 29 for Power Down Mode effects on PSD ports.
- Typical standby current is 50 μ A for 5 V devices, and 25 μ A for 3 V devices. These standby current values assume that there are no transitions on any PLD input.

Table 29. Power Down Mode's Effect on Ports

<i>Port Function</i>	<i>Pin Level</i>
MCU I/O	No Change
PLD Out	No Change
Address Out	Undefined
Data Port	Three-State
Peripheral I/O	Three-State

Table 30. PSD813F Timing and Standby Current During Power Down Mode

<i>Mode</i>	<i>PLD Propagation Delay</i>	<i>Memory Access Time</i>	<i>Access Recovery Time to Normal Access</i>	<i>5V V_{CC}, Typical Standby Current</i>
Power Down	Normal tpd (Note 1)	No Access	tLVDV	50 μ A (Note 2)

- NOTES:**
1. Power Down does not affect the operation of the PLD. The PLD operation in this mode is based only on the Turbo Bit.
 2. Typical current consumption assuming no PLD inputs are changing state and the PLD Turbo bit is off.

HC11 (or compatible) Users Note

The HC11 turns off its E clock when it sleeps. Therefore, if you are using an HC11 (or compatible) in your design, and you wish to use the Power Down, you must not connect the E clock to the CLKIN input (PD1). You should instead connect an independent clock signal to the CLKIN input. The clock frequency must be **less than** 15 times the frequency of AS. The reason for this is that if the frequency is greater than 15 times the frequency of AS, the PSD813F will keep going into Power Down Mode.



The PSD813F Functional Blocks (cont.)

Figure 31. APD Logic Block

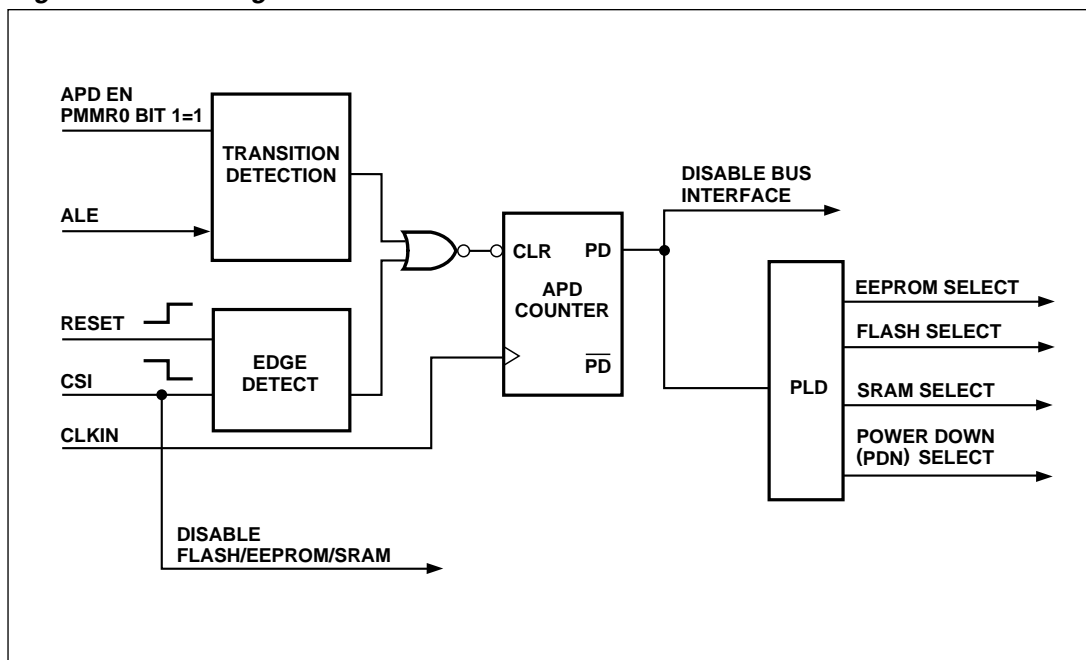
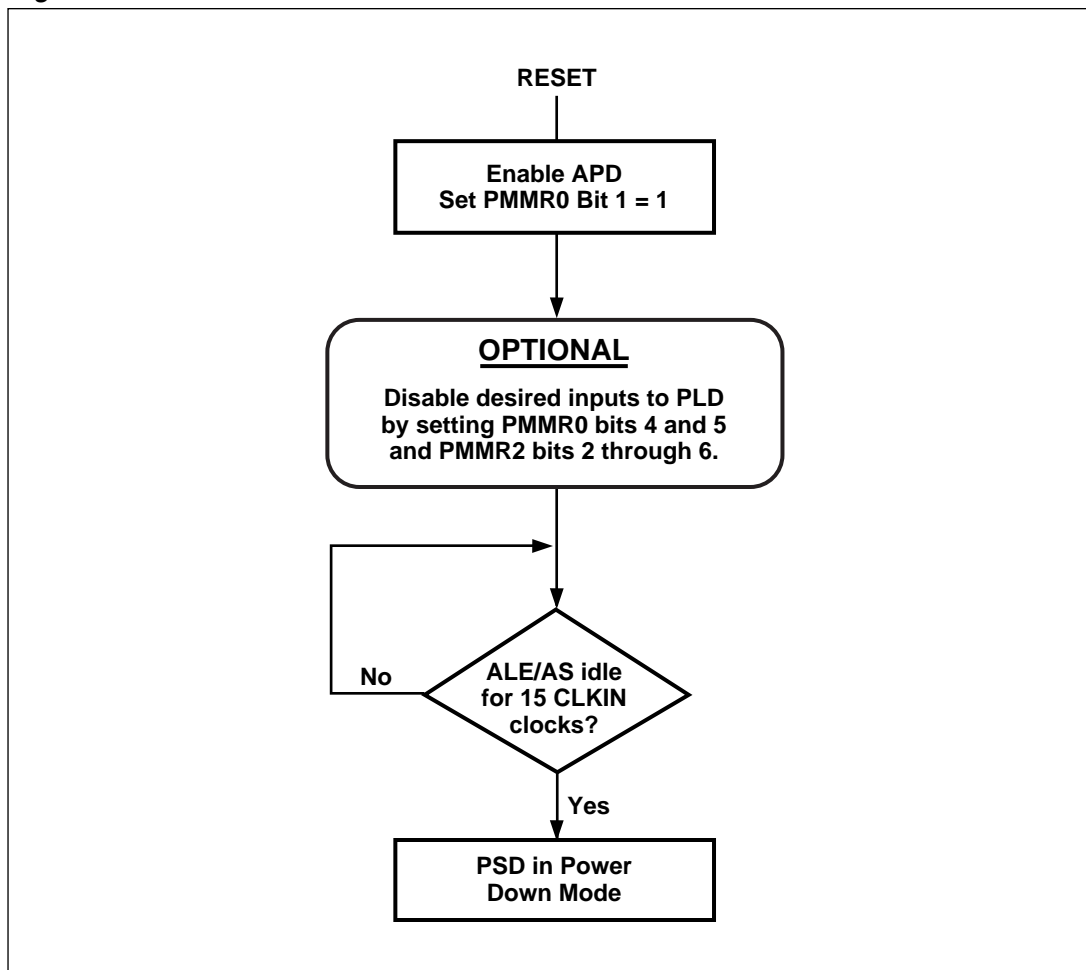


Figure 32. Enable Power Down Flow Chart



**The
PSD813F
Functional
Blocks
(cont.)**

Table 31. Power Management Mode Registers (PMMR0, PMMR2)**

PMMR0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
*	*	PLD Mcell clk	PLD Array clk	PLD Turbo***	X	APD Enable	X
		1 = off	1 = off	1 = off		1 = on	

*Bits 0, 2, 6, and 7 are not used, and should be set to 0.

**The PMMR0, and PMMR2 register bits are cleared to zero following power up. Subsequent reset pulses will not clear the registers.

***ZPSD813F and ZPSD813FV only.

- Bit 1 0 = Automatic Power Down (APD) is disabled.
1 = Automatic Power Down (APD) is enabled.
- Bit 3 0 = PLD Turbo is on. Available in ZPSD813F only.
1 = PLD Turbo is off, saving power.
- Bit 4 0 = CLKIN input to the PLD AND array is connected.
Every CLKIN change will power up the PLD when Turbo bit is off.
1 = CLKIN input to PLD AND array is disconnected, saving power.
- Bit 5 0 = CLKIN input to the PLD Micro⇔Cells is connected.
1 = CLKIN input to PLD Micro⇔Cells is disconnected, saving power.

PMMR2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
*	PLD array DBE	PLD array ALE	PLD array CNTL2	PLD array CNTL1	PLD array CNTL0	*	*
	1 = off	1 = off	1 = off	1 = off	1 = off		

*Unused bits should be set to 0.

- Bit 2 0 = Cntl0 input to the PLD AND array is connected.
1 = Cntl0 input to PLD AND array is disconnected, saving power.
- Bit 3 0 = Cntl1 input to the PLD AND array is connected.
1 = Cntl1 input to PLD AND array is disconnected, saving power.
- Bit 4 0 = Cntl2 input to the PLD AND array is connected.
1 = Cntl2 input to PLD AND array is disconnected, saving power.
- Bit 5 0 = ALE input to the PLD AND array is connected.
1 = ALE input to PLD AND array is disconnected, saving power.
- Bit 6 0 = DBE input to the PLD AND array is connected.
1 = DBE input to PLD AND array is disconnected, saving power.



**The
PSD813F
Functional
Blocks
(cont.)**

Table 32. APD Counter Operation

APD Enable Bit	ALE PD Polarity	ALE Level	APD Counter
0	X	X	Not Counting
1	X	Pulsing	Not Counting
1	1	1	Counting (Generates PDN after 15 Clocks)
1	0	0	Counting (Generates PDN after 15 Clocks)

9.5.2 Other Power Saving Options

The PSD813F offers other reduced power saving options that are independent of the Power Down Mode. Except for the SRAM Standby and CSI input features, they are enabled by setting bits in the PMMR0 and PMMR2 registers.

9.5.2.1 Zero Power PLD (ZPSD813F)

The power and speed of the PLDs are controlled by the Turbo bit (bit 3) in the PMMR0. By setting the bit to “1”, the Turbo mode is disabled and the PLDs consume Zero Power current when the inputs are not switching for an extended time of 70 ns. The propagation delay time will be increased by 10 ns after the Turbo bit is set to “1” (turned off) when the inputs change at a composite frequency of less than 15 MHz. When the Turbo bit is set to a “0” (turned on), the PLDs run at full power and speed. The Turbo bit affects the PLD’s D.C. power, AC power, and propagation delay.

Note: Blocking MCU control signals with PMMR2 bits can further reduce PLD AC power consumption.

9.5.2.2 SRAM Standby Mode (Battery Backup)

The PSD813F supports a battery backup operation that retains the contents of the SRAM in the event of a power loss. The SRAM has a Vstby pin (PC2) that can be connected to an external battery. When V_{CC} becomes lower than Vstby then the PSD will automatically connect to Vstby as a power source to the SRAM. The SRAM Standby Current (Istby) is typically 0.5 µA. The SRAM data retention voltage is 2 V minimum. The battery-on indicator (Vbaton) can be routed to PC4. This signal indicates when the V_{CC} has dropped below the Vstby voltage.

9.5.2.3 The CSI Input

Pin PD2 of Port D can be configured in PSDsoft as the CSI input. When low, the signal selects and enables the internal Flash, EEPROM, SRAM, and I/O for read or write operations involving the PSD813F. A high on the CSI pin will disable the Flash memory, EEPROM, and SRAM, and reduce the PSD power consumption. However, the PLD and I/O pins remain operational when CSI is high. **Note:** there may be a timing penalty when using the CSI pin depending on the speed grade of the PSD that you are using. See the timing parameter t_{SLQV} in the AC/DC specs.

9.5.2.4 Input Clock

The PSD813F provides the option to turn off the CLKIN input to the PLD to save AC power consumption. The CLKIN is an input to the PLD AND array and the Output Micro↔Cells. During Power Down Mode, or, if the CLKIN input is not being used as part of the PLD logic equation, the clock should be disabled to save AC power. The CLKIN will be disconnected from the PLD AND array or the Micro↔Cells by setting bits 4 or 5 to a “1” in PMMR0.

9.5.2.5 Input Control Signals

The PSD813F provides the option to turn off the input control signals (CNTL0-2, ALE, and DBE) to the PLD to save AC power consumption. These control signals are inputs to the PLD AND array. During Power Down Mode, or, if any of them are not being used as part of the PLD logic equation, these control signals should be disabled to save AC power. They will be disconnected from the PLD AND array by setting bits 2, 3, 4, 5, and 6 to a “1” in the PMMR2.

**The
PSD813F
Functional
Blocks
(cont.)**

9.5.3 Reset and Power On Requirement

Power On Reset

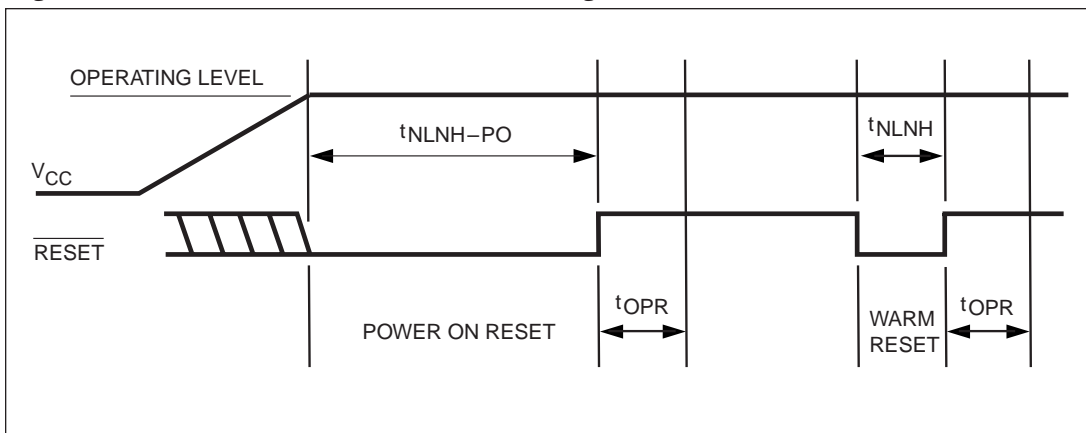
Upon power up the PSD813F requires a reset pulse of $t_{NLNH-PO}$ (minimum 1ms) after V_{CC} is steady. During this time period the device loads internal configurations, clears some of the registers and sets the Flash or EEPROM into operating mode. After the rising edge of reset, the PSD813F remains in the reset state for an additional t_{OPR} (minimum 120 ns) nanoseconds before the first memory access is allowed.

The PSD813F Flash or EEPROM memory is reset to the read array mode upon power up. The FS_i and $CSBOOT_i$ select signals along with the write strobe signal must be in the false state during power-up reset for maximum security of the data contents and to remove the possibility of a byte being written on the first edge of a write strobe signal. The PSD automatically prevents write strobes from reaching the EEPROM memory array for about 5 ms (t_{EEHWL}). Any Flash memory write cycle initiation is prevented automatically when V_{CC} is below V_{LKO} .

Warm Reset

Once the device is up and running, the device can be reset with a much shorter pulse of t_{NLNH} (minimum 150 ns). The same t_{OPR} time is needed before the device is operational after warm reset. Figure 33 shows the timing of the power on and warm reset.

Figure 33. Power On and Warm Reset Timing



I/O Pin, Register and PLD Status at Reset

Table 33 shows the I/O pin, register and PLD status during power on reset, warm reset and power down mode. PLD outputs are always valid during warm reset, and they are valid in power on reset once the internal PSD configuration bits are loaded. This loading of PSD is completed typically long before the V_{CC} ramps up to operating level. Once the PLD is active, the state of the outputs are determined by the PSD_{label} equations.

**The
PSD813F
Functional
Blocks
(cont.)**

Table 33. Status During Power On Reset, Warm Reset and Power Down Mode

Port Configuration	Power On Reset	Warm Reset	Power Down Mode
MCU I/O	Input Mode	Input Mode	Unchanged
PLD Output	Valid after internal PSD configuration bits are loaded	Valid	Depend on inputs to PLD (address are blocked in PD mode)
Address Out	Tri-stated	Tri-stated	Not defined
Data Port	Tri-stated	Tri-stated	Tri-stated
Peripheral I/O	Tri-stated	Tri-stated	Tri-stated

Register	Power On Reset	Warm Reset	Power Down Mode
PMMR0, 2	Cleared to "0"	Unchanged	Unchanged
Micro↔Cells Flip Flop status	Cleared to "0" by internal power on reset	Depend on .re and .pr equations	Depend on .re and .pr equations
VM Register*	Initialized based on the selection in PSDsoft Configuration Menu.	Initialized based on the selection in PSDsoft Configuration Menu	Unchanged
All other registers	Cleared to "0"	Cleared to "0"	Unchanged

*SR_cod and Periph Mode bits in the VM Register are always cleared to zero on power on or warm reset.

9.6 Programming In-Circuit using the JTAG Interface

The JTAG interface on the PSD813F can be enabled on Port C (see Table 34). All memory (Flash and EEPROM), PLD logic, and PSD configuration bits may be programmed through the JTAG interface. A blank part can be mounted on a printed circuit board and programmed using JTAG.

The standard JTAG signals (IEEE 1149.1) are TMS, TCK, TDI, and TDO. Two additional signals, $\overline{\text{TSTAT}}$ and $\overline{\text{TERR}}$, are optional JTAG extensions used to speed up program and erase operations.

By default, on a blank PSD (as shipped from factory or after erasure), four pins on Port C are enabled for the basic JTAG signals TMS, TCK, TDI, and TDO.

See WSI Application Note 54 for more details on JTAG In-System-Programming.

Table 34. JTAG Port Signals

Port C Pin	JTAG Signals	Description
PC0	TMS	Mode Select
PC1	TCK	Clock
PC3	$\overline{\text{TSTAT}}$	Status
PC4	$\overline{\text{TERR}}$	Error Flag
PC5	TDI	Serial Data In
PC6	TDO	Serial Data Out

**The
PSD813F
Functional
Blocks
(cont.)**

9.6.1 Standard JTAG Signals

The standard JTAG signals (TMS, TCK, TDI, and TDO) can be enabled by any of three different conditions that are logically ORed. When enabled, TDI, TDO, TCK, and TMS are inputs, waiting for a serial command from an external JTAG controller device (such as FlashLink or Automated Test Equipment). When the enabling command is received from the external JTAG controller, TDO becomes an output and the JTAG channel is fully functional inside the PSD. The same command that enables the JTAG channel may optionally enable the two additional JTAG pins, TSTAT and TERR.

The following symbolic logic equation specifies the conditions enabling the four basic JTAG pins (TMS, TCK, TDI, and TDO) on their respective Port C pins. For purposes of discussion, the logic label JTAG_ON will be used. When JTAG_ON is true, the four pins are enabled for JTAG. When JTAG_ON is false, the four pins can be used for general PSD I/O.

```
JTAG_ON = PSDsoft_enabled +
          /* An NVM configuration bit inside the PSD is set by the designer
           in the PSDsoft Configuration utility. This dedicates the pins for
           JTAG at all times (compliant with IEEE 1149.1) */

          Microcontroller_enabled +
          /* The microcontroller can set a bit at run-time by writing to the
           PSD register, JTAG Enable. This register is located at address
           CSIOP + offset C7h. Setting the JTAG_ENABLE bit in this
           register will enable the pins for JTAG use. This bit is cleared
           by a PSD reset or the microcontroller. See Table 35 for bit
           definition. */

          PSD_product_term_enabled;
          /* A dedicated product term (PT) inside the PSD can be used to
           enable the JTAG pins. This PT has the reserved name
           JTAGSEL. Once defined as a node in PSDlabel, the designer
           can write an equation for JTAGSEL. This method is used when
           the Port C JTAG pins are multiplexed with other I/O signals.
           It is recommended to logically tie the node JTAGSEL to the
           JEN\ signal on the Flashlink cable when multiplexing JTAG
           signals. See Application Note 54 for details.
```

Table 35. JTAG Enable Register
JTAG Enable

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
*	*	*	*	*	*	*	JTAG_ENABLE

*Bits 1-7 are not used and should set to 0.

Bit definitions:

JTAG_ENABLE 1 = JTAG Port is Enabled.
0 = JTAG Port is Disabled.



**The
PSD813F
Functional
Blocks**
(cont.)

9.6.1 Standard JTAG Signals (cont.)

The PSD813F supports JTAG In-System-Configuration (ISC) commands, but not Boundary Scan. A definition of these JTAG-ISC commands and sequences are defined in a supplemental document available from WSI. WSI's PSDsoft software tool and FlashLink JTAG programming cable implement these JTAG-ISC commands. This document is needed only as a reference for designers who use a FlashLink to program their PSD813F.

9.6.2 JTAG Extensions

$\overline{\text{TSTAT}}$ and $\overline{\text{TERR}}$ are two JTAG extension signals enabled by an "ISC_ENABLE" command received over the four standard JTAG pins (TMS, TCK, TDI, and TDO). They are used to speed programming and erase functions by indicating status on PSD pins instead of having to scan the status out serially using the standard JTAG channel. See Application Note 54.

$\overline{\text{TERR}}$ will indicate if an error has occurred when erasing a sector or programming a byte in Flash memory. This signal will go low (active) when an error condition occurs, and stay low until an "ISC_CLEAR" command is executed or a chip reset pulse is received after an "ISC-DISABLE" command. $\overline{\text{TERR}}$ does not apply to EEPROM.

$\overline{\text{TSTAT}}$ behaves the same as the Rdy/Bsy signal described in section 9.1.1.2. $\overline{\text{TSTAT}}$ will be high when the PSD813F device is in read array mode (Flash memory and EEPROM contents can be read). $\overline{\text{TSTAT}}$ will be low when Flash memory programming or erase cycles are in progress, and also when data is being written to EEPROM.

$\overline{\text{TSTAT}}$ and $\overline{\text{TERR}}$ can be configured as open-drain type signals during an "ISC_ENABLE" command. This facilitates a wired-OR connection of $\overline{\text{TSTAT}}$ signals from several PSD813F devices and a wired-OR connection of $\overline{\text{TERR}}$ signals from those same devices. This is useful when several PSD813F devices are "chained" together in a JTAG environment.

9.6.3 Security and Flash Memories and EEPROM Protection

When the security bit is set, the device cannot be read on a device programmer or through the JTAG Port. When using the JTAG Port, only a full chip erase command is allowed. All other program/erase/verify commands are blocked. Full chip erase returns the part to a non-secured blank state. The Security Bit can be set in PSDsoft Configuration.

All Flash Memory and EEPROM sectors can individually be sector protected against erasures. The sector protect bits can be set in PSDsoft Configuration.

**Absolute
Maximum
Ratings**

<i>Symbol</i>	<i>Parameter</i>	<i>Condition</i>	<i>Min</i>	<i>Max</i>	<i>Unit</i>
T _{STG}	Storage Temperature	PLDCC	- 65	+ 125	°C
	Operating Temperature	Commercial	0	+ 70	°C
		Industrial	- 40	+ 85	°C
	Voltage on any Pin	With Respect to GND	- 0.6	+ 7	V
V _{PP}	Device Programmer Supply Voltage	With Respect to GND	- 0.6	+ 14	V
V _{CC}	Supply Voltage	With Respect to GND	- 0.6	+ 7	V
	ESD Protection		>2000		V

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not recommended. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

**Operating
Range**

<i>Range</i>	<i>Temperature</i>	<i>V_{CC} Tolerance</i>
Commercial	0° C to +70°C	+ 5 V ± 10%
Industrial	-40° C to +85°C	+ 5 V ± 10%
Commercial	0° C to +70°C	2.7 V to 3.6 V
Industrial	-40° C to +85°C	2.7 V to 3.6 V

**Recommended
Operating
Conditions**

<i>Symbol</i>	<i>Parameter</i>	<i>Condition</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>
V _{CC}	Supply Voltage	All Speeds	4.5	5	5.5	V
V _{CC}	Supply Voltage	V-Versions All Speeds	2.7		3.6	V

**AC/DC
Parameters**

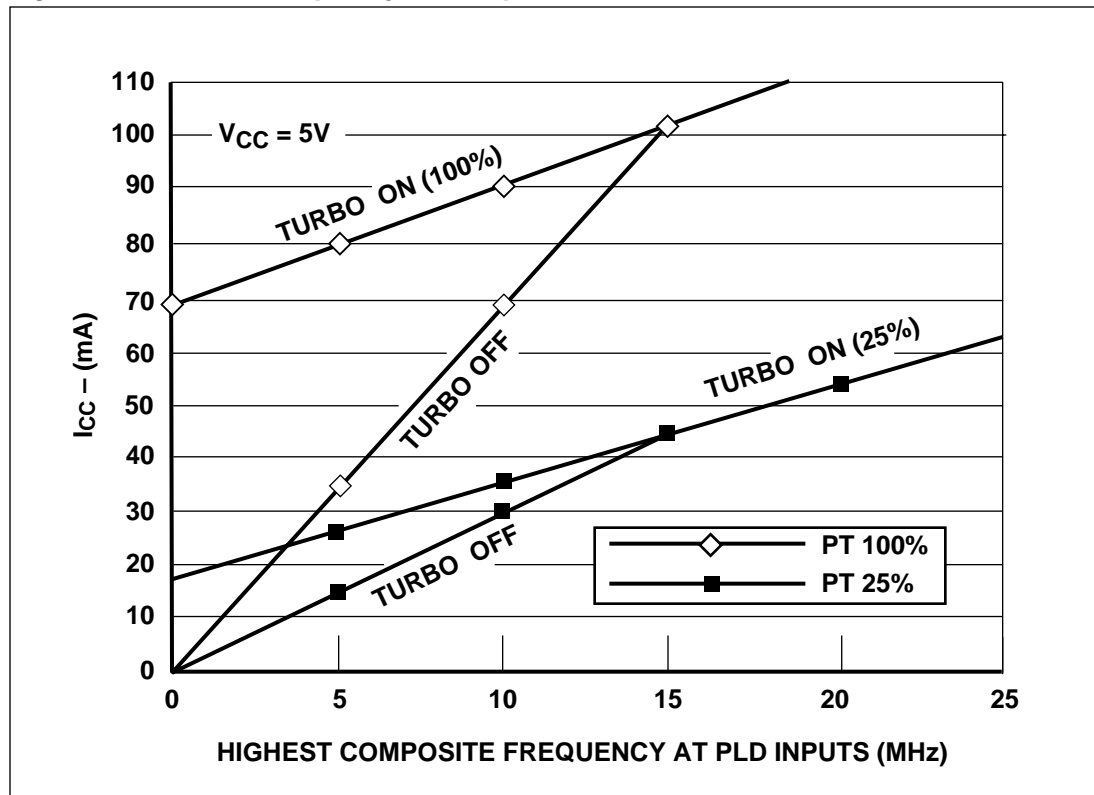
The following tables describe the AD/DC parameters of the PSD813F family:

- DC Electrical Specification
- AC Timing Specification
 - PLD Timing
 - Combinatorial Timing
 - Synchronous Clock Mode
 - Asynchronous Clock Mode
 - Input Micro↔Cell Timing
 - Microcontroller Timing
 - Read Timing
 - Write Timing
 - Peripheral Mode Timing
 - Power Down and Reset Timing

Following are issues concerning the parameters presented:

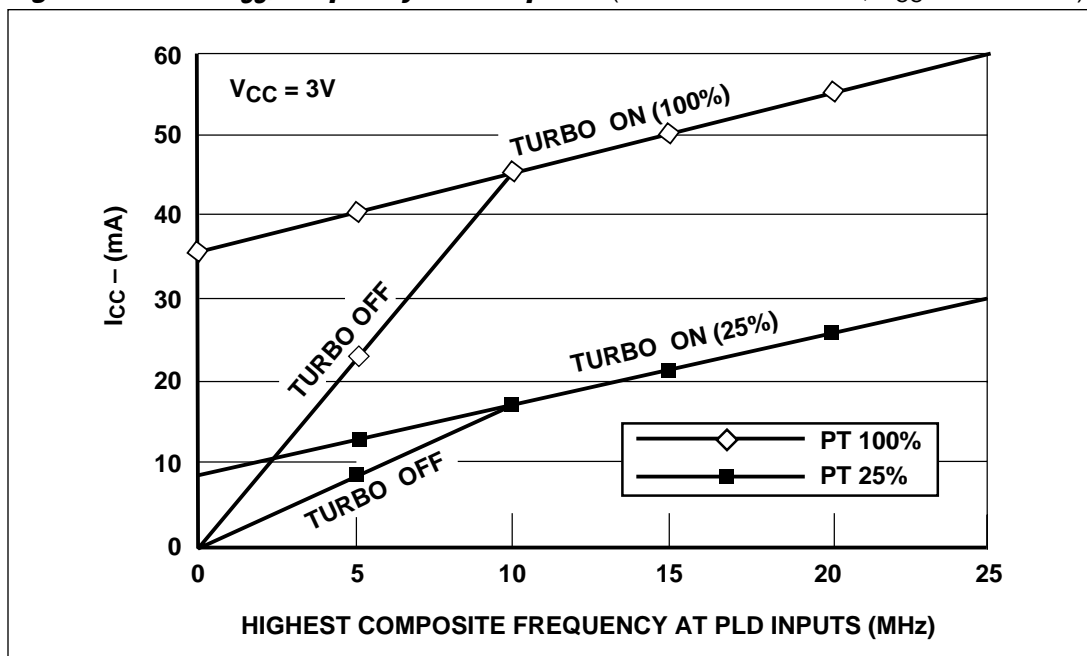
- In the DC specification the supply current is given for different modes of operation. Before calculating the total power consumption, determine the percentage of time that the PSD813F is in each mode. Also, the supply power is considerably different if the Turbo bit is "OFF" (ZPSD813F and ZPSD813FV).
- The AC power component gives the PLD, EPROM, and SRAM mA/MHz specification. Figures 34 and 34a show the PLD mA/MHz as a function of the number of Product Terms (PT) used.
- In the PLD timing parameters, add the required delay when Turbo bit is "OFF".

Figure 34. PLD I_{CC} /Frequency Consumption ($V_{CC} = 5\text{ V} \pm 10\%$)



**AC/DC
Parameters
(cont.)**

Figure 34a. PLD I_{CC} /Frequency Consumption (PSD813FV Versions, $V_{CC} = 3\text{ V} \pm 10\%$)



Example of PSD813F Typical Power Calculation at $V_{CC} = 5.0\text{ V}$

Conditions	
Highest Composite PLD input frequency (Freq PLD)	= 8 MHz
MCU ALE frequency (Freq ALE)	= 4 MHz
% Flash Access	= 80%
% SRAM access	= 15%
% I/O access	= 5% (no additional power above base)
Operational Modes	
% Normal	= 10%
% Power Down Mode	= 90%
Number of product terms used (from fitter report)	
	= 45 PT
% of total product terms	= 45/182 = 24.7%
Turbo Mode	= ON
Calculation (typical numbers used)	
$I_{CC\ total} = I_{pwrdown} \times \%pwrdown + \%normal \times (I_{CC\ (ac)} + I_{CC\ (dc)})$ $= I_{pwrdown} \times \%pwrdown + \%normal \times (\%flash \times 2.5\text{ mA/MHz} \times \text{Freq ALE} + \%SRAM \times 1.5\text{ mA/MHz} \times \text{Freq ALE} + \%PLD \times 2\text{ mA/MHz} \times \text{Freq PLD} + \#PT \times 400\ \mu\text{A/PT})$ $= 50\ \mu\text{A} \times 0.90 + 0.1 \times (0.8 \times 2.5\text{ mA/MHz} \times 4\text{ MHz} + 0.15 \times 1.5\text{ mA/MHz} \times 4\text{ MHz} + 2\text{ mA/MHz} \times 8\text{ MHz} + 45 \times 0.4\text{ mA/PT})$ $= 45\ \mu\text{A} + 0.1 \times (8 + 0.9 + 16 + 18\text{ mA})$ $= 45\ \mu\text{A} + 0.1 \times 42.9$ $= 45\ \mu\text{A} + 4.29\text{ mA}$ $= \mathbf{4.34\text{ mA}}$	
This is the operating power with no EEPROM writes or Flash erases. Calculation is based on $I_{OUT} = 0\text{ mA}$.	



**AC/DC
Parameters
(cont.)**

Example of ZPSD813F Typical Power Calculation at $V_{CC} = 5.0\text{ V}$

Conditions	
Highest Composite PLD input frequency (Freq PLD)	= 8 MHz
MCU ALE frequency (Freq ALE)	= 4 MHz
% Flash Access	= 80%
% SRAM access	= 15%
% I/O access	= 5% (no additional power above base)
Operational Modes	
% Normal	= 10%
% Power Down Mode	= 90%
Number of product terms used (from fitter report)	= 45 PT
% of total product terms	= 45/182 = 24.7%
Turbo Mode	= Off
Calculation (typical numbers used)	
$I_{CC} \text{ total} = I_{pwrdown} \times \%pwrdown + \%normal \times (I_{CC} \text{ (ac)} + I_{CC} \text{ (dc)})$ $= I_{pwrdown} \times \%pwrdown + \%normal \times (\%flash \times 2.5 \text{ mA/MHz} \times \text{Freq ALE} + \%SRAM \times 1.5 \text{ mA/MHz} \times \text{Freq ALE} + \%PLD \times (\text{from graph using Freq PLD}))$ $= 50 \mu\text{A} \times 0.90 + 0.1 \times (0.8 \times 2.5 \text{ mA/MHz} \times 4 \text{ MHz} + 0.15 \times 1.5 \text{ mA/MHz} \times 4 \text{ MHz} + 24 \text{ mA})$ $= 45 \mu\text{A} + 0.1 \times (8 + 0.9 + 24)$ $= 45 \mu\text{A} + 0.1 \times 32.9$ $= 45 \mu\text{A} + 3.29 \text{ mA}$ $= \mathbf{3.34 \text{ mA}}$	
<p>This is the operating power with no EEPROM writes or Flash erases. Calculation is based on $I_{OUT} = 0 \text{ mA}$.</p>	

PSD813F/ZPSD813F DC Characteristics (5 V \pm 10% Versions)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	All Speeds	4.5	5	5.5	V
V _{IH}	High Level Input Voltage	4.5 V < V _{CC} < 5.5 V	2		V _{CC} +.5	V
V _{IL}	Low Level Input Voltage	4.5 V < V _{CC} < 5.5 V	-.5		0.8	V
V _{IH1}	Reset High Level Input Voltage	(Note 1)	.8 V _{CC}		V _{CC} +.5	V
V _{IL1}	Reset Low Level Input Voltage	(Note 1)	-.5		.2 V _{CC} -.1	V
V _{HYS}	Reset Pin Hysteresis		0.3			V
V _{LKO}	V _{CC} Min for Flash Erase and Program		2.5		4.2	V
V _{OL}	Output Low Voltage	I _{OL} = 20 μ A, V _{CC} = 4.5 V		0.01	0.1	V
		I _{OL} = 8 mA, V _{CC} = 4.5 V		0.25	0.45	V
V _{OH}	Output High Voltage Except V _{STBY} On	I _{OH} = -20 μ A, V _{CC} = 4.5 V	4.4	4.49		V
		I _{OH} = -2 mA, V _{CC} = 4.5 V	2.4	3.9		V
V _{OH1}	Output High Voltage V _{STBY} On	I _{OH1} = 1 μ A	V _{SBY} - 0.8			V
V _{SBY}	SRAM Standby Voltage		2.0		V _{CC}	V
I _{SBY}	SRAM Standby Current	V _{CC} = 0 V		0.5	1	μ A
I _{IDLE}	Idle Current (V _{STBY} Pin)	V _{CC} > V _{SBY}	-0.1		0.1	μ A
V _{DF}	SRAM Data Retention Voltage	Only on V _{STBY}	2			V
I _{LI}	Input Leakage Current	V _{SS} < V _{IN} < V _{CC}	-1	\pm 1	1	μ A
I _{LO}	Output Leakage Current	0.45 < V _{IN} > V _{CC}	-10	\pm 5	10	μ A

NOTES: 1. Reset input has hysteresis. V_{IL1} is valid at or below .2V_{CC} -.1. V_{IH1} is valid at or above .8V_{CC}.

PSD813F DC Characteristics (I_{CC})

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
I_{CC} (DC) (Note 4)	Operating Supply Current	PLD Only	$f = 0$ MHz		400	700	μ A/PT
		Flash or EEPROM	During Flash or EEPROM Write/Erase Only		30	60	mA
			Read Only, $f = 0$ MHz		0	0	mA
		SRAM	$f = 0$ MHz		0	0	mA
I_{CC} (AC) (Note 4)	PLD AC Adder				2	3	mA/MHz
	Flash or EEPROM AC Adder				2.5	3.5	mA/MHz
	SRAM AC Adder				1.5	3.0	mA/MHz
I_{SB}	Standby Supply Current for Power Down Mode		$\overline{CSi} > V_{CC} - 0.3$ V (Note 1)	200 μ A + PLD Current (Note 3)			μ A

ZPSD813F DC Characteristics (I_{CC})

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
I_{CC} (DC) (Note 4)	Operating Supply Current	ZPLD Only	ZPLD_TURBO = OFF, $f = 0$ MHz (Note 4)		0		mA
			ZPLD_TURBO = ON, $f = 0$ MHz		400	700	μ A/PT
		Flash or EEPROM	During Flash or EEPROM Write/Erase Only		30	60	mA
			Read Only, $f = 0$ MHz		0	0	mA
		SRAM	$f = 0$ MHz		0	0	mA
I_{CC} (AC) (Note 4)	ZPLD AC Adder						Figure 34
	FLASH or EEPROM AC Adder				2.5	3.5	mA/MHz
	SRAM AC Adder				1.5	3.0	mA/MHz
I_{SB}	Standby Supply Current for Power Down Mode		$\overline{CSi} > V_{CC} - 0.3$ V (Notes 1 and 2)		50	200	μ A

- NOTES:**
- \overline{CSi} deselected or internal Power Down mode is active.
 - PLD is in non-turbo mode and none of the inputs are switching.
 - Refer to Figure 34 for PLD current calculation.
 - $I_{OUT} = 0$ mA

**PSD813F AC/DC
Parameters –
CPLD Timing
Parameters**
(5 V ± 10% Versions)

CPLD Combinatorial Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-90		-12		-15		Fast PT Aloc	TURBO OFF*	Slew (Note 1)	Unit
			Min	Max	Min	Max	Min	Max				
t _{PD}	CPLD Input Pin/Feedback to CPLD Combinatorial Output			25			30		32	Add 2	Sub 2	ns
t _{EA}	CPLD Input to CPLD Output Enable			26			30		32	Add 10	Sub 2	ns
t _{ER}	CPLD Input to CPLD Output Disable			26			30		32	Add 10	Sub 2	ns
t _{ARP}	CPLD Register Clear or Preset Delay			26			30		33	Add 10	Sub 2	ns
t _{ARPW}	CPLD Register Clear or Preset Pulse Width		20		24					Add 10		ns
t _{ARD}	CPLD Array Delay	Any Micro↔Cell		16		18		22	Add 2			ns

NOTE: 1. Fast Slew Rate output available on PA[3:0], PB[3:0], and PD[2:0].

*ZPSD versions only.



**PSD813F AC/DC
Parameters –
CPLD Timing
Parameters**
(5 V ± 10% Versions)

CPLD Micro ↔ Cell Synchronous Clock Mode Timing (5 V ± 10% Versions)

Symbol	Parameter	Conditions	-90		-12		-15		Fast PT Aloc	TURBO OFF*	Slew (Note 1)	Unit
			Min	Max	Min	Max	Min	Max				
f _{MAX}	Maximum Frequency External Feedback	1/(t _s +t _{CO})		30.30		26.3		23.8				MHz
	Maximum Frequency Internal Feedback (f _{CNT})	1/(t _s +t _{CO} -10)		43.48		35.7		31.25				MHz
	Maximum Frequency Pipelined Data	1/(t _{CH} +t _{CL})		50.00		41.67		33.3				MHz
t _s	Input Setup Time		15		18		20		Add 2	Add 10		ns
t _H	Input Hold Time		0		0		0					ns
t _{CH}	Clock High Time	Clock Input	10		12		15					ns
t _{CL}	Clock Low Time	Clock Input	10		12		15					ns
t _{CO}	Clock to Output Delay	Clock Input		18		20		22			Sub 2	ns
t _{ARD}	CPLD Array Delay	Any Micro ↔ Cell		16		18		22	Add 2			ns
t _{MIN}	Minimum Clock Period	t _{CH} +t _{CL} (Note 2)	20		24		30					ns

NOTES: 1. Fast Slew Rate output available on PA[3:0], PB[3:0], and PD[2:0].

2. CLKIN t_{CLCL} = t_{CH} + t_{CL}.

*ZPSD versions only.



**PSD813F AC/DC
Parameters –
CPLD Timing
Parameters**
(5 V ± 10% Versions)

CPLD Micro ↔ Cell Asynchronous Clock Mode Timing (5 V ± 10% Versions)

Symbol	Parameter	Conditions	-90		-12		-15		PT Alloc	TURBO OFF*	Slew Rate	Unit
			Min	Max	Min	Max	Min	Max				
f _{MAXA}	Maximum Frequency External Feedback	1/(t _{SA} + t _{COA})		26.32		23.25		20.4				MHZ
	Maximum Frequency Internal Feedback (f _{CNTA})	1/(t _{SA} + t _{COA} - 10)		35.71		30.30		25.64				MHZ
	Maximum Frequency Pipelined Data	1/(t _{CHA} + t _{CLA})		41.67		35.71		33.3				MHZ
t _{SA}	Input Setup Time		8		10				Add 2	Add 10		ns
t _{HA}	Input Hold Time		12		14							ns
t _{CHA}	Clock Input High Time		12		14					Add 10		ns
t _{CLA}	Clock Input Low Time		12		14					Add 10		ns
t _{COA}	Clock to Output Delay			30		33		37		Add 10	Sub 2	ns
t _{ARDA}	CPLD Array Delay	Any Micro ↔ Cell		16		18		22	Add 2			ns
t _{MINA}	Minimum Clock Period	1/f _{CNTA}	28		33			39				ns

*ZPSD versions only.



PSD813F AC/DC Parameters – CPLD Timing Parameters

(5 V ± 10% Versions)

Input Micro ⇄ Cell Timing (5 V ± 10% Versions)

Symbol	Parameter	Conditions	-90		-12		15		PT Aloc	TURBO OFF*	Unit
			Min	Max	Min	Max	Min	Max			
t _{IS}	Input Setup Time	(Note 1)	0		0		0				ns
t _{IH}	Input Hold Time	(Note 1)	20		22		26			Add 10	ns
t _{INH}	NIB Input High Time	(Note 1)	12		15		18				ns
t _{INL}	NIB Input Low Time	(Note 1)	12		15		18				ns
t _{INO}	NIB Input to Combinatorial Delay	(Note 1)		46		50		59	Add 2	Add 10	ns

NOTE: 1. Inputs from Port A, B, and C relative to register/latch clock from the PLD. ALE/AS latch timings refer to t_{AVLX} and t_{AXX}.

*ZPSD versions only.



Microcontroller Interface – AC/DC Parameters

(5V ± 10% Versions)

AC Symbols for PLD Timing.

Example: t_{AVLX} – Time from Address Valid to ALE Invalid.

Signal Letters

- A** – Address Input
- C** – CEout Output
- D** – Input Data
- E** – E Input
- G** – Internal WDOG_ON signal
- I** – Interrupt Input
- L** – ALE Input
- N** – Reset Input or Output
- P** – Port Signal Output
- Q** – Output Data
- R** – \overline{WR} , \overline{UDS} , \overline{LDS} , \overline{DS} , IORD, \overline{PSEN} Inputs
- S** – Chip Select Input
- T** – R/W Input
- W** – Internal PDN Signal
- B** – Vstby Output
- M** – Output Micro↔Cell

Signal Behavior

- t** – Time
- L** – Logic Level Low or ALE
- H** – Logic Level High
- V** – Valid
- X** – No Longer a Valid Logic Level
- Z** – Float
- PW** – Pulse Width

Microcontroller Interface – PSD813F AC/DC Parameters

(5V ± 10% Versions)

Read Timing (5 V ± 10% Versions)

Symbol	Parameter	Conditions	-90		-12		-15		Turbo Off	Unit
			Min	Max	Min	Max	Min	Max		
t _{LVLX}	ALE or AS Pulse Width		20		22		28			ns
t _{AVLX}	Address Setup Time	(Note 3)	6		8		10			ns
t _{LXAX}	Address Hold Time	(Note 3)	8		9		11			ns
t _{AVQV}	Address Valid to Data Valid	(Note 3)		90		120		150	Add 10	ns
t _{SLQV}	CS Valid to Data Valid			100		135		150		ns
t _{RLQV}	\overline{RD} to Data Valid 8-Bit Bus	(Note 5)		32		35		40		ns
	\overline{RD} or \overline{PSEN} to Data Valid 8-Bit Bus, 8031, 80251	(Note 2)		38		42		45		ns
t _{RHQX}	\overline{RD} Data Hold Time	(Note 1)	0		0		0			ns
t _{RLRH}	\overline{RD} Pulse Width	(Note 1)	32		35		38			ns
t _{RHQZ}	\overline{RD} to Data High-Z	(Note 1)		25		29		33		ns
t _{EHEL}	E Pulse Width		32		36		38			ns
t _{THEH}	R/ \overline{W} Setup Time to Enable		10		13		18			ns
t _{ELTL}	R/ \overline{W} Hold Time After Enable		0		0		0			ns
t _{AVPV}	Address Input Valid to Address Output Delay	(Note 4)		32		40		48		ns

- NOTES:**
1. \overline{RD} timing has the same timing as \overline{DS} , \overline{LDS} , \overline{UDS} , and \overline{PSEN} signals.
 2. \overline{RD} and \overline{PSEN} have the same timing.
 3. Any input used to select an internal PSD813F function.
 4. In multiplexed mode, latched addresses generated from ADIO delay to address output on any Port.
 5. \overline{RD} timing has the same timing as \overline{DS} , \overline{LDS} , and \overline{UDS} signals.

Microcontroller Interface – PSD813F AC/DC Parameters

(5V ± 10% Versions)

Write, Erase and Program Timing (5 V ± 10% Versions)

Symbol	Parameter	Conditions	-90		-12		-15		Unit
			Min	Max	Min	Max	Min	Max	
t_{LVLX}	ALE or AS Pulse Width		20		22		28		
t_{AVLX}	Address Setup Time	(Note 1)	6		8		10		ns
t_{LXAX}	Address Hold Time	(Note 1)	8		9		11		ns
t_{AVWL}	Address Valid to Leading Edge of \overline{WR}	(Notes 1 and 3)	20		25		30		ns
t_{SLWL}	\overline{CS} Valid to Leading Edge of \overline{WR}	(Note 3)	25		30		35		ns
t_{DVWH}	\overline{WR} Data Setup Time	(Note 3)	35		40		45		ns
t_{WHDX}	\overline{WR} Data Hold Time	(Note 3)	5		5		5		ns
t_{WLVH}	\overline{WR} Pulse Width	(Note 3)	35		40		45		ns
t_{WHAX}	Trailing Edge of \overline{WR} to Address Invalid	(Note 3)	0		0		0		ns
t_{WHPV}	Trailing Edge of \overline{WR} to Port Output Valid Using I/O Port Data Register	(Note 3)		30		35		38	ns
t_{WLMV}	\overline{WR} Valid to Port Output Valid Using Micro \leftrightarrow Cell Register Preset/Clear	(Notes 3 and 4)		55		60		65	ns
t_{WHQV1}	Byte Programming Operation	Also including pre-programming time	14		14		14		μ s
t_{WHQV2}	Sector Erase Operation	Note 100% tested		2.2		2.2		2.2	sec
t_{Q7VQV}	Q7 Valid to Output Valid (Data Polling)			60		65		70	ns
t_{VCS}	V_{CC} Setup Time V_{CC} High to First Flash \overline{WR} Low		45		48		50		μ s
t_{DVMV}	Data Valid to Port Output Valid Using Micro \leftrightarrow Cell Register Preset/Clear	(Notes 3 and 5)		55		60		65	ns
t_{AVPV}	Address Input Valid to Address Output Delay	(Note 2)		32		40		48	ns

- NOTES:**
- Any input used to select an internal PSD813F function.
 - In multiplexed mode, latched addresses generated from ADIO delay to address output on any Port.
 - \overline{WR} timing has the same timing as E, \overline{LDS} , \overline{UDS} , \overline{WRL} , and \overline{WRH} signals.
 - Assuming data is stable before active write signal.
 - Assuming write is active before data becomes valid.

Microcontroller Interface – PSD813F AC/DC Parameters

(5V ± 10% Versions)

Port A Peripheral Data Mode Read Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-90		-12		-15		Turbo Off	Unit
			Min	Max	Min	Max	Min	Max		
t _{AVQV (PA)}	Address Valid to Data Valid	(Note 3)		55		59		62	Add 10	ns
t _{SLQV (PA)}	$\overline{\text{CSI}}$ Valid to Data Valid			55		59		62	Add 10	ns
t _{RLQV (PA)}	$\overline{\text{RD}}$ to Data Valid	(Notes 1 and 4)		32		35		40		ns
	$\overline{\text{RD}}$ to Data Valid 8031 Mode			38		42		45		ns
t _{DVQV (PA)}	Data In to Data Out Valid			40		43		45		ns
t _{QXRH (PA)}	$\overline{\text{RD}}$ Data Hold Time		0		0		0			ns
t _{RLRH (PA)}	$\overline{\text{RD}}$ Pulse Width	(Note 1)	32		35		38			ns
t _{RHQZ (PA)}	$\overline{\text{RD}}$ to Data High-Z	(Note 1)		25		30		33		ns

Port A Peripheral Data Mode Write Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-90		-12		-15		Unit
			Min	Max	Min	Max	Min	Max	
t _{WLQV (PA)}	$\overline{\text{WR}}$ to Data Propagation Delay	(Note 2)		35		38		40	ns
t _{DVQV (PA)}	Data to Port A Data Propagation Delay	(Note 5)		40		43		45	ns
t _{WHQZ (PA)}	$\overline{\text{WR}}$ Invalid to Port A Tri-state	(Note 2)		25		30		33	ns

- NOTES:**
- $\overline{\text{RD}}$ timing has the same timing as $\overline{\text{DS}}$, $\overline{\text{LDS}}$, $\overline{\text{UDS}}$, and $\overline{\text{PSEN}}$ (in 8031 combined mode) signals.
 - $\overline{\text{WR}}$ timing has the same timing as $\overline{\text{E}}$, $\overline{\text{LDS}}$, $\overline{\text{UDS}}$, $\overline{\text{WRL}}$, and $\overline{\text{WRH}}$ signals.
 - Any input used to select Port A Data Peripheral Mode.
 - Data is already stable on Port A.
 - Data stable on ADIO pins to data on Port A.

Microcontroller Interface – PSD813F AC/DC Parameters

(5V ± 10% Versions)

Power Down Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-90		-12		-15		Unit
			Min	Max	Min	Max	Min	Max	
t _{LVDV}	ALE Access Time from Power Down			120		135		150	ns
t _{CLWH}	Maximum Delay from APD Enable to Internal PDN Valid Signal	Using CLKIN Input	15 * t _{CLCL} (Note 1)						µs

NOTE: 1. t_{CLCL} is the CLKIN clock period.**V_{stbyon} Timing** (5 V ± 10%)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{BVBH}	V _{stby} Detection to V _{stbyon} Output High			20		µs
t _{BXBL}	V _{stby} Off Detection to V _{stbyon} Output Low			20		µs

Reset Timing (5 V ± 10%)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{NLNH}	Warm RESET Active Low Time (Note 1)		150			ns
t _{OPR}	RESET High to Operational Device				120	ns
t _{NLNH-PO}	Power On Reset Active Low Time (Note 2)		1			ms

NOTE: 1. RESET will not reset Flash or EEPROM programming/erase cycles.
2. t_{NLNH-PO} is 10 ms for devices manufactured before rev. A.

Microcontroller Interface – PSD813F AC/DC Parameters

(5V ± 10% Versions)

Flash Program, Write and Erase Times (5 V ± 10%)

Symbol	Parameter	Min	Typ	Max	Unit
	Flash Program		8.5		sec
	Flash Bulk Erase (Preprogrammed) (Note 1)		3	30	sec
	Flash Bulk Erase (Not Preprogrammed)		10		sec
t _{WHQV3}	Sector Erase (Preprogrammed)		1	30	sec
t _{WHQV2}	Sector Erase (Not Preprogrammed)		2.2		sec
t _{WHQV1}	Byte Program	14		1200	μs
	Program/Erase Cycles (Per Sector)	100,000			cycles
t _{WHWLO}	Sector Erase Time-Out		100		μs

NOTE: 1. Programmed to all zeros before erase.**EEPROM Write Times** (5 V ± 10%)

Symbol	Parameter	Min	Typ	Max	Unit
t _{EEHWL}	Write Protect After Power Up		5		msec
t _{BLC}	EEPROM Byte Load Cycle Timing (Note 1)	0.2		120	μsec
t _{WCB}	EEPROM Byte Write Cycle Time		4	10	msec
t _{WCP}	EEPROM Page Write Cycle Time (Note 2)		6	30	msec
	Program/Erase Cycles (Per Sector)	10,000			cycles

NOTES: 1. If the maximum time has elapsed between successive writes to an EEPROM page, the transfer of this data to EEPROM cells will begin. Also, bytes cannot be written (loaded) to a page any faster than the indicated minimum type.
 2. These specifications are for writing a page to EEPROM cells.

ISC Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-90		-12		-15		Unit
			Min	Max	Min	Max	Min	Max	
t _{ISCCF}	TCK Clock Frequency (except for PLD)	(Note 1)		18		16		14	MHz
t _{ISCHH}	TCK Clock High Time	(Note 1)	26		29		31		ns
t _{ISCLL}	TCK Clock Low Time	(Note 1)	26		29		31		ns
t _{ISCCF-P}	TCK Clock Frequency (for PLD only)	(Note 2)		2		2		2	MHz
t _{ISCHH-P}	TCK Clock High Time (for PLD only)	(Note 2)	240		240		240		ns
t _{ISCLL-P}	TCK Clock Low Time (for PLD only)	(Note 2)	240		240		240		ns
t _{ISCPsu}	ISC Port Set Up Time		8		10		10		ns
t _{ISCPH}	ISC Port Hold Up Time		5		5		5		ns
t _{ISPCO}	ISC Port Clock to Output			23		24		25	ns
t _{ISCPZV}	ISC Port High-Impedance to Valid Output			23		24		25	ns
t _{ISCPVZ}	ISC Port Valid Output to High-Impedance			23		24		25	ns

NOTES: 1. For “non-PLD” programming, erase or in ISC by-pass mode.
 2. For program or erase PLD only.

ZPSD813FV DC Characteristics (2.7 V to 3.6 V Versions)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V _{CC}	Supply Voltage		All Speeds	2.7		3.6	V
V _{IH}	High Level Input Voltage		2.7 V < V _{CC} < 3.6 V	.7 V _{CC}		V _{CC} +.5	V
V _{IL}	Low Level Input Voltage		2.7 V < V _{CC} < 3.6 V	-.5		0.8	V
V _{IH1}	Reset High Level Input Voltage		(Note 1)	.8 V _{CC}		V _{CC} +.5	V
V _{IL1}	Reset Low Level Input Voltage		(Note 1)	-.5		.2 V _{CC} -.1	V
V _{HYS}	Reset Pin Hysteresis			0.3			V
V _{LKO}	V _{CC} Min for Flash Erase and Program			1.9		2.2	V
V _{OL}	Output Low Voltage		I _{OL} = 20 μA, V _{CC} = 2.7 V		0.01	0.1	V
			I _{OL} = 4 mA, V _{CC} = 2.7 V		0.15	0.45	V
V _{OH}	Output High Voltage Except V _{STBY} On		I _{OH} = -20 μA, V _{CC} = 2.7 V	2.6	2.69		V
			I _{OH} = -1 mA, V _{CC} = 2.7 V	2.3	2.4		V
V _{OH1}	Output High Voltage V _{STBY} On		I _{OH1} = 1 μA			V _{SBY} - 0.8	V
V _{SBY}	SRAM Standby Voltage			2.0		V _{CC}	V
I _{SBY}	SRAM Standby Current		V _{CC} = 0 V		0.5	1	μA
I _{IDLE}	Idle Current (V _{STBY} Pin)		V _{CC} > V _{SBY}	-0.1		0.1	μA
V _{DF}	SRAM Data Retention Voltage		Only on V _{STBY}	2			V
I _{SB}	Standby Supply Current for Power Down Mode		$\overline{\text{CSI}} > V_{CC} - 0.3 \text{ V}$ (Note 2)		25	100	μA
I _{LI}	Input Leakage Current		V _{SS} < V _{IN} < V _{CC}	-1	±1	1	μA
I _{LO}	Output Leakage Current		0.45 < V _{IN} < V _{CC}	-10	±5	10	μA
I _{CC} (DC) (Note 3)	Operating Supply Current	ZPLD Only	ZPLD_TURBO = OFF, f = 0 MHz (Note 3)		0		mA
			ZPLD_TURBO = ON, f = 0 MHz		200	400	μA/PT
		FLASH or EEPROM	During FLASH or EEPROM Write/Erase Only		10	25	mA
			Read Only, f = 0 MHz		0	0	mA
SRAM	f = 0 MHz		0	0	mA		
I _{CC} (AC) (Note 3)	ZPLD AC Adder						Figure 34a
	FLASH or EEPROM AC Adder			2	2.5		mA/MHz
	SRAM AC Adder			0.8	1.5		mA/MHz

- NOTES:**
- Reset input has hysteresis. V_{IL1} is valid at or below .2V_{CC} -.1. V_{IH1} is valid at or above .8V_{CC}.
 - CSI deselected or internal PD is active.
 - I_{OUT} = 0 mA

ZPSD813FV AC/DC Parameters – CPLD Timing Parameters

(2.7 V to 3.6 V Versions)

CPLD Combinatorial Timing (2.7 V to 3.6 V Versions)

Symbol	Parameter	Conditions	-15		-20		PT Aloc	TURBO OFF*	Slew Rate (Note 1)	Unit
			Min	Max	Min	Max				
t _{PD}	CPLD Input Pin/Feedback to CPLD Combinatorial Output			48		55	Add 4	Add 20	Sub 6	ns
t _{EA}	CPLD Input to CPLD Output Enable			43		50		Add 20	Sub 6	ns
t _{ER}	CPLD Input to CPLD Output Disable			43		50		Add 20	Sub 6	ns
t _{ARP}	CPLD Register Clear or Preset Delay			48		55		Add 20	Sub 6	ns
t _{ARPW}	CPLD Register Clear or Preset Pulse Width		30		35			Add 20		ns
t _{ARD}	CPLD Array Delay	Any Micro↔Cell		29		33	Add 4			ns

NOTE: 1. Fast Slew Rate output available on PA[3:0], PB[3:0], and PD[2:0].

*ZPSD versions only.

CPLD Micro↔Cell Synchronous Clock Mode Timing (2.7 V to 3.6 V Versions)

Symbol	Parameter	Conditions	-15		-20		PT Aloc	TURBO OFF*	Slew Rate (Note 1)	Unit
			Min	Max	Min	Max				
f _{MAX}	Maximum Frequency External Feedback	1/(t _S +t _{CO})		17.8		14.7				MHz
	Maximum Frequency Internal Feedback (f _{CNT})	1/(t _S +t _{CO} -10)		19.6		17.2				MHz
	Maximum Frequency Pipelined Data	1/(t _{CH} +t _{CL})		33.3		31.2				MHz
t _S	Input Setup Time		27		35		Add 4	Add 20		ns
t _H	Input Hold Time		0		0					ns
t _{CH}	Clock High Time	Clock Input	15		16					ns
t _{CL}	Clock Low Time	Clock Input	15		16					ns
t _{CO}	Clock to Output Delay	Clock Input		35		39			Sub 6	ns
t _{ARD}	CPLD Array Delay	Any Micro↔Cell		29		33	Add 4			ns
t _{MIN}	Minimum Clock Period	t _{CH} +t _{CL} (Note 2)	29		32					ns

NOTES: 1. Fast Slew Rate output available on PA[3:0], PB[3:0], and PD[2:0].

2. CLKIN t_{CLCL} = t_{CH} + t_{CL}.

*ZPSD versions only.

ZPSD813FV AC/DC Parameters – CPLD Timing Parameters

(2.7 V to 3.6 V Versions)

CPLD Micro↔Cell Asynchronous Clock Mode Timing (2.7 V to 3.6 V Versions)

Symbol	Parameter	Conditions	-15		-20		PT Aloc	TURBO OFF*	Slew Rate	Unit
			Min	Max	Min	Max				
f _{MAXA}	Maximum Frequency External Feedback	1/(t _{SA} +t _{COA})		16.9		14.7				MHz
	Maximum Frequency Internal Feedback (f _{CNTA})	1/(t _{SA} +t _{COA} -10)		20.4		17.2				MHz
	Maximum Frequency Pipelined Data	1/(t _{CHA} +t _{CLA})		27		24.4				MHz
t _{SA}	Input Setup Time		12		13		Add 4	Add 20		ns
t _{HA}	Input Hold Time		15		17					ns
t _{CHA}	Clock High Time		22		25			Add 20		ns
t _{CLA}	Clock Low Time		15		16			Add 20		ns
t _{COA}	Clock to Output Delay			47		55		Add 20	Sub 6	ns
t _{ARD}	CPLD Array Delay	Any Micro↔Cell		29		33	Add 4			ns
t _{MINA}	Minimum Clock Period	1/f _{CNTA}	43		58					ns

*ZPSD Versions Only.

Input Micro↔Cell Timing (2.7 V to 3.6 V Versions)

Symbol	Parameter	Conditions	-15		-20		PT Aloc	TURBO OFF*	Unit
			Min	Max	Min	Max			
t _{IS}	Input Setup Time	(Note 1)	0		0				ns
t _{IH}	Input Hold Time	(Note 1)	30		35			Add 20	ns
t _{INH}	NIB Input High Time	(Note 1)	13		15				ns
t _{INL}	NIB Input Low Time	(Note 1)	13		15				ns
t _{INO}	NIB Input to Combinatorial Delay	(Note 1)		90		100	Add 4	Add 20	ns

NOTE: 1. Inputs from Port A, B, and C relative to register/latch clock from the PLD. ALE latch timings refer to t_{AVLX} and t_{LXAX}.

*ZPSD Versions Only.

**Microcontroller
Interface –
ZPSD813FV
AC/DC
Parameters**

(3V ± 10% Versions)

AC Symbols for PLD Timing.

Example: t_{AVLX} – Time from Address Valid to ALE Invalid.

Signal Letters

- A** – Address Input
- C** – CEout Output
- D** – Input Data
- E** – E Input
- G** – Internal WDOG_ON signal
- I** – Interrupt Input
- L** – ALE Input
- N** – Reset Input or Output
- P** – Port Signal Output
- Q** – Output Data
- R** – \overline{WR} , \overline{UDS} , \overline{LDS} , \overline{DS} , IORD, \overline{PSEN} Inputs
- S** – Chip Select Input
- T** – R/W Input
- W** – Internal PDN Signal
- B** – Vstby Output
- M** – Output Micro↔Cell

Signal Behavior

- t** – Time
- L** – Logic Level Low or ALE
- H** – Logic Level High
- V** – Valid
- X** – No Longer a Valid Logic Level
- Z** – Float
- PW** – Pulse Width

Microcontroller Interface – ZPSD813FV AC/DC Parameters

(2.7 V to 3.6 V Versions)

Read Timing (2.7 V to 3.6 V Versions)

Symbol	Parameter	Conditions	-15		-20		Turbo Off	Unit
			Min	Max	Min	Max		
t _{LVLX}	ALE or AS Pulse Width		28		30			ns
t _{AVLX}	Address Setup Time	(Note 3)	10		12			ns
t _{LXAX}	Address Hold Time	(Note 3)	12		14			ns
t _{AVQV}	Address Valid to Data Valid	(Note 3)		150		200	Add 20	ns
t _{SLQV}	CS Valid to Data Valid			150		200		ns
t _{RLQV}	\overline{RD} to Data Valid 8-Bit Bus	(Note 5)		35		40		ns
	\overline{RD} or \overline{PSEN} to Data Valid 8-Bit Bus, 8031, 80251	(Note 2)		50		55		ns
t _{RHQX}	\overline{RD} Data Hold Time	(Note 1)	0		0			ns
t _{RLRH}	\overline{RD} Pulse Width (also \overline{DS} , \overline{LDS} , \overline{UDS})		40		45			ns
	\overline{RD} or \overline{PSEN} Pulse Width (8031, 80251)		55		60			ns
t _{RHQZ}	\overline{RD} to Data High-Z	(Note 1)		45		45		ns
t _{EHEL}	E Pulse Width		52		57			ns
t _{THEH}	R/ \overline{W} Setup Time to Enable		18		20			ns
t _{ELTL}	R/W Hold Time After Enable		0		0			ns
t _{AVPV}	Address Input Valid to Address Output Delay	(Note 4)		48		50		ns

- NOTES:**
1. \overline{RD} timing has the same timing as \overline{DS} , \overline{LDS} , \overline{UDS} , and \overline{PSEN} signals.
 2. \overline{RD} and \overline{PSEN} have the same timing for 8031.
 3. Any input used to select an internal PSD813F function.
 4. In multiplexed mode latched address generated from ADIO delay to address output on any Port.
 5. RD timing has the same timing as \overline{DS} , \overline{LDS} , and \overline{UDS} signals.

Microcontroller Interface – ZPSD813FV AC/DC Parameters

(2.7 V to 3.6 V Versions)

Write, Erase and Program Timing (2.7 V to 3.6 V Versions)

Symbol	Parameter	Conditions	-15		-20		Unit
			Min	Max	Min	Max	
t _{LVLX}	ALE or AS Pulse Width		28		30		
t _{AVLX}	Address Setup Time	(Note 1)	10		12		ns
t _{LXAX}	Address Hold Time	(Note 1)	12		14		ns
t _{AVWL}	Address Valid to Leading Edge of WR	(Notes 1 and 3)	30		35		ns
t _{SLWL}	$\overline{\text{CS}}$ Valid to Leading Edge of $\overline{\text{WR}}$	(Note 3)	34		40		ns
t _{DVWH}	$\overline{\text{WR}}$ Data Setup Time	(Note 3)	45		50		ns
t _{WHDX}	$\overline{\text{WR}}$ Data Hold Time	(Note 3)	8		10		ns
t _{WLWH}	$\overline{\text{WR}}$ Pulse Width	(Note 3)	48		53		ns
t _{WHAX}	Trailing Edge of $\overline{\text{WR}}$ to Address Invalid	(Note 3)	0		0		ns
t _{WHPV}	Trailing Edge of $\overline{\text{WR}}$ to Port Output Valid Using I/O Port Data Register	(Note 3)		45		50	ns
t _{WLMV}	$\overline{\text{WR}}$ Valid to Port Output Valid Using Micro \leftrightarrow Cell Register Preset/Clear	(Notes 3 and 4)		90		100	ns
t _{WHQV1}	Byte Programming Operation	Also including pre-programming time	14		14		μs
t _{WHQV2}	Sector Erase Operation	Note 100% tested		2.2		2.2	sec
t _{Q7VQV}	Q7 Valid to Output Valid (Data Polling)			70		75	ns
t _{VCS}	V _{CC} Setup Time V _{CC} High to First Flash $\overline{\text{WR}}$ Low		45		50		μs
t _{DVMV}	Data Valid to Port Output Valid Using Micro \leftrightarrow Cell Register Preset/Clear	(Notes 3 and 5)		90		100	ns
t _{AVPV}	Address Input Valid to Address Output Delay	(Note 2)		48		55	ns

- NOTES:**
- Any input used to select an internal PSD813F function.
 - In multiplexed mode, latched addresses generated from ADIO delay to address output on any Port.
 - WR timing has the same timing as E, LDS, UDS, WRL, and WRH signals.
 - Assuming data is stable before active write signal.
 - Assuming write is active before data becomes valid.

Microcontroller Interface – ZPSD813FV AC/DC Parameters

(2.7 V to 3.6 V Versions)

Port A Peripheral Data Mode Read Timing (2.7 V to 3.6 V Versions)

Symbol	Parameter	Conditions	-15		-20		Turbo Off	Unit
			Min	Max	Min	Max		
$t_{AVQV} (PA)$	Address Valid to Data Valid	(Note 3)		87		95	Add 20	ns
$t_{SLQV} (PA)$	\overline{CS} Valid to Data Valid			70		80	Add 20	ns
$t_{RLQV} (PA)$	\overline{RD} to Data Valid	(Notes 1 and 4)		40		45		ns
	\overline{RD} to Data Valid 8031 Mode			45		50		ns
$t_{DVQV} (PA)$	Data In to Data Out Valid			50		55		ns
$t_{QXRH} (PA)$	\overline{RD} Data Hold Time		0		0			ns
$t_{RLRH} (PA)$	\overline{RD} Pulse Width	(Note 1)	36		46			ns
$t_{RHQZ} (PA)$	\overline{RD} to Data High-Z	(Note 1)		32		35		ns

Port A Peripheral Data Mode Write Timing (2.7 V to 3.6 V Versions)

Symbol	Parameter	Conditions	-15		-20		Unit
			Min	Max	Min	Max	
$t_{WLQV} (PA)$	\overline{WR} to Data Propagation Delay	(Note 2)		45		55	ns
$t_{DVQV} (PA)$	Data to Port A Data Propagation Delay	(Note 5)		50		55	ns
$t_{WHQZ} (PA)$	\overline{WR} Invalid to Port A Tri-state	(Note 2)		33		35	ns

- NOTES:**
- \overline{RD} timing has the same timing as \overline{DS} , \overline{LDS} , \overline{UDS} , and \overline{PSEN} (in 8031 combined mode) signals.
 - \overline{WR} timing has the same timing as \overline{E} , \overline{LDS} , \overline{UDS} , \overline{WRL} , and \overline{WRH} signals.
 - Any input used to select Port A Data Peripheral Mode.
 - Data is already stable on Port A.
 - Data stable on ADIO pins to data on Port A.

Microcontroller Interface – ZPSD813FV AC/DC Parameters

(2.7 V to 3.6 V Versions)

Power Down Timing (2.7 V to 3.6 V Versions)

Symbol	Parameter	Conditions	-15		-20		Unit
			Min	Max	Min	Max	
t_{LVDV}	ALE Access Time from Power Down			150		200	ns
t_{CLWH}	Maximum Delay from APD Enable to Internal PDN Valid Signal	Using CLKIN Input	15 * t_{CLCL} (Note 1)				μ s

NOTE: 1. t_{CLCL} is the CLKIN clock period. **V_{stbyon} Timing** (2.7 V to 3.6 V Versions)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{BVBH}	V_{stby} Detection to V_{stbyon} Output High			2.0		μ s
t_{BXBL}	V_{stby} Off Detection to V_{stbyon} Output Low			2.0		μ s

Reset Timing (2.7 V to 3.6 V Versions)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{NLNH}	Warm RESET Active Low Time (Note 1)		300			ns
t_{OPR}	RESET High to Operational Device				300	ns
$t_{NLNH-PO}$	Power On Reset Active Low Time (Note 2)		1			ms

NOTE: 1. RESET will not reset Flash or EEPROM programming/erase cycles.
2. $t_{NLNH-PO}$ is 10 ms for devices manufactured before the rev. A.

Microcontroller Interface – ZPSD813FV AC/DC Parameters

(2.7 V to 3.6 V Versions)

Flash Program, Write and Erase Times (2.7 V to 3.6 V Versions)

Symbol	Parameter	Min	Typ	Max	Unit
	Flash Program		8.5		sec
	Flash Bulk Erase (Preprogrammed) (Note 1)		3	30	sec
	Flash Bulk Erase (Not Preprogrammed)		10		sec
t _{WHQV3}	Sector Erase (Preprogrammed)		1	30	sec
t _{WHQV2}	Sector Erase (Not Preprogrammed)		2		sec
t _{WHQV1}	Byte Program	10		1200	μs
	Program/Erase Cycles (Per Sector)	100,000			cycles
t _{WHWLO}	Sector Erase Time-Out		100		μs

NOTES: 1. Programmed to all zeros before erase.**EEPROM Write Times** (2.7 V to 3.6 V Versions)

Symbol	Parameter	Min	Typ	Max	Unit
t _{EEHWL}	Write Protect After Power Up		5		msec
t _{BLC}	EEPROM Byte Load Cycle Timing (Note 1)	0.2		120	μsec
t _{WCB}	EEPROM Byte Write Cycle Time		4	10	msec
t _{WCP}	EEPROM Page Write Cycle Time (Note 2)		6	30	msec
	Program/Erase Cycles (Per Sector)	10,000			cycles

NOTES: 1. If the maximum time has elapsed between successive writes to an EEPROM page, the transfer of this data to EEPROM cells will begin. Also, bytes cannot be written (loaded) to a page any faster than the indicated minimum type.

2. These specifications are for writing a page to EEPROM cells.

ISC Timing (2.7 V to 3.6 V Versions)

Symbol	Parameter	Conditions	-15		-20		Unit
			Min	Max	Min	Max	
t _{ISCCF}	TCK Clock Frequency (except for PLD)	(Note 1)		10		9	MHz
t _{ISCCH}	TCK Clock High Time	(Note 1)	45		51		ns
t _{ISCLL}	TCK Clock Low Time	(Note 1)	45		51		ns
t _{ISCCF-P}	TCK Clock Frequency (for PLD only)	(Note 2)		2		2	MHz
t _{ISCCH-P}	TCK Clock High Time (for PLD only)	(Note 2)	240		240		ns
t _{ISCLL-P}	TCK Clock Low Time (for PLD only)	(Note 2)	240		240		ns
t _{ISCPsu}	ISC Port Set Up Time		13		15		ns
t _{ISCPH}	ISC Port Hold Up Time		5		5		ns
t _{ISPCO}	ISC Port Clock to Output			36		40	ns
t _{ISCPZV}	ISC Port High-Impedance to Valid Output			36		40	ns
t _{ISCPVZ}	ISC Port Valid Output to High-Impedance			36		40	ns

NOTES: 1. For “non-PLD” programming, erase or in ISC by-pass mode.

2. For program or erase PLD only.

Figure 35. Read Timing

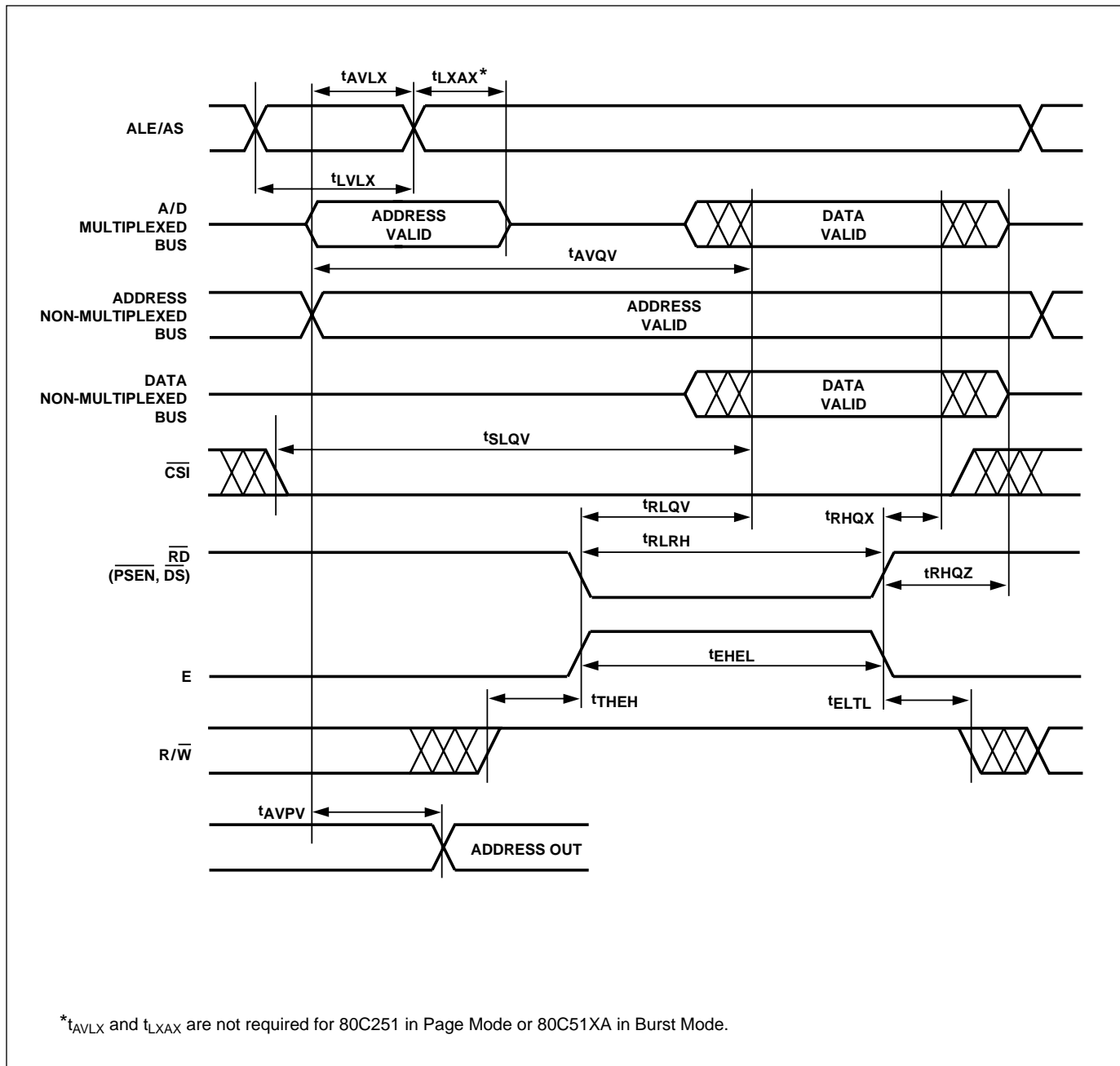


Figure 36. Write Timing

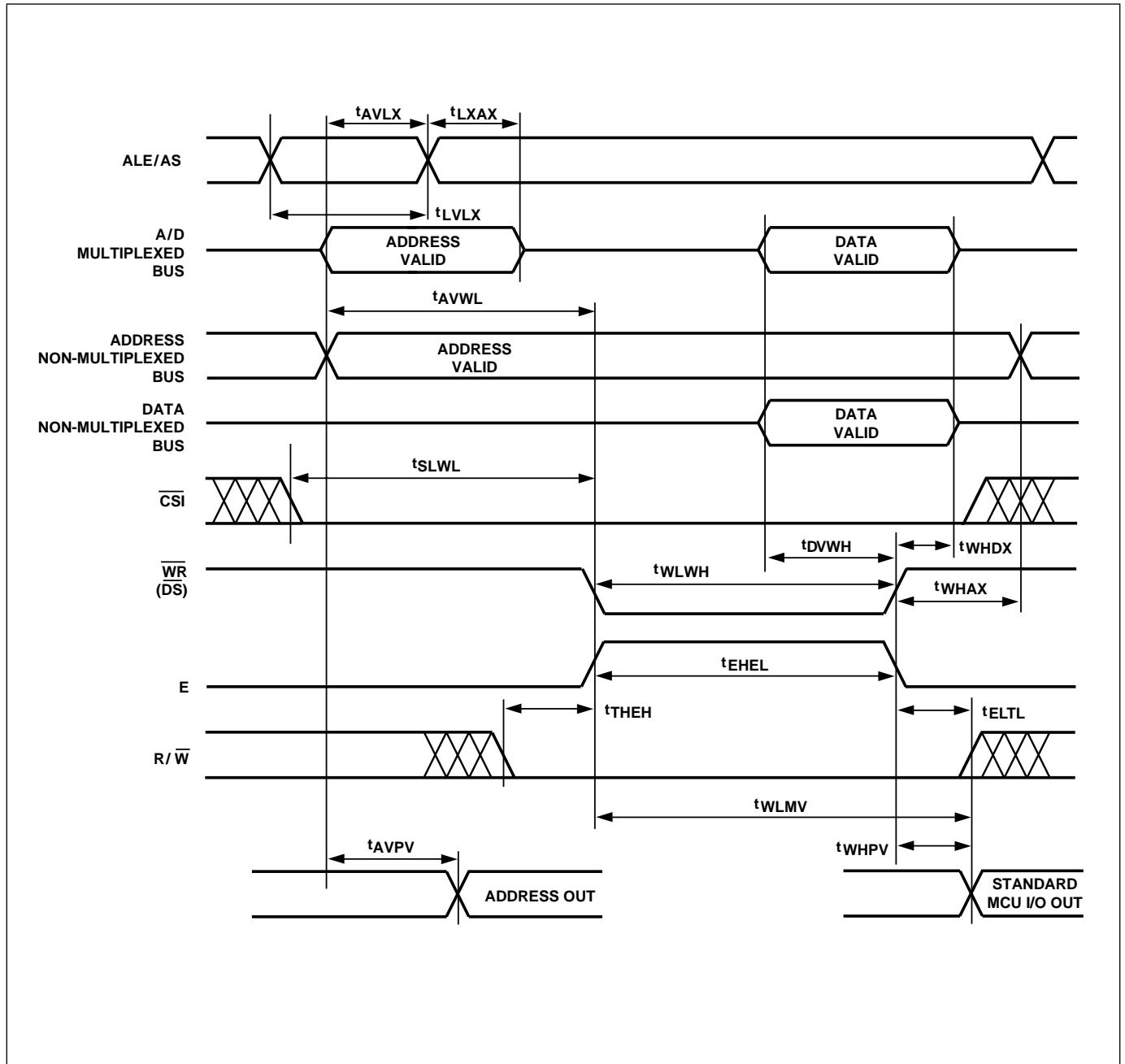


Figure 37. Peripheral I/O Read Timing

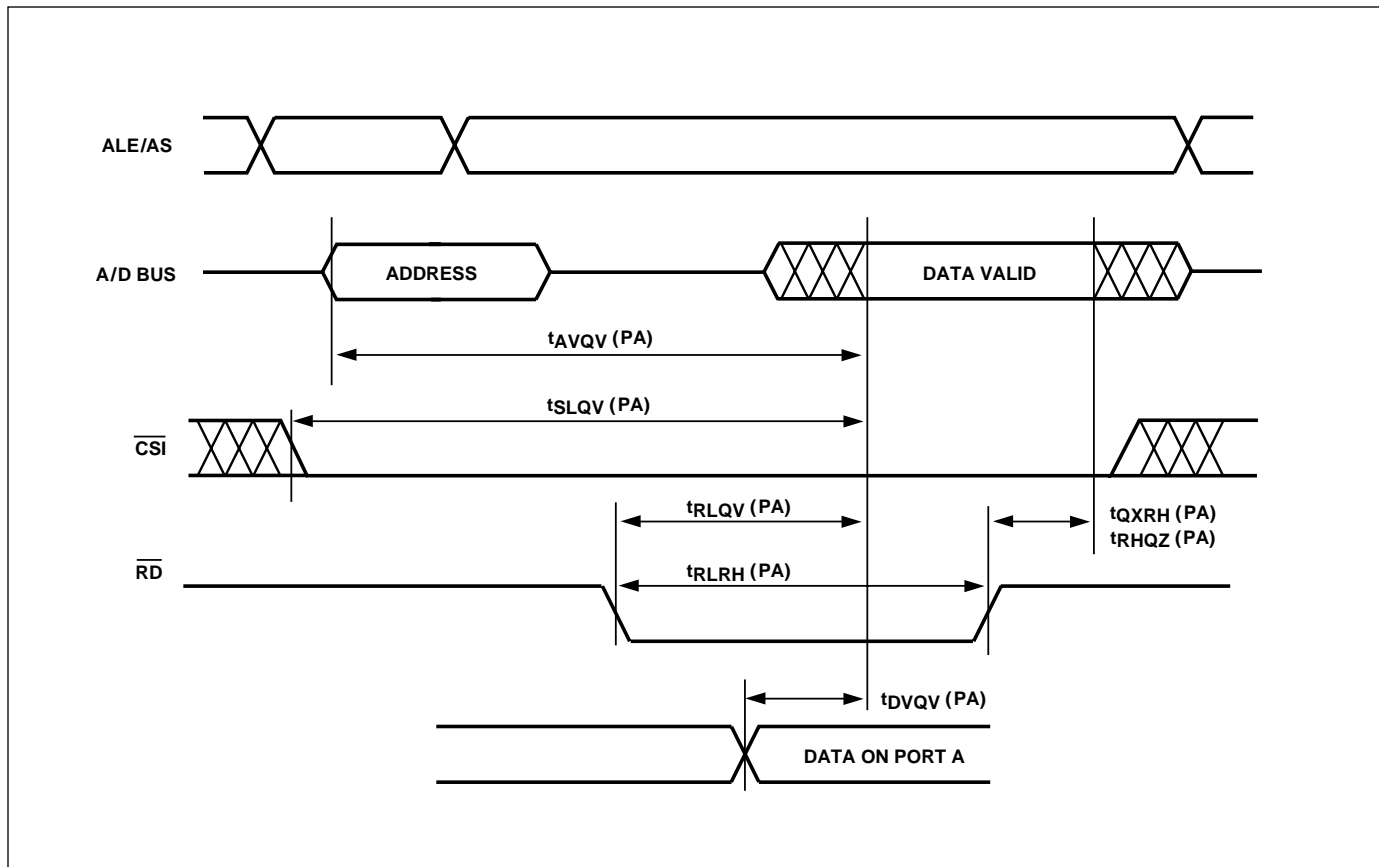


Figure 38. Peripheral I/O Write Timing

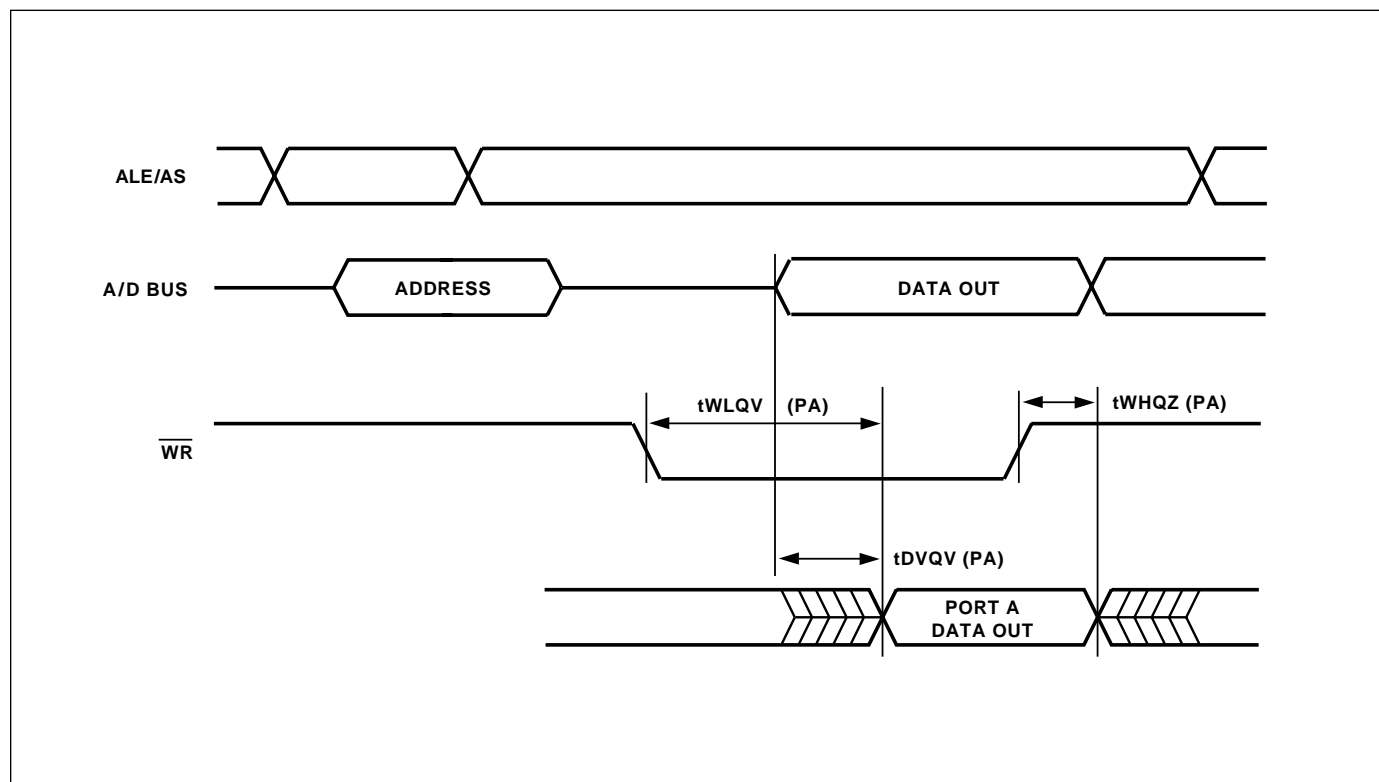


Figure 39. Combinatorial Timing – PLD

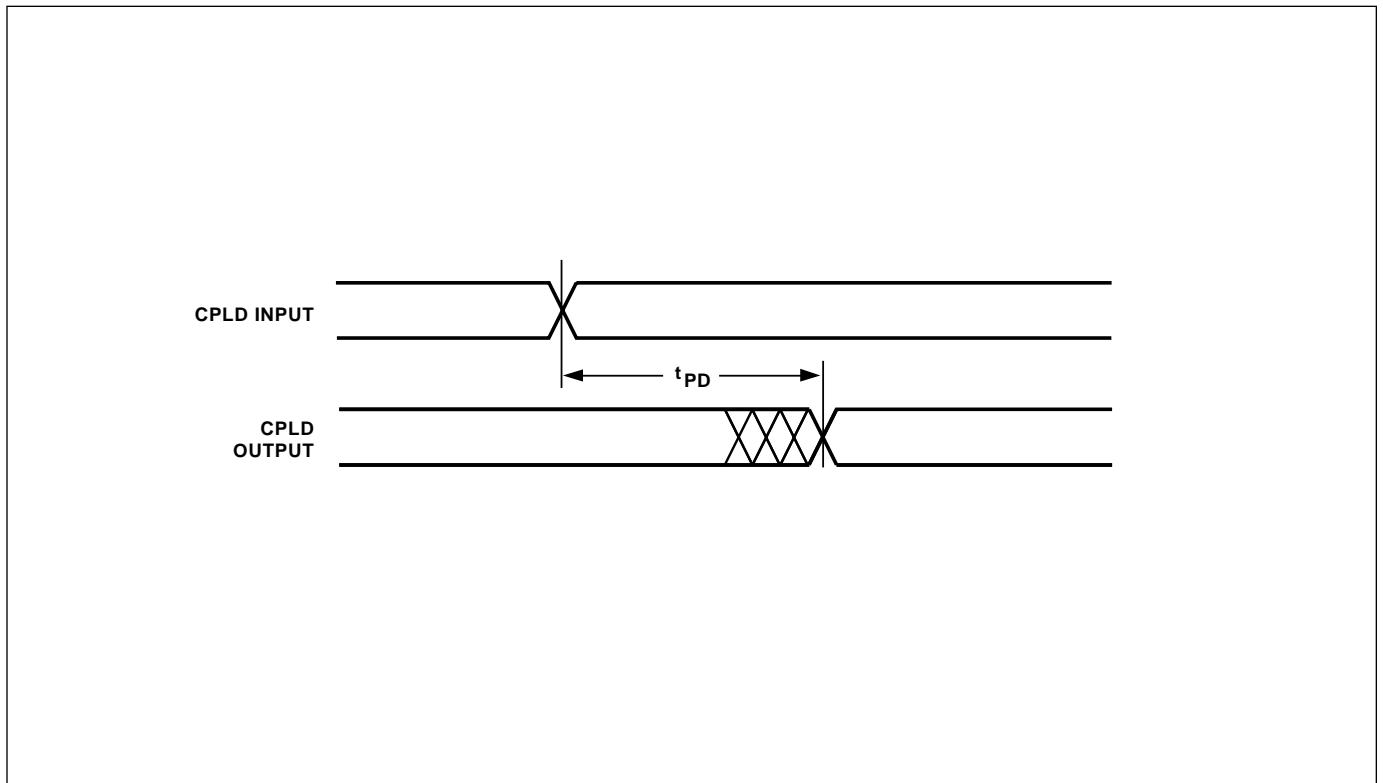


Figure 40. Synchronous Clock Mode Timing – PLD

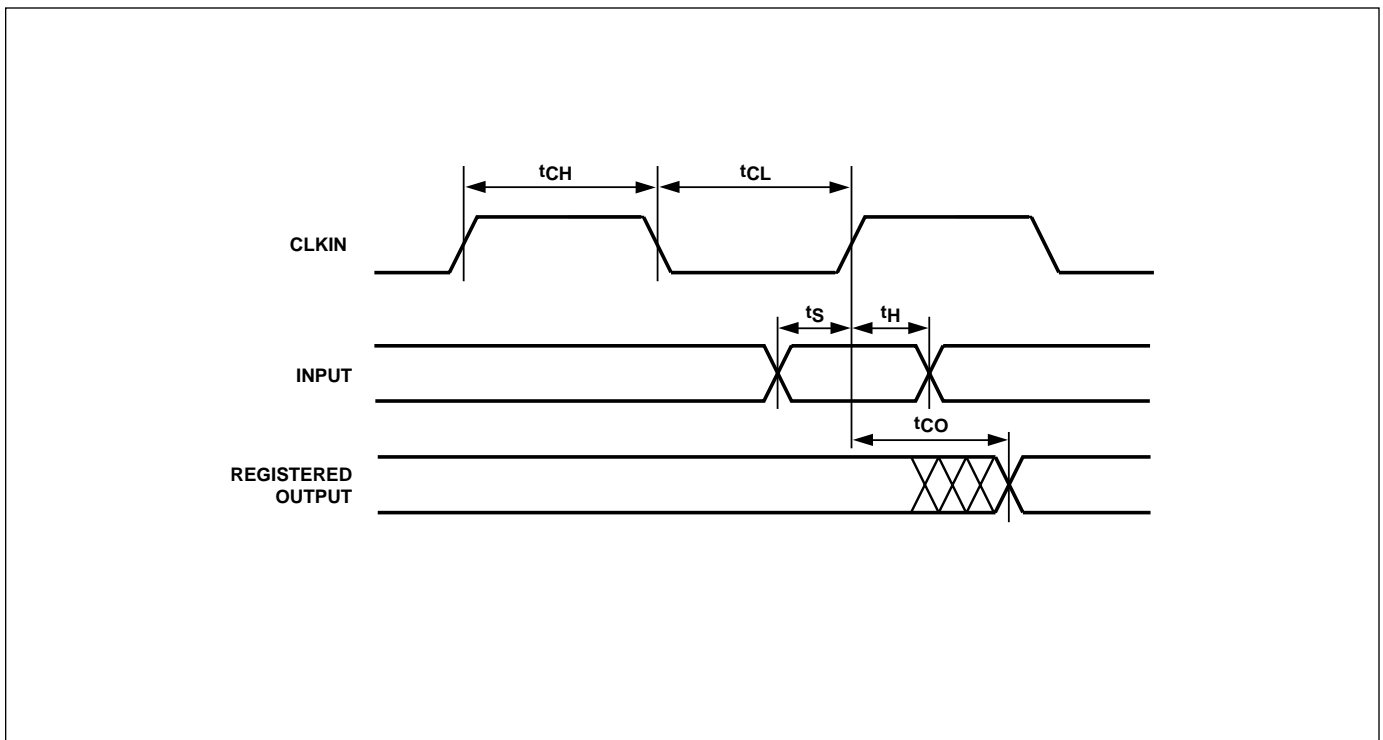


Figure 41. Asynchronous Clock Mode Timing (Product-Term Clock)

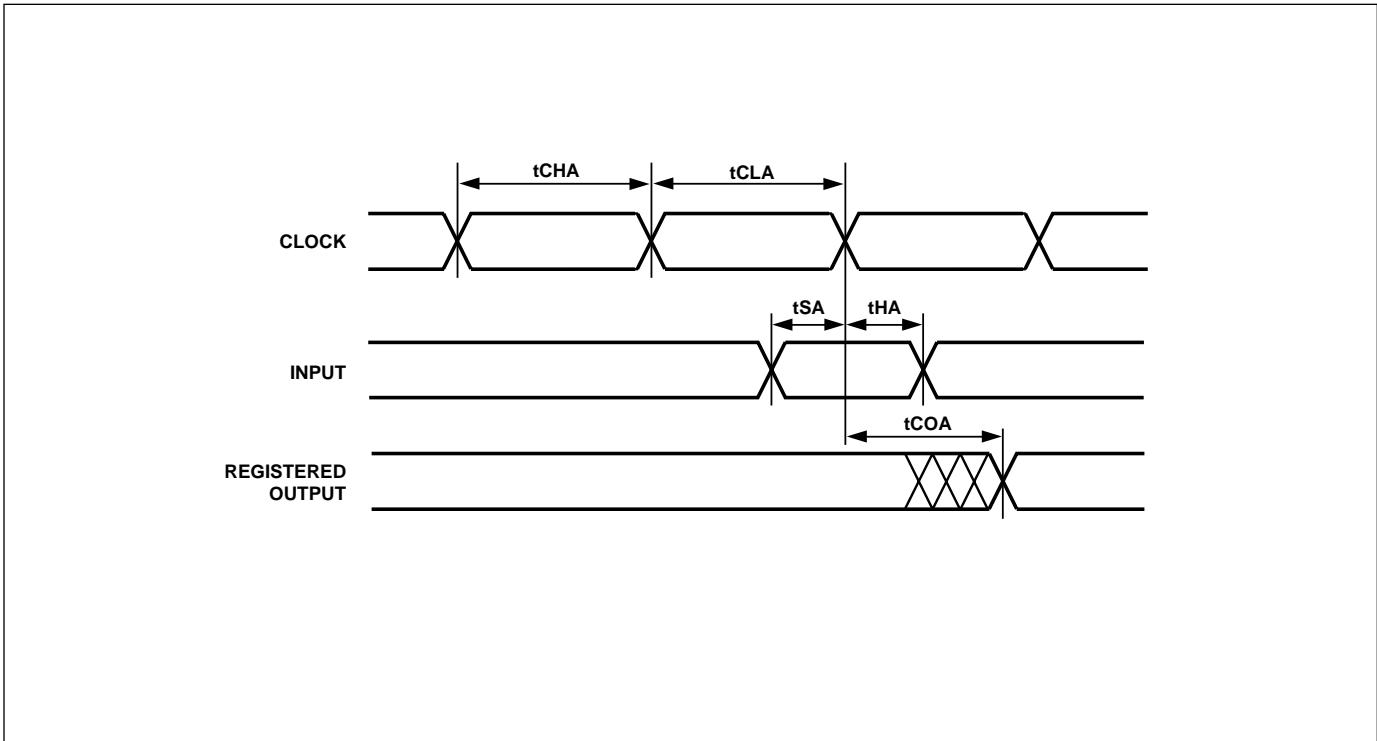


Figure 42. Input Micro↔Cell Timing (Product-Term Clock)

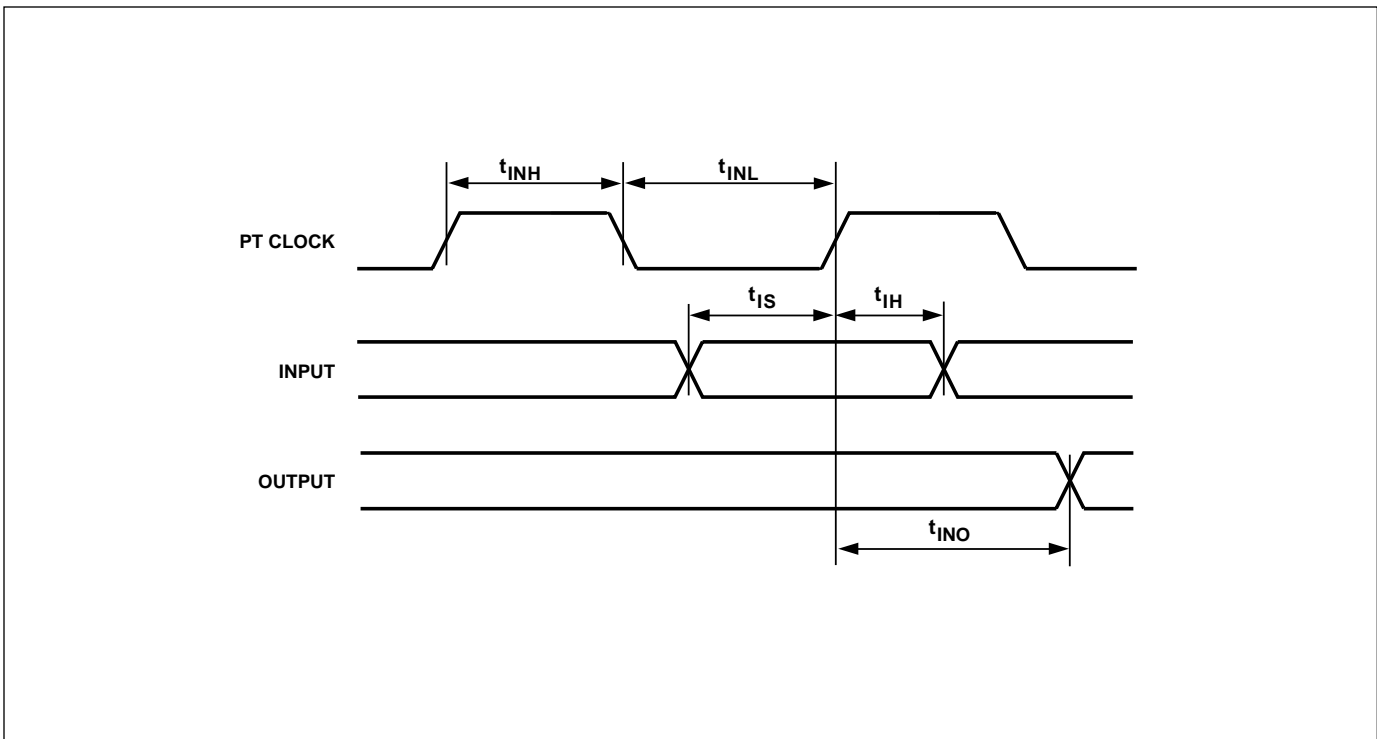


Figure 43. Input to Output Disable/Enable

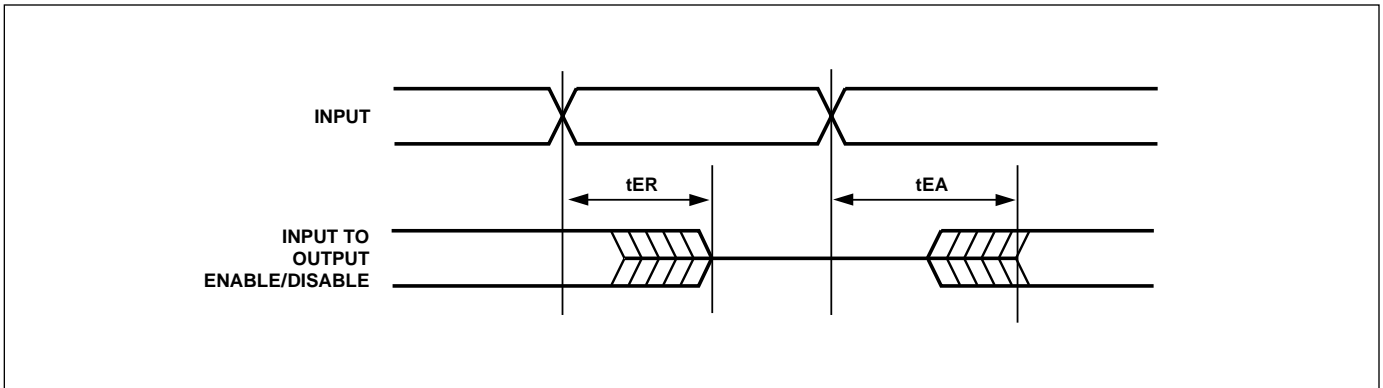


Figure 44. Asynchronous Reset/Preset

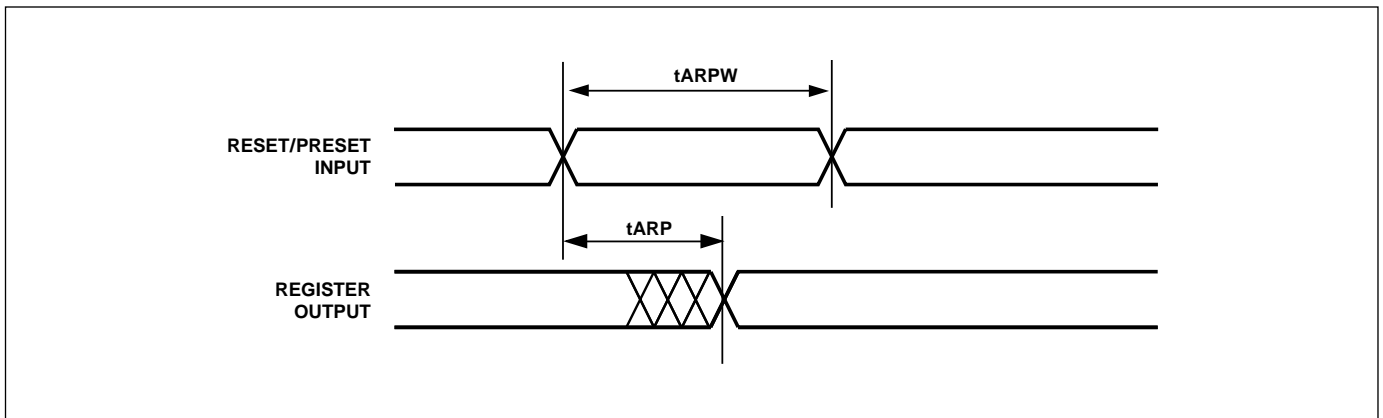


Figure 45. ISC Timing

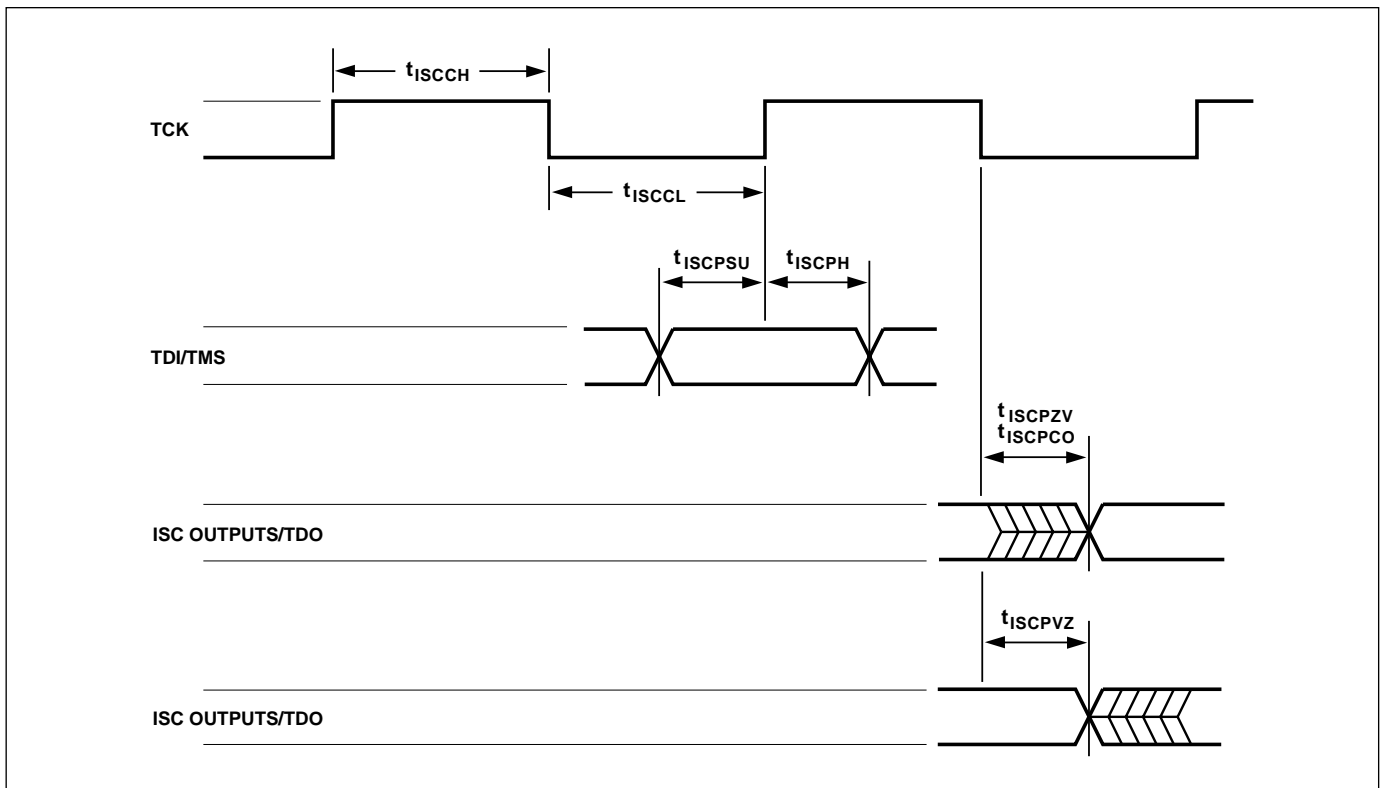


Figure 46. Reset Timing

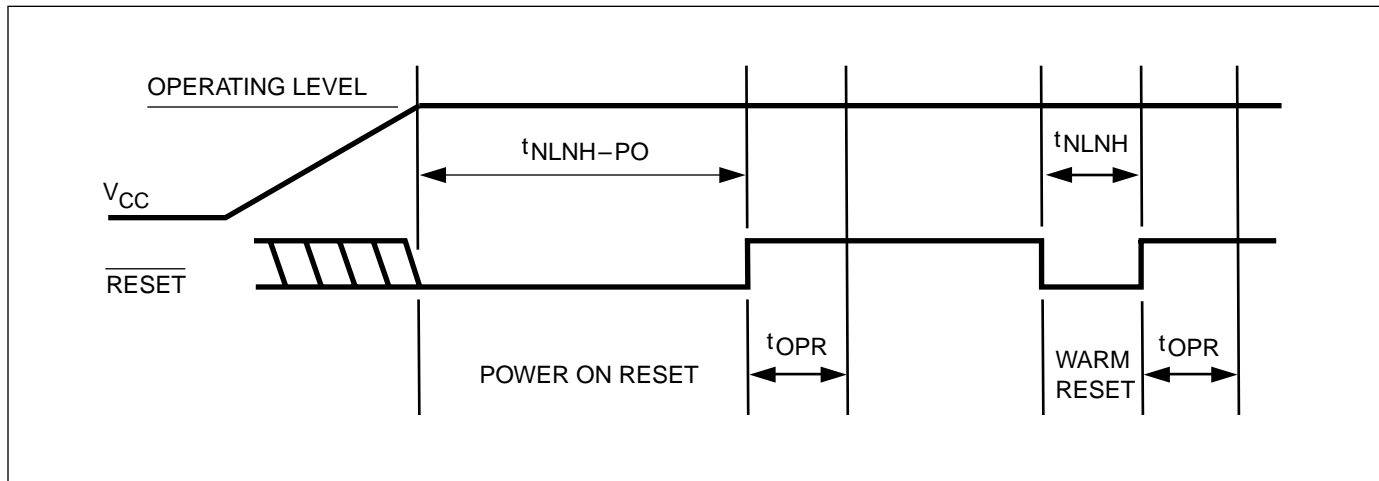


Figure 47. Key to Switching Waveforms

WAVEFORMS	INPUTS	OUTPUTS
	STEADY INPUT	STEADY OUTPUT
	MAY CHANGE FROM HI TO LO MAY CHANGE FROM LO TO HI	WILL BE CHANGING FROM HI TO LO WILL BE CHANGING LO TO HI
	DON'T CARE	CHANGING, STATE UNKNOWN
	OUTPUTS ONLY	CENTER LINE IS TRI-STATE

Pin Capacitance

$T_A = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$

Symbol	Parameter¹	Conditions	Typical²	Max	Unit
C_{IN}	Capacitance (for input pins only)	$V_{IN} = 0\text{ V}$	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	$V_{OUT} = 0\text{ V}$	8	12	pF
C_{VPP}	Capacitance (for CNTL2/ V_{PP})	$V_{PP} = 0\text{ V}$	18	25	pF

NOTES: 1. These parameters are only sampled and are not 100% tested.
 2. Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltages.

Figure 48.
AC Testing
Input/Output
Waveform

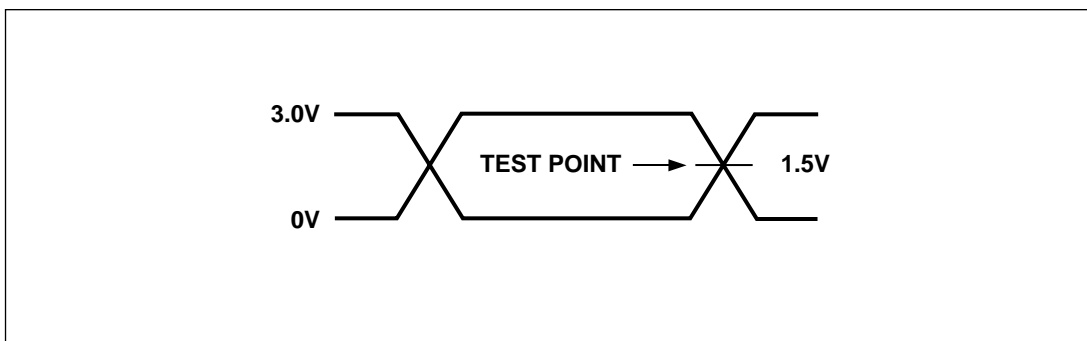
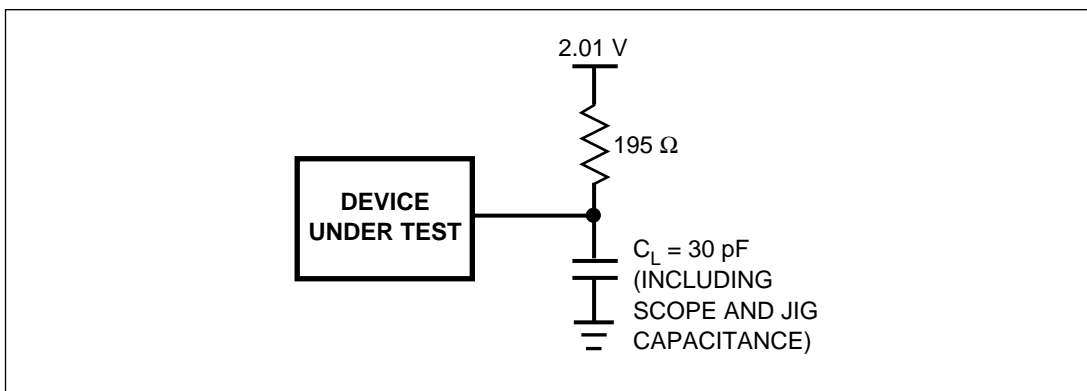


Figure 49.
AC Testing
Load Circuit



Programming

Upon delivery from WSI, the PSD813F device has all bits in the PLDs and memories in the “1” or high state. The configuration bits are in the “0” or low state. The code, configuration, and PLDs logic are loaded through the procedure of programming.

Information for programming the device is available directly from WSI. Please contact your local sales representative. (See the last page.)

PSD813F
Pin
Assignments

52-Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)

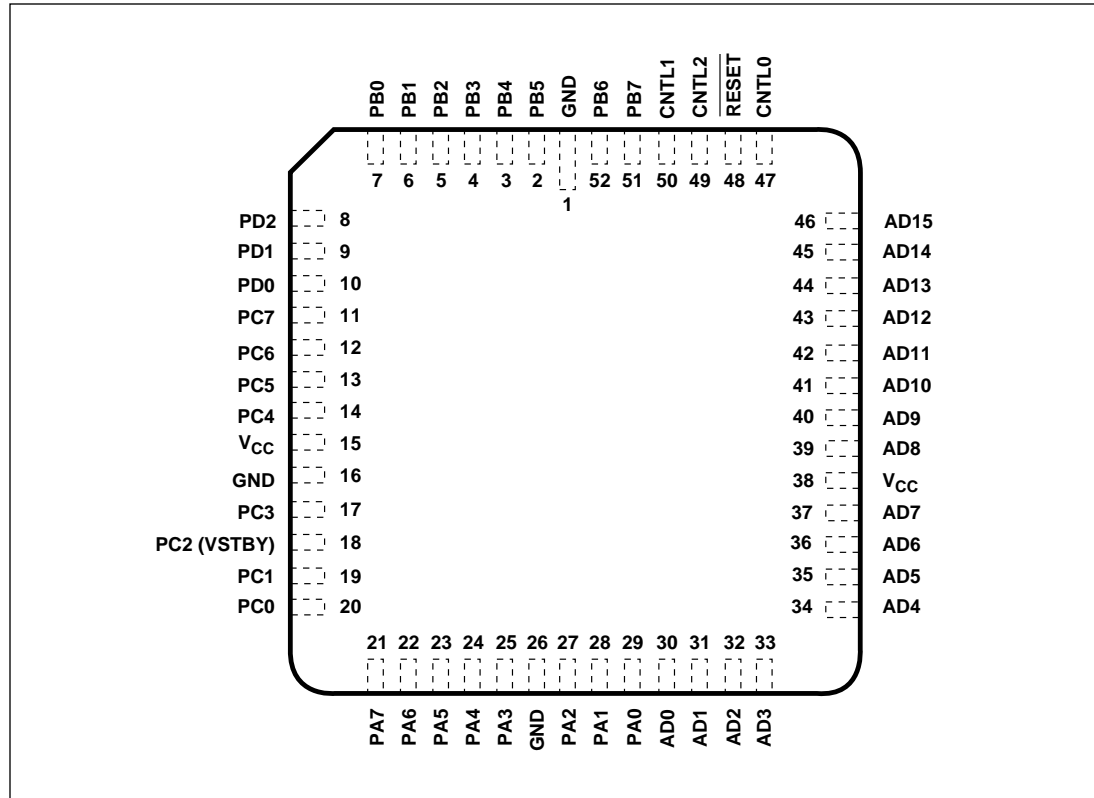
Pin No.	Pin Assignments	Pin No.	Pin Assignments
1	GND	27	PA2
2	PB5	28	PA1
3	PB4	29	PA0
4	PB3	30	AD0
5	PB2	31	AD1
6	PB1	32	AD2
7	PB0	33	AD3
8	PD2	34	AD4
9	PD1	35	AD5
10	PD0	36	AD6
11	PC7	37	AD7
12	PC6	38	V _{CC}
13	PC5	39	AD8
14	PC4	40	AD9
15	V _{CC}	41	AD10
16	GND	42	AD11
17	PC3	43	AD12
18	PC2 (VSTBY)	44	AD13
19	PC1	45	AD14
20	PC0	46	AD15
21	PA7	47	CNTL0
22	PA6	48	RESET
23	PA5	49	CNTL2
24	PA4	50	CNTL1
25	PA3	51	PB7
26	GND	52	PB6

PSD813F**Pin
Assignments
(cont.)****64-Pin Plastic Thin Quad Flatpack (TQFP) (Package Type U)**

Pin No.	Pin Assignments	Pin No.	Pin Assignments
1	PD2	33	AD3
2	PD1	34	AD4
3	PD0	35	AD5
4	PC7	36	AD6
5	PC6	37	AD7
6	PC5	38	V _{CC}
7	PC4	39	V _{CC}
8	V _{CC}	40	AD8
9	V _{CC}	41	AD9
10	GND	42	AD10
11	GND	43	AD11
12	PC3	44	AD12
13	PC2	45	AD13
14	PC1	46	AD14
15	PC0	47	AD15
16	N/C	48	CNTL0
17	N/C	49	N/C
18	N/C	50	RESET
19	PA7	51	CNTL2
20	PA6	52	CNTL1
21	PA5	53	PB7
22	PA4	54	PB6
23	PA3	55	GND
24	GND	56	GND
25	GND	57	PB5
26	PA2	58	PB4
27	PA1	59	PB3
28	PA0	60	PB2
29	AD0	61	PB1
30	AD1	62	PB0
31	N/C	63	N/C
32	AD2	64	N/C

**PSD813F
Package
Information**

**Figure 50. Drawing J7 – 52-Pin Plastic Leaded Chip Carrier (PLDCC)
(Package Type J)**



**Figure 51. Drawing U4 – 64-Pin Plastic Thin Quad Flatpack (TQFP)
(Package Type U)**

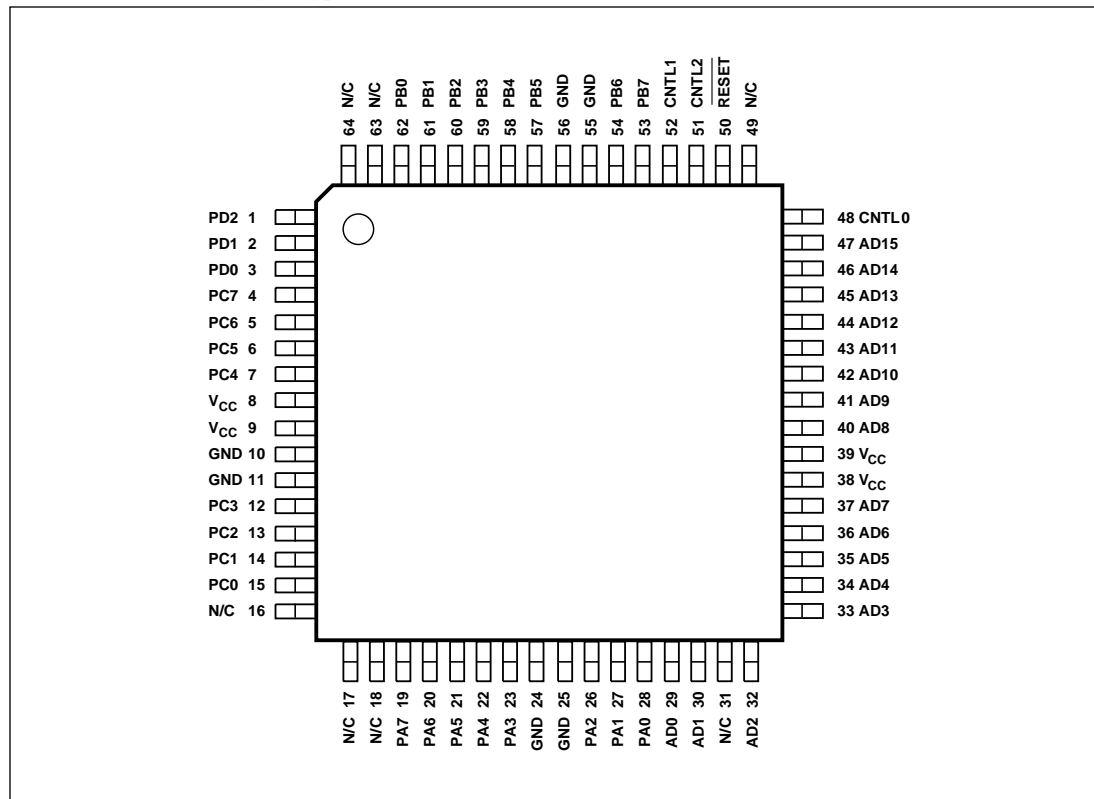
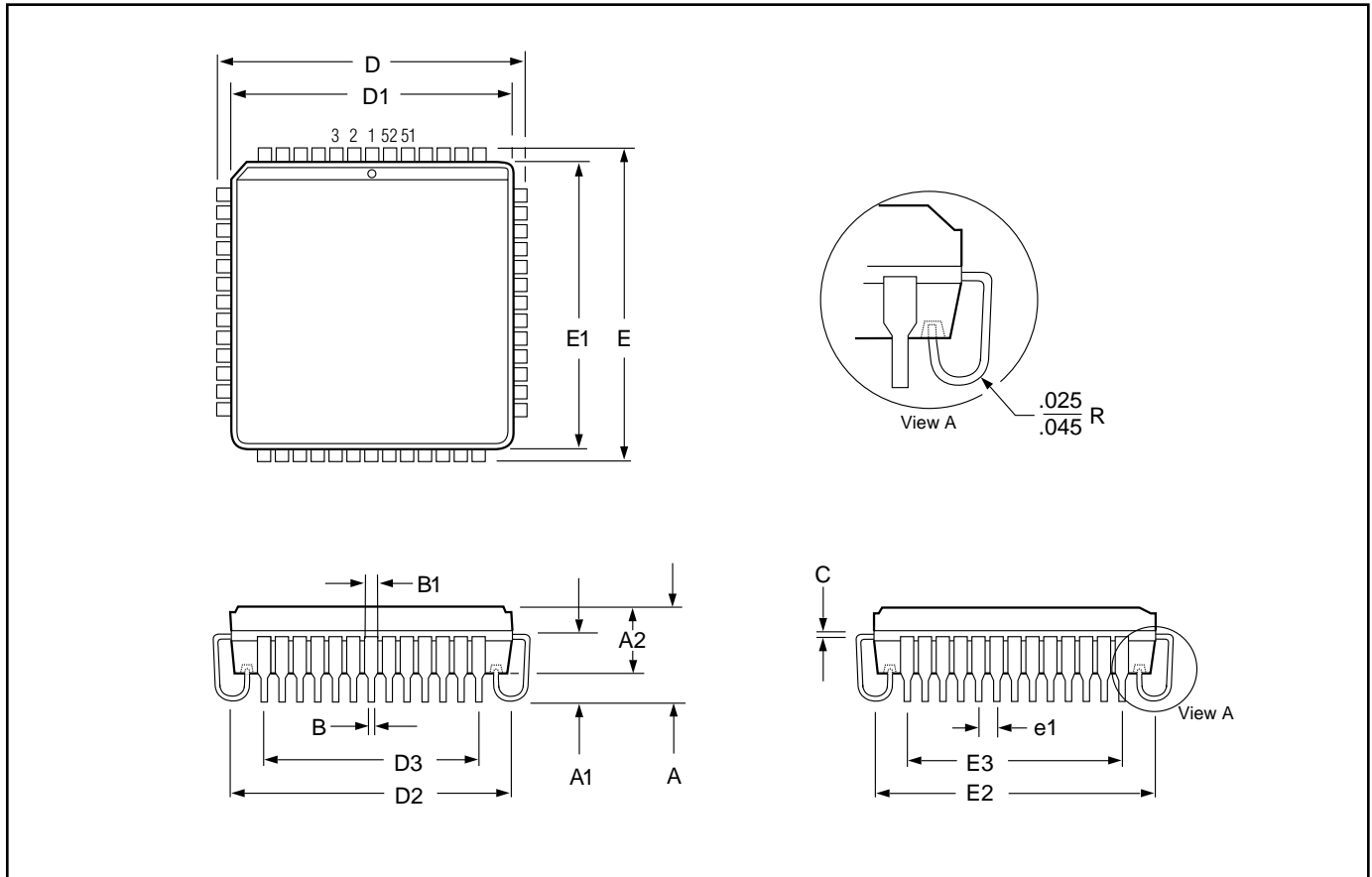


Figure 50A.
Drawing J7 – 52-Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)



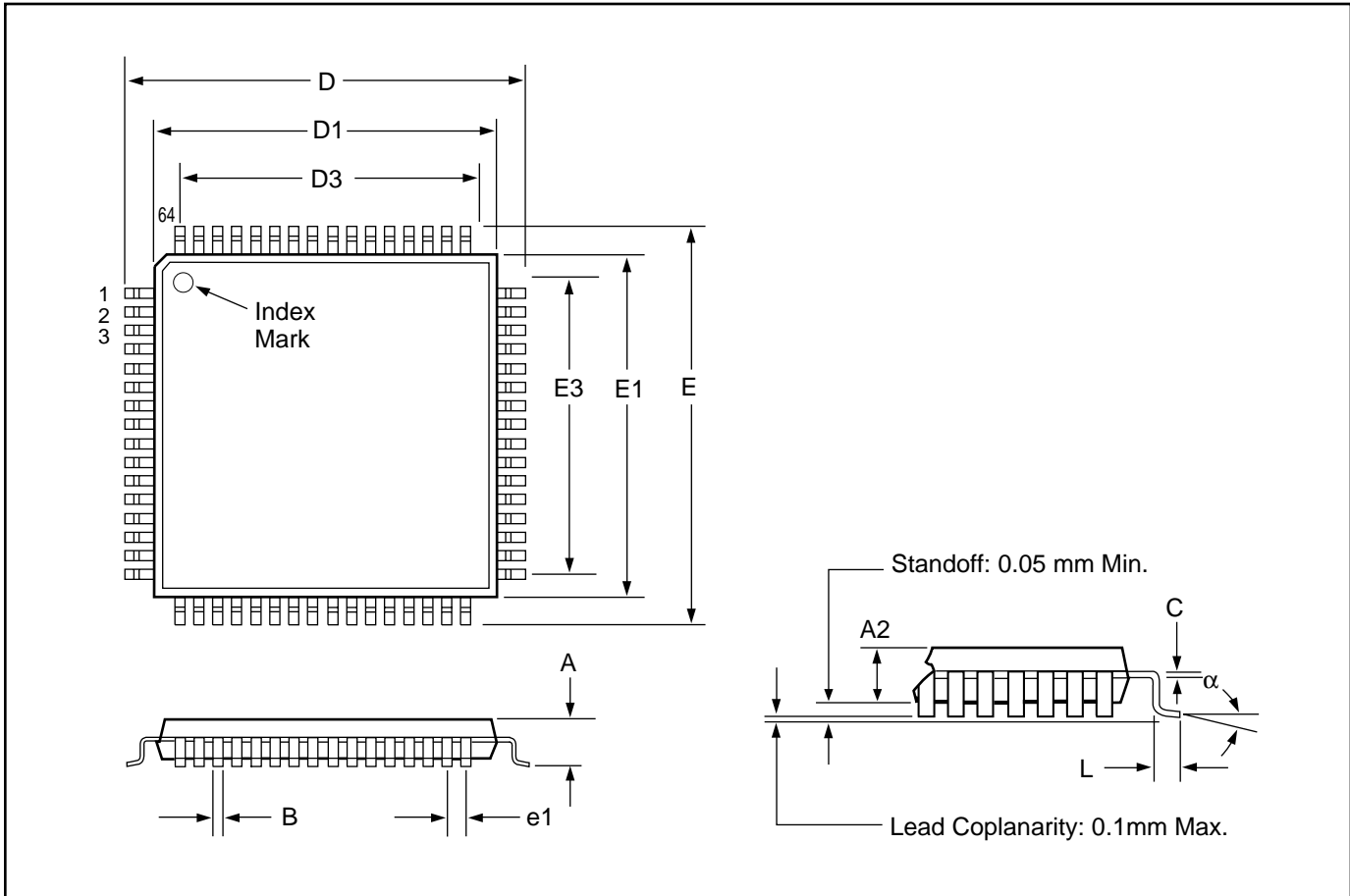
Family: Plastic Leaded Chip Carrier

Symbol	Millimeters		Notes	Inches		Notes
	Min	Max		Min	Max	
A	4.19	4.57		0.165	0.180	
A1	2.54	2.79		0.100	0.110	
A2	3.66	3.86		0.144	0.152	
B	0.33	0.53		0.013	0.021	
B1	0.66	0.81		0.026	0.032	
C	0.246	0.261		0.0097	0.0103	
D	19.94	20.19		0.785	0.795	
D1	19.05	19.15		0.750	0.754	
D2	17.53	18.54		0.690	0.730	
D3	15.24		Reference	0.600		Reference
E	19.94	20.19		0.785	0.795	
E1	19.05	19.15		0.750	0.754	
E2	17.53	18.54		0.690	0.730	
E3	15.24		Reference	0.600		Reference
e1	1.27		Reference	0.050		Reference
N	52			52		

020197R1



Figure 51A.
Drawing U4 – 64-Pin Plastic Thin Quad Flatpack (TQFP) (Package Type U)



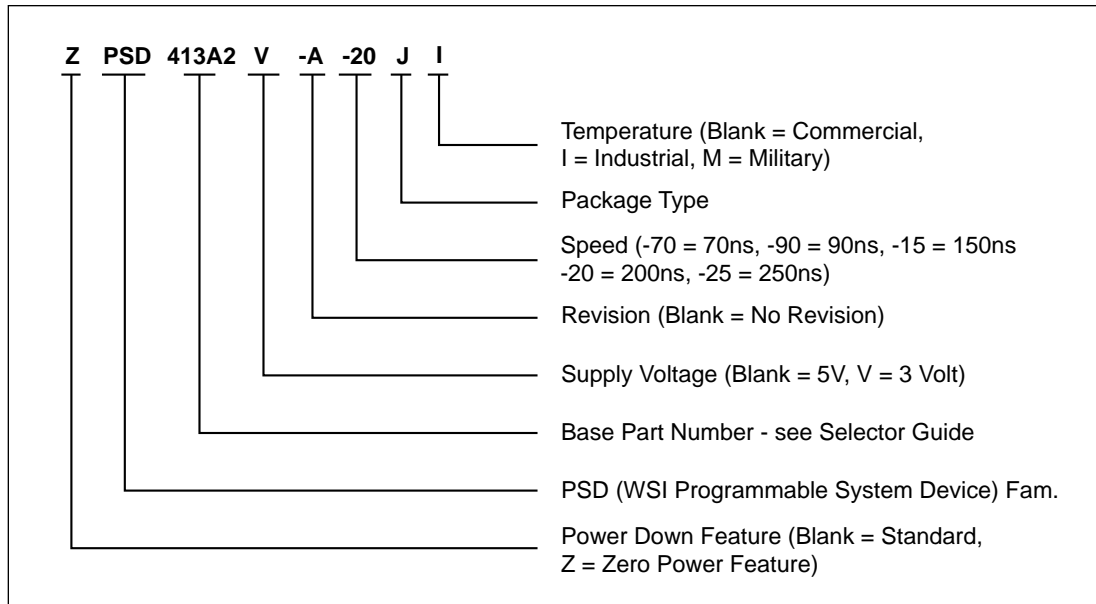
Family: Plastic Thin Quad Flatpack (TQFP)

Symbol	Millimeters		Notes	Inches		Notes
	Min	Max		Min	Max	
α	0°	8°		0°	8°	
A	–	1.60		–	0.063	
A2	1.35	1.45		0.053	0.057	
B	0.30	0.40	Reference	0.012	0.016	
C		0.17			0.007	
D	15.95	16.05		0.628	0.632	
D1	13.95	14.05		0.549	0.553	
D3	12.00		Reference	0.472		Reference
E	15.95	16.05		0.628	0.632	
E1	13.95	14.05		0.549	0.553	
E3	12.00		Reference	0.472		Reference
e1	0.80		Reference	0.031		Reference
L	0.50	0.75		0.019	0.030	
N	64			64		

060198R0



Part Number Construction



Ordering Information

Part Number	Speed (ns)	Package Type	Operating Temperature Range
PSD813F1-90J	90	52 Pin PLDCC	Comm'l
PSD813F1-90JI	90	52 Pin PLDCC	Industrial
PSD813F1-90U	90	64 Pin TQFP	Comm'l
PSD813F1-90UI	90	64 Pin TQFP	Industrial
PSD813F1-12J	120	52 Pin PLDCC	Comm'l
PSD813F1-12JI	120	52 Pin PLDCC	Industrial
PSD813F1-12U	120	64 Pin TQFP	Comm'l
PSD813F1-12UI	120	64 Pin TQFP	Industrial
PSD813F1-15J	150	52 Pin PLDCC	Comm'l
PSD813F1-15JI	150	52 Pin PLDCC	Industrial
PSD813F1-15U	150	64 Pin TQFP	Comm'l
PSD813F1-15UI	150	64 Pin TQFP	Industrial
PSD813F2-90J	90	52 Pin PLDCC	Comm'l
PSD813F2-90JI	90	52 Pin PLDCC	Industrial
PSD813F2-90U	90	64 Pin TQFP	Comm'l
PSD813F2-90UI	90	64 Pin TQFP	Industrial
PSD813F2-12J	120	52 Pin PLDCC	Comm'l
PSD813F2-12JI	120	52 Pin PLDCC	Industrial
PSD813F2-12U	120	64 Pin TQFP	Comm'l
PSD813F2-12UI	120	64 Pin TQFP	Industrial
PSD813F2-15J	150	52 Pin PLDCC	Comm'l
PSD813F2-15JI	150	52 Pin PLDCC	Industrial
PSD813F2-15U	150	64 Pin TQFP	Comm'l
PSD813F2-15UI	150	64 Pin TQFP	Industrial



**Ordering
Information**

Part Number	Speed (ns)	Package Type	Operating Temperature Range
PSD813F3-90J	90	52 Pin PLDCC	Comm'l
PSD813F3-90JI	90	52 Pin PLDCC	Industrial
PSD813F3-90U	90	64 Pin TQFP	Comm'l
PSD813F3-90UI	90	64 Pin TQFP	Industrial
PSD813F3-12J	120	52 Pin PLDCC	Comm'l
PSD813F3-12JI	120	52 Pin PLDCC	Industrial
PSD813F3-12U	120	64 Pin TQFP	Comm'l
PSD813F3-12UI	120	64 Pin TQFP	Industrial
PSD813F3-15J	150	52 Pin PLDCC	Comm'l
PSD813F3-15JI	150	52 Pin PLDCC	Industrial
PSD813F3-15U	150	64 Pin TQFP	Comm'l
PSD813F3-15UI	150	64 Pin TQFP	Industrial
PSD813F4-90J	90	52 Pin PLDCC	Comm'l
PSD813F4-90JI	90	52 Pin PLDCC	Industrial
PSD813F4-90U	90	64 Pin TQFP	Comm'l
PSD813F4-90UI	90	64 Pin TQFP	Industrial
PSD813F4-12J	120	52 Pin PLDCC	Comm'l
PSD813F4-12JI	120	52 Pin PLDCC	Industrial
PSD813F4-12U	120	64 Pin TQFP	Comm'l
PSD813F4-12UI	120	64 Pin TQFP	Industrial
PSD813F4-15J	150	52 Pin PLDCC	Comm'l
PSD813F4-15JI	150	52 Pin PLDCC	Industrial
PSD813F4-15U	150	64 Pin TQFP	Comm'l
PSD813F4-15UI	150	64 Pin TQFP	Industrial
PSD813F5-90J	90	52 Pin PLDCC	Comm'l
PSD813F5-90JI	90	52 Pin PLDCC	Industrial
PSD813F5-90U	90	64 Pin TQFP	Comm'l
PSD813F5-90UI	90	64 Pin TQFP	Industrial
PSD813F5-12J	120	52 Pin PLDCC	Comm'l
PSD813F5-12JI	120	52 Pin PLDCC	Industrial
PSD813F5-12U	120	64 Pin TQFP	Comm'l
PSD813F5-12UI	120	64 Pin TQFP	Industrial
PSD813F5-15J	150	52 Pin PLDCC	Comm'l
PSD813F5-15JI	150	52 Pin PLDCC	Industrial
PSD813F5-15U	150	64 Pin TQFP	Comm'l
PSD813F5-15UI	150	64 Pin TQFP	Industrial

**Ordering
Information**

Part Number	Speed (ns)	Package Type	Operating Temperature Range
ZPSD813F1-90J	90	52 Pin PLDCC	Comm'l
ZPSD813F1-90JI	90	52 Pin PLDCC	Industrial
ZPSD813F1-90U	90	64 Pin TQFP	Comm'l
ZPSD813F1-90UI	90	64 Pin TQFP	Industrial
ZPSD813F1-12J	120	52 Pin PLDCC	Comm'l
ZPSD813F1-12JI	120	52 Pin PLDCC	Industrial
ZPSD813F1-12U	120	64 Pin TQFP	Comm'l
ZPSD813F1-12UI	120	64 Pin TQFP	Industrial
ZPSD813F1-15J	150	52 Pin PLDCC	Comm'l
ZPSD813F1-15JI	150	52 Pin PLDCC	Industrial
ZPSD813F1-15U	150	64 Pin TQFP	Comm'l
ZPSD813F1-15UI	150	64 Pin TQFP	Industrial
ZPSD813F1V-15J	150	52 Pin PLDCC	Comm'l
ZPSD813F1V-15U	150	64 Pin TQFP	Industrial
ZPSD813F1V-20J	200	52 Pin PLDCC	Comm'l
ZPSD813F1V-20U	200	64 Pin TQFP	Comm'l
ZPSD813F1V-20JI	200	52 Pin PLDCC	Industrial
ZPSD813F1V-20UI	200	64 Pin TQFP	Industrial
ZPSD813F2-90J	90	52 Pin PLDCC	Comm'l
ZPSD813F2-90JI	90	52 Pin PLDCC	Industrial
ZPSD813F2-90U	90	64 Pin TQFP	Comm'l
ZPSD813F2-90UI	90	64 Pin TQFP	Industrial
ZPSD813F2-12J	120	52 Pin PLDCC	Comm'l
ZPSD813F2-12JI	120	52 Pin PLDCC	Industrial
ZPSD813F2-12U	120	64 Pin TQFP	Comm'l
ZPSD813F2-12UI	120	64 Pin TQFP	Industrial
ZPSD813F2-15J	150	52 Pin PLDCC	Comm'l
ZPSD813F2-15JI	150	52 Pin PLDCC	Industrial
ZPSD813F2-15U	150	64 Pin TQFP	Comm'l
ZPSD813F2-15UI	150	64 Pin TQFP	Industrial
ZPSD813F2V-15J	150	52 Pin PLDCC	Comm'l
ZPSD813F2V-15U	150	64 Pin TQFP	Comm'l
ZPSD813F2V-20J	200	52 Pin PLDCC	Comm'l
ZPSD813F2V-20U	200	64 Pin TQFP	Comm'l
ZPSD813F2V-20JI	200	52 Pin PLDCC	Industrial
ZPSD813F2V-20UI	200	64 Pin TQFP	Industrial
ZPSD813F3-90J	90	52 Pin PLDCC	Comm'l
ZPSD813F3-90JI	90	52 Pin PLDCC	Industrial
ZPSD813F3-90U	90	64 Pin TQFP	Comm'l
ZPSD813F3-90UI	90	64 Pin TQFP	Industrial
ZPSD813F3-12J	120	52 Pin PLDCC	Comm'l
ZPSD813F3-12JI	120	52 Pin PLDCC	Industrial
ZPSD813F3-12U	120	64 Pin TQFP	Comm'l
ZPSD813F3-12UI	120	64 Pin TQFP	Industrial
ZPSD813F3-15J	150	52 Pin PLDCC	Comm'l
ZPSD813F3-15JI	150	52 Pin PLDCC	Industrial
ZPSD813F3-15U	150	64 Pin TQFP	Comm'l
ZPSD813F3-15UI	150	64 Pin TQFP	Industrial

**Ordering
Information**

Part Number	Speed (ns)	Package Type	Operating Temperature Range
ZPSD813F3V-15J	150	52 Pin PLDCC	Comm'l
ZPSD813F3V-15U	150	64 Pin TQFP	Comm'l
ZPSD813F3V-20J	200	52 Pin PLDCC	Comm'l
ZPSD813F3V-20U	200	64 Pin TQFP	Comm'l
ZPSD813F3V-20JI	200	52 Pin PLDCC	Industrial
ZPSD813F3V-20UI	200	64 Pin TQFP	Industrial
ZPSD813F4-90J	90	52 Pin PLDCC	Comm'l
ZPSD813F4-90JI	90	52 Pin PLDCC	Industrial
ZPSD813F4-90U	90	64 Pin TQFP	Comm'l
ZPSD813F4-90UI	90	64 Pin TQFP	Industrial
ZPSD813F4-12J	120	52 Pin PLDCC	Comm'l
ZPSD813F4-12JI	120	52 Pin PLDCC	Industrial
ZPSD813F4-12U	120	64 Pin TQFP	Comm'l
ZPSD813F4-12UI	120	64 Pin TQFP	Industrial
ZPSD813F4-15J	150	52 Pin PLDCC	Comm'l
ZPSD813F4-15JI	150	52 Pin PLDCC	Industrial
ZPSD813F4-15U	150	64 Pin TQFP	Comm'l
ZPSD813F4-15UI	150	64 Pin TQFP	Industrial
ZPSD813F4V-15J	150	52 Pin PLDCC	Comm'l
ZPSD813F4V-15U	150	64 Pin TQFP	Comm'l
ZPSD813F4V-20J	200	52 Pin PLDCC	Comm'l
ZPSD813F4V-20U	200	64 Pin TQFP	Comm'l
ZPSD813F4V-20JI	200	52 Pin PLDCC	Industrial
ZPSD813F4V-20UI	200	64 Pin TQFP	Industrial
ZPSD813F5-90J	90	52 Pin PLDCC	Comm'l
ZPSD813F5-90JI	90	52 Pin PLDCC	Industrial
ZPSD813F5-90U	90	64 Pin TQFP	Comm'l
ZPSD813F5-90UI	90	64 Pin TQFP	Industrial
ZPSD813F5-12J	120	52 Pin PLDCC	Comm'l
ZPSD813F5-12JI	120	52 Pin PLDCC	Industrial
ZPSD813F5-12U	120	64 Pin TQFP	Comm'l
ZPSD813F5-12UI	120	64 Pin TQFP	Industrial
ZPSD813F5-15J	150	52 Pin PLDCC	Comm'l
ZPSD813F5-15JI	150	52 Pin PLDCC	Industrial
ZPSD813F5-15U	150	64 Pin TQFP	Comm'l
ZPSD813F5-15UI	150	64 Pin TQFP	Industrial
ZPSD813F5V-15J	150	52 Pin PLDCC	Comm'l
ZPSD813F5V-15U	150	64 Pin TQFP	Comm'l
ZPSD813F5V-20J	200	52 Pin PLDCC	Comm'l
ZPSD813F5V-20U	200	64 Pin TQFP	Comm'l
ZPSD813F5V-20JI	200	52 Pin PLDCC	Industrial
ZPSD813F5V-20UI	200	64 Pin TQFP	Industrial

Temporary Exceptions to Specifications

The following information describes exceptions to specifications contained in this data sheet. These exceptions will be corrected in future releases of PSD813F products. Please note the device markings for which these exceptions apply.

For PSD813F devices marked “ES3” on the topside, the following specification exceptions apply.

1. The “TURBO OFF” adder parameter has changed (5V ZPSD813Fx devices only).

Normal Operation – When the 5V ZPSD813F device is operated in non-turbo mode, the amount of propagation delay in the CPLD, and the memory access times, are increased by the “TURBO OFF” adder parameter of 10 nsec, as listed throughout the AC/DC Parameter section.

Discrepancy – The value of the “TURBO OFF” adder for 5V ZPSD813F devices has increased from 10 nsec to 15 nsec. When viewing the 5V AC/DC Parameter specifications, replace any occurrence of 10 nsec for the “TURBO OFF” adder parameter with 15 nsec.

2. The User Code feature of IEEE 1149.1 is not supported via the PSD JTAG channel. (PSD813Fx, ZPSD813Fx, and ZPSD813FxV devices)

Normal Operation – The PSD813F provides 32 bits of non-volatile memory (User Code), to allow the user to store information. Typical uses are product ID, product software revision information, etc. Read and Write access is available through a stand-alone device programmer (like PSDpro) or the IEEE 1149.1 JTAG channel. The microcontroller does not have access.

Discrepancy – The user code information cannot be accessed through the PSD JTAG channel. However, it can be accessed using a device programmer (like PSDpro).

3. Initial enabling of Software Data Protect (SDP) mode requires writing data to a reserved memory space. (PSD813F1 and ZPSD813F1 only)

Normal Operation – The Software Data Protect (SDP) mode for EEPROM can be set when the microcontroller (MCU) writes a three byte command sequence to the EEPROM per Table 9. Once SDP mode is set, any further writes to EEPROM must be preceded by these same three command bytes to “unlock” the EEPROM per Figure 3. This offers data protection much like that of flash memory.

SDP mode may be enabled when the MCU initializes the system, and left on all the time for maximum protection. Alternately, SDP mode may be disabled before writing blocks of data to EEPROM, and enabled after writing. This method still offers good protection without the time penalty of writing AAh, 55h, A0h before each set of data.

The MCU can enable SDP mode by either of two methods:

- 1) write three command bytes and no data (AAh,55h, A0h) as shown in table 9.
- 2) write three command bytes followed by one or more actual data bytes to be written into the EEPROM (AAh, 55h, A0h, data1, data2, data64), also shown in Table 9

SDP mode is controlled by a programmable non-volatile (NVM) bit inside the PSD. Once SDP mode is enabled, it will stay enabled until the MCU or a device programmer erases the NVM bit. PSD813F devices are shipped from Waferscale with SDP mode not enabled.

Temporary Exceptions to Specifications (cont.)

Discrepancy – Anytime the MCU changes the state of SDP mode from disabled to enabled, it must write three command bytes (AAh, 55h, A0h), then write a single dummy byte to a reserved address space of 128 bytes in length. The dummy byte can be any pattern. The MCU should not use method 1 or method 2 shown above to enable SDP mode.

This is only necessary when going from SDP mode disabled to SDP mode enabled. If SDP mode is already enabled (enabled from the MCU or a stand-alone device programmer), then the command sequences in Table 9 of the data sheets may be used to write byte(s) into the EEPROM (no dummy write to reserved space is needed). If the MCU disables SDP mode, then enables SDP mode again, a dummy write to the reserved address space is needed to get SDP mode enabled again.

Interim Solution –

Reserve an address range 128 bytes in length within an unused portion of EEPROM. This 128-byte space can be in any of the four EEPROM segments, and must begin on a 128-byte address boundary.

To enable SDP mode (only after previously being disabled), the MCU must write the command sequence AAh, 55h, A0h to any valid EEPROM sector at addresses X555h, XAAAh, X555h respectively. But then it must write a single dummy byte to the first location within the reserved 128-byte address space. Example (you don't have to use these exact addresses or dummy byte value):

AAh >> 8555h

55h >> 8AAAh

A0h >> 8555h Just like data PSD813F sheet so far.

EEh >> 8080h Dummy byte EEh is written to reserved address block starting at 8080h (block is from 8080h to 80FFh).

From this point forward, SDP mode is enabled, until disabled by the MCU or a device programmer.

If you cannot locate 128 bytes of unused space in your EEPROM memory map, then you can use populated EEPROM memory. However, you must first read the existing 128 bytes in the reserved space, enable SDP mode with the single dummy write, then write the original 128 bytes back into the reserved address space.

**Document
Revisions**

Date	Revision Reason	Data Sheet Changes
10 NOV 97	PSD813F Initial release	–
1 JUL 98	Data Sheet Updated	Minor changes
3 JUL 98	Data Sheet Updated	Minor changes
22 SEP 98	Data Sheet Updated	Page 18 – C7h changed to E3h. Page 27 – C7h changed to E3h, C1h changed to E4h. Page 14 – EEPROM changed to EPROM
13 JAN 99	Data Sheet Updated	<p>Major changes – Reorganization of information updated and expanded text for clarification and readability. Changes to technical data and specifications as well. Please disregard previous versions.</p> <p>Following is a listing of major parameters and areas that have changed, added, or deleted:</p> <p>Page 2: changed Standby reference, added Erase/Write cycle info</p> <p>Page 17: added notes 3 and 4</p> <p>Page 35: added text for “blocking bits” in PMMR2</p> <p>Page 69: deleted Sleep Mode feature</p> <p>Page 71: major changes to Figs 31 and 32</p> <p>Page 72: deleted register PMMR1</p> <p>Page 76: new info on JTAG invocation</p> <p>Page 78: changed V_{CC} tolerance, Ind Temp</p> <p>Page 79: changed y-axis in Fig 34</p> <p>Page 80: changed y-axis in Fig 34a</p> <p>Page 82: added V_{OH1}, deleted Sleep Mode from i_{SB}</p> <p>Page 84: changed t_{ARPW}</p> <p>Page 85: changed t_{HA}, t_{CHA}, t_{COA}, t_{IS}, t_{IH}</p> <p>Page 87: added column for Turbo Off, changed t_{AVQV}, t_{RHQX}, t_{RLRH}</p> <p>Page 88: changed t_{WLWH}, t_{WLMV}, t_{WHQV2}, t_{VCS}, t_{DVMV}</p> <p>Page 89: added column for Turbo Off, changed $t_{AVQV(PA)}$, $t_{SLQV(PA)}$, $t_{DVQV(PA)}$, $t_{WLQV(PA)}$</p> <p>Page 90: deleted t_{LVDV1}, t_{PD5}, t_{BVBH}, t_{BXBL}, added note for reset while prog/erase</p> <p>Page 91: added note 2</p> <p>Page 92: added V_{OH1}, deleted Sleep Mode from i_{SB}</p> <p>Page 93: changed t_{ARPW}</p> <p>Page 94: changed t_{HA}, t_{CHA}, t_{COA}, t_{IS}, t_{IH}</p> <p>Page 96: added column for Turbo Off, changed t_{AVQV}</p> <p>Page 97: changed t_{DVWH}, t_{WHDX}, t_{WLWH}, t_{WLMV}, t_{Q7VQV}, changed t_{VCS}, t_{DVMV}, t_{AVPV}</p>

**Document
Revisions
(cont.)**

Date	Revision Reason	Data Sheet Changes
13 JAN 99	Data Sheet Updated	Page 98: added column for Turbo Off, changed $t_{AVQV(PA)}$, $t_{SLQV(PA)}$, $t_{DVQV(PA)}$ Page 99: deleted t_{LVDV1} , t_{PD5} , changed t_{BVBH} , t_{BXBL} , added note for reset while prog/erase Page 100: added note 2 Page 108: changed C_{VPP}
29 JAN 99	Data Sheet Updated	Page 78: changed V_{CC} tolerance, Ind Temp
11 FEB 99	Data Sheet Updated	Pages 84, 85, 86, 88, 89, 90, 91, 92: added -12 to AC DC Specifications.
22 FEB 99	Data Sheet Updated	Page 117: added Selector Guide Page 118: added Part Number Construction and Ordering Information
12 MAY 99	Data Sheet Updated	Page 18: added notes to Table 9 Page 22: page write timeout value changed. Deleted reference to JTAG and SDP mode. Page 24: additional condition for writing to the OTP row. Page 29: additional condition for reading the Main Flash Identifier. Page 94 & 103: corrected spec for EEPROM page write cycle time. Changed spec for maximum EEPROM write time. Page 114: corrected signal name in Figure 51. Page 122: included exceptions to specifications for particular PSD devices.
18 June 99	Data Sheet	Page 94: added more ISC specifications: $t_{ISCCF-P}$, $t_{ISCCCH-P}$, $t_{ISCCCL-P}$ Page 95: changed V_{OH} specification. Page 99: changed t_{RLRH} , specification. Page 100: changed t_{LXAX} , t_{WLWH} , t_{WHPV} , t_{WLMV} , t_{DVMV} , specifications Page 101: changed $t_{DVQV(PA)}$, $t_{WLQV(PA)}$, specifications Page 103: added more ISC specifications: $t_{ISCCF-P}$, $t_{ISCCCH-P}$, $t_{ISCCCL-P}$ Page 122: changed specification exception number 3. Removed reference to ZPSD813FV since the exception does not apply to the 3 V PSD. Pages 79,95,96,97,99,100,101,103: changed the 3 V PSD V_{CC} range from 3 V \pm 10% to 2.7 V to 3.6 V.
9 Sept 99	Data Sheet Updated	Pages 32, 33: changed mixed mode equations. Pages 75, 93, 102, 110: changed \overline{RESET} requirement on power up. Page 84: added ISB to PSD813F DC spec. Page 94: changed ISC Port Set up Time.

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