REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
SHEET																								
REV																								
SHEET	22	23	24	25	26	27																		
REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21		

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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APPROVED BY: William K. Heckman

DRAWING APPROVAL DATE: 7 DECEMBER 1990

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS, 8-BIT MICROPROCESSOR CPU, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-86016

SHEET 1

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1693

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-86016	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	80C88	CMOS, 8-bit microprocessor CPU

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096"x.620"x.225"), dual-in-line package
X	C-5 (44-terminal, .662"x.662"x.120), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage	+8.0 V dc
Input, output, or I/O voltage applied	GND - 0.5 V dc to V_{CC} + 0.5 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Power dissipation (P_D);	
Case Q	1820 mW
Case X	806 mW
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Thermal resistance, junction-to-ambient (θ_{JA});	
Case Q	27.5°C/W
Case X	62.2°C/W
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroup	Limits		Unit
				Min	Max	
Low level input voltage 1/	V_{IL}	V_{CC} = 4.5 V	1,2,3		0.8	V
High level input voltage 1/	V_{IH}	V_{CC} = 5.5 V		2.2		
High level output voltage 2/	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -2.5 mA		3.0		
		V_{CC} = 4.5 V, I_{OH} = -100 uA		4.1		
Low level output voltage 2/	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 2.5 mA			0.4	
Operating power supply current	I_{CC}	V_{CC} = 5.5 V, f = 5.0 MHz, V_{IN} = 0 V or 5.5 V, Outputs open			50	mA
Standby power supply current 3/	I_{SB}	V_{CC} = 5.5 V, V_{IN} = 0 V or 5.5 V, Outputs unloaded			500	µA
Input leakage current 4/	I_{LI}	V_{CC} = 5.5 V, V_{IN} = 0 V or 5.5 V		-1.0	+1.0	
Output leakage current 5/	I_{LO}	V_{CC} = 5.5 V, V_{OUT} = 0 V			-10	
Clock input high voltage	V_{CH}	V_{CC} = 5.5 V		4.7		V
Clock input low voltage	V_{CL}	V_{CC} = 4.5 V			0.8	
Input current, bus hold high 6/	I_{BHH}	V_{IN} = 3.0 V, V_{CC} = 4.5 V and 5.5 V		-40	-400	µA
Input current, bus hold low 7/	I_{BHL}	V_{IN} = 0.8 V, V_{CC} = 4.5 V and 5.5 V		40	400	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroup	Limits		Unit
				Min	Max	
Input capacitance	C_{IN}	V_{CC} = 4.5 V to 5.5 V, all measurements are referenced to GND. See 4.3.1c	4		25	pF
Output capacitance	C_{OUT}					
I/O capacitance	$C_{I/O}$					
Functional testing		See 4.3.1d	7,8			
Clock cycle period	t_{CLCL}	C_L = 100 pF, V_{CC} = 4.5 V, 8/ f = 1.0 MHz, See figure 3	9,10,11	200		ns
Clock low time	t_{CLCH}			118		
Clock high time	t_{CHCL}			69		
Data in setup time	t_{DVCL}			30		
Data in hold time	t_{CLDX1}			10		
READY setup time into device	t_{RYHCH}			118		
READY hold time into device	t_{CHRYX}			30		
READY to inactive CLK 9/	t_{RYLCL}			-8.0		
HOLD setup time 10/	t_{HVCH}			35		
INTR, NMI, $\overline{TEST}$ setup time 11/	t_{INVCH}			30		
$\overline{RQ}/\overline{GT}$ setup time 12/	t_{GVCH}			30		
$\overline{RQ}$ hold time into device 01 12/ 13/	t_{CHGX}			40	$t_{CHCL}+10$	
Hold/hold acknowledge time	t_{CHSZ}				80	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroup	Limits		Unit
				Min	Max	
READY active to status passive 9/ 12/ 14/	t_{RYHSH}	C_L = 100 pF, V_{CC} = 4.5 V, f = 1.0 MHz, See figure 3 8/	9,10,11		110	ns
Status active delay 12/	t_{CHSV}			10	110	
Status inactive delay 12/ 14/	t_{CLSH}			10	130	
Address valid delay	t_{CLAV}			10	110	
Address hold time	t_{CLAX}			10		
Address float delay 15/	t_{CLAZ}			t_{CLAX}	80	
ALE width 10/	t_{LHLL}			t_{CLCH} -20		
ALE active delay 10/	t_{CLLH}				80	
ALE inactive delay 10/	t_{CHLL}				85	
Address hold time to ALE inactive 10/	t_{LLAX}			t_{CHCL} -10		
Data valid delay	t_{CLDV}			10	110	
Data hold time 15/	t_{CLDX2}			10		
Data hold time after $\overline{WR}$ 15/	t_{WHDX}			t_{CLCL} -30		
Control active delay 1 10/	t_{CVCTV}			10	110	
Control active delay 2 10/	t_{CHCTV}			10	110	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroup	Limits		Unit
				Min	Max	
Control inactive delay 10/	t_{CVCTX}	C_L = 100 pF, V_{CC} = 4.5 V, f = 1.0 MHz, See figure 3 8/	9,10,11	10	110	ns
Address float to $\overline{RD}$ active 10/ 15/	t_{AZRL}			0		
$\overline{RD}$ active delay	t_{CLRL}			10	165	
$\overline{RD}$ inactive delay	t_{CLRH}			10	150	
$\overline{RD}$ inactive to next address active	t_{RHAV}			t_{CLCL} -45		
HLDA valid delay 10/	t_{CLHAV}			10	160	
$\overline{GT}$ active delay 12/	t_{CLGL}			0	85	
GT inactive delay 12/	t_{CLGH}			0	85	
$\overline{WR}$ width 10/	t_{WLWH}			$2t_{CLCL}$ -60		
Address valid to ALE low 10/	t_{AVAL}			t_{CLCH} -60		
$\overline{RD}$ width	t_{RLRH}			$2t_{CLCL}$ -75		
Output rise time 15/	t_{OLOH}	From 0.8 to 2.0 V			15	
Output fall time 15/	t_{OHOL}	From 2.0 to 0.8 V			15	

1/ MN/$\overline{MX}$ is a strap option and should be held to V_{CC} or GND.

2/ Interchanging of force and sense conditions is permitted.

3/ Measured during clock high time after HALT instruction execution.

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TABLE I. Electrical performance characteristics - Continued.

4/ Applies to NMI, INTR, CLK, RESET, READY, $\overline{TEST}$, and MN/$\overline{MX}$ inputs only.

5/ I_{LO} should be measured by putting the pin in a high impedance state and then driving V_{OUT} to GND. Applies to $\overline{DEN}$, DT/$\overline{R}$, IO/$\overline{M}$, $\overline{WR}$, and $\overline{RD}$ outputs only.

6/ I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering to valid input high level of 3.0 V on the following inputs: AD0 thru AD7, A8 thru A15, A16/S3 thru A19/S6, $\overline{DEN}$, DT/$\overline{R}$, IO/$\overline{M}$, $\overline{WR}$, HLDA, HOLD, $\overline{RD}$, $\overline{SSO}$.

7/ I_{BHL} should be measured after lowering V_{IN} to GND and then raising to valid input low level of 0.8 V on the following inputs: AD0 thru AD7, A8 thru A15, and A16/S3 thru A19/S6.

8/ AC tests apply for both minimum and maximum mode system timing unless otherwise specified.

9/ Applies only to T2 state (8.0 ns into T3).

10/ Applies to minimum mode timing only.

11/ Setup requirement for asynchronous signal only to guaranteed recognition at next clock.

12/ Applies to maximum mode timing only.

13/ Device 01 actively pulls the $\overline{RG}$/$\overline{GT}$ pin to a logic one on the following clock cycle.

14/ Status lines return to their inactive (logic one) state after CLK goes low and READY goes high.

15/ If not tested, shall be guaranteed to the limits specified in table I.

Device type	01				
Case outline	Q	X	Case outline	Q	X
Terminal number	Terminal symbol		Terminal number	Terminal symbol	
1	GND	NC	23	$\overline{TEST}$	NC
2	A14	GND	24	$\overline{INTA}$(QS1)	RESET
3	A13	A14	25	ALE(QS0)	READY
4	A12	A13	26	$\overline{DEN}$($\overline{S0}$)	$\overline{TEST}$
5	A11	A12	27	DT/$\overline{R}$($\overline{SI}$)	$\overline{INTA}$(QS1)
6	A10	A11	28	IO/$\overline{M}$($\overline{S2}$)	ALE(QS0)
7	A9	A10	29	$\overline{WR}$($\overline{LOCK}$)	$\overline{DEN}$($\overline{S0}$)
8	A8	A9	30	HLDA($\overline{RQ}$/$\overline{GTI}$)	DT/$\overline{R}$($\overline{SI}$)
9	AD7	A8	31	HOLD($\overline{RQ}$/$\overline{GTO}$)	IO/$\overline{M}$($\overline{S2}$)
10	AD6	AD7	32	$\overline{RD}$	$\overline{WR}$($\overline{LOCK}$)
11	AD5	AD6	33	MN/$\overline{MX}$	HLDA($\overline{RQ}$/$\overline{GTI}$)
12	AD4	AD5	34	$\overline{SSO}$(HIGH)	HOLD($\overline{RQ}$/$\overline{GTO}$)
13	AD3	AD4	35	A19/S6	$\overline{RD}$
14	AD2	AD3	36	A18/S5	MN/$\overline{MX}$
15	AD1	AD2	37	A17/S4	$\overline{SSO}$(HIGH)
16	AD0	AD1	38	A16/S5	A19/S6
17	NMI	AD0	39	A15	NC
18	INTR	NC	40	V_{CC}	A18/S5
19	CLK	NMI	41	---	A17/S4
20	GND	INTR	42	---	A16/S5
21	RESET	CLK	43	---	A15
22	READY	GND	44	---	V_{CC}

Note: Parenthetical references apply to maxium mode only.

FIGURE 1. Terminal connections.

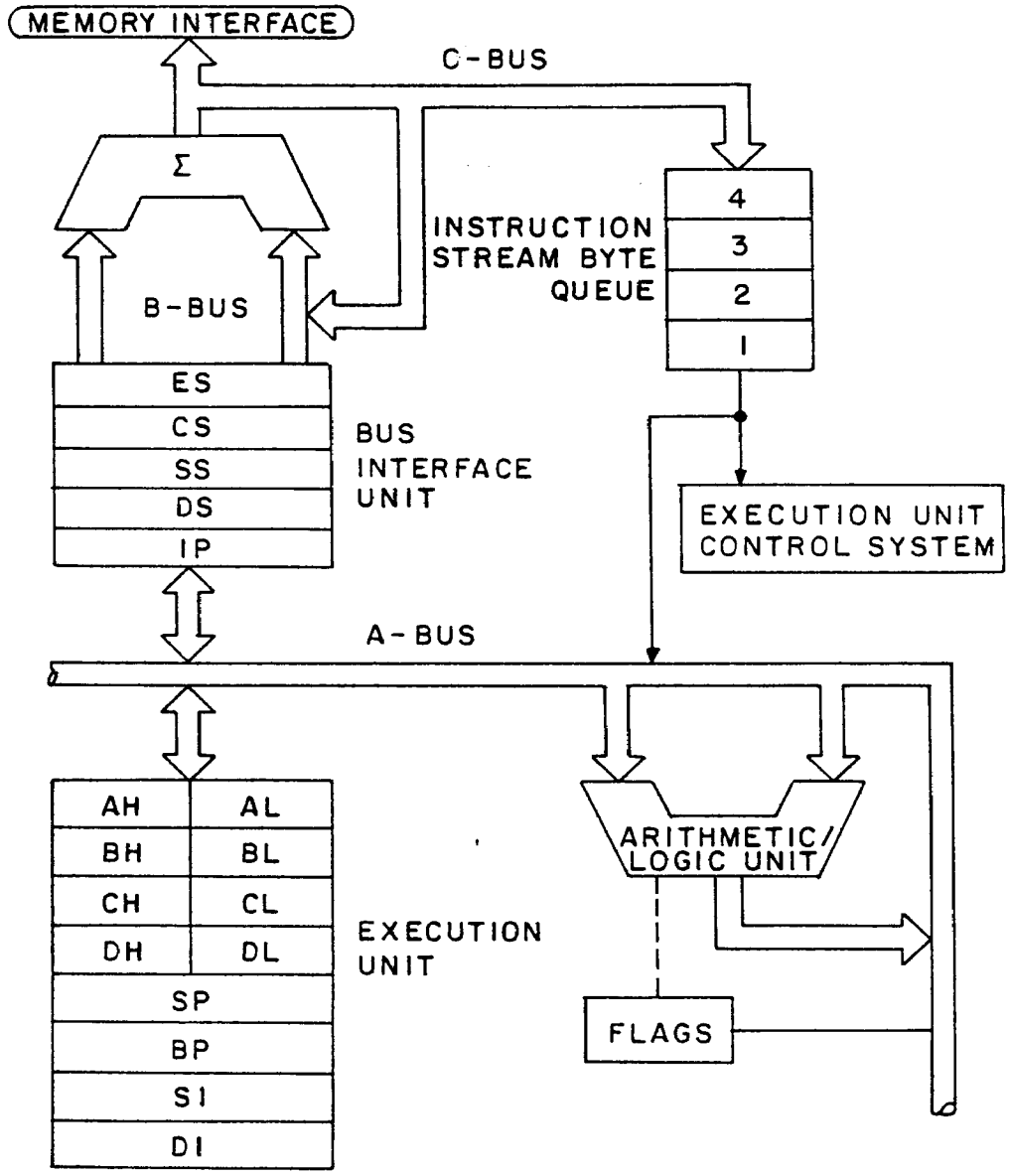
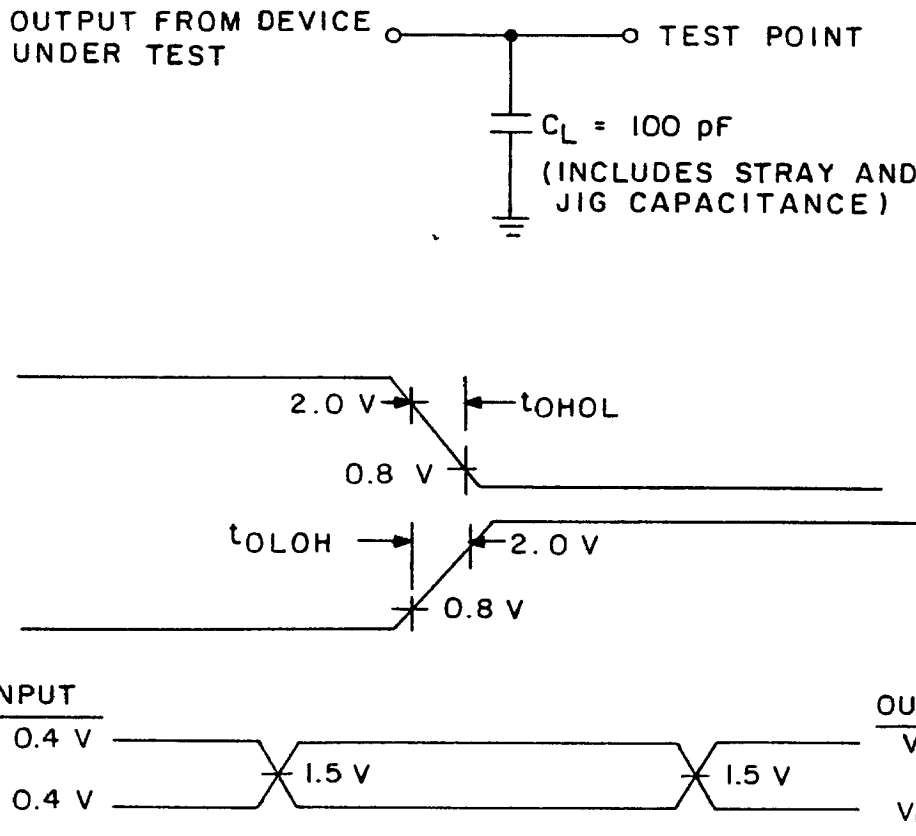
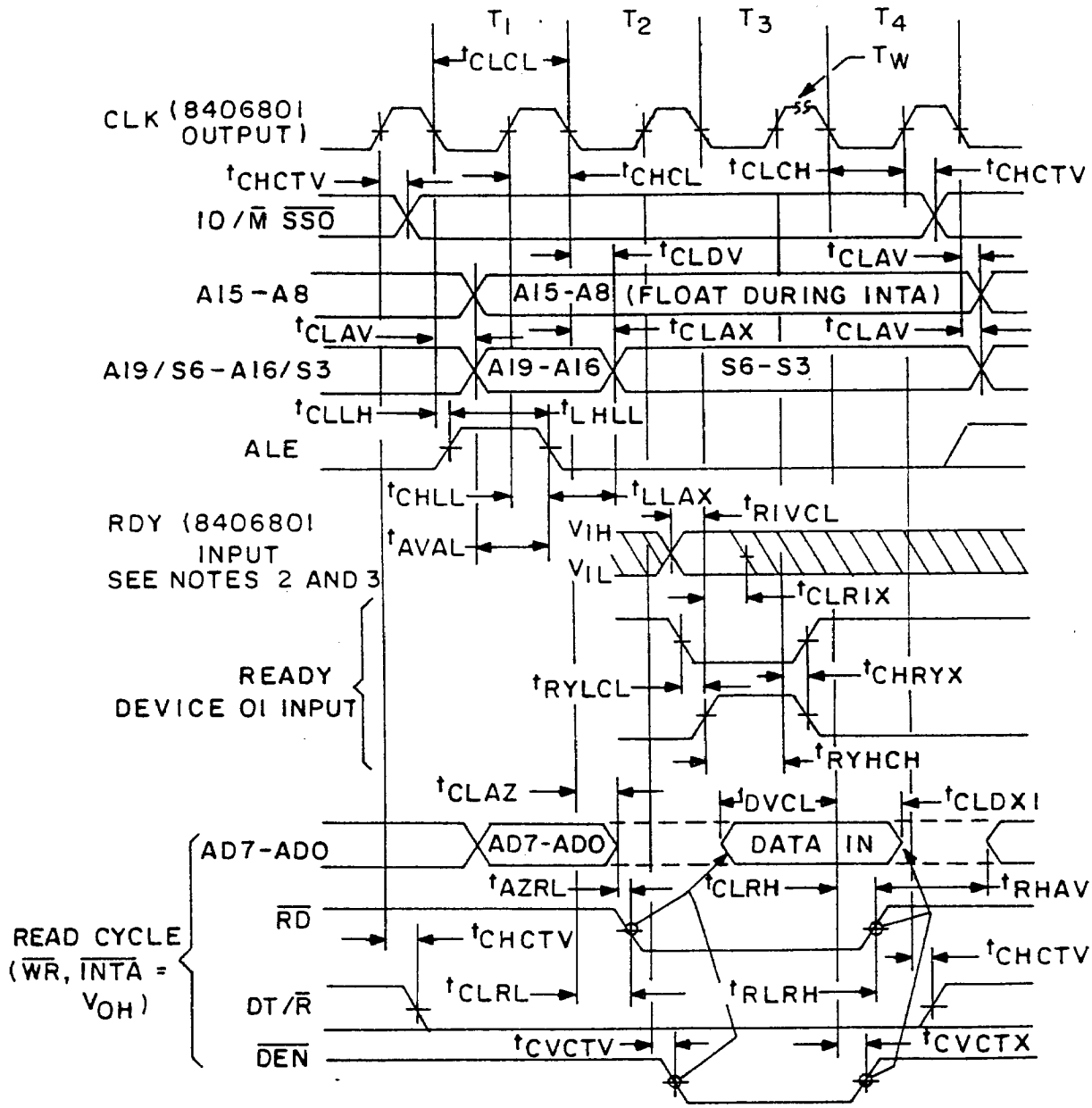


FIGURE 2. Block diagram.



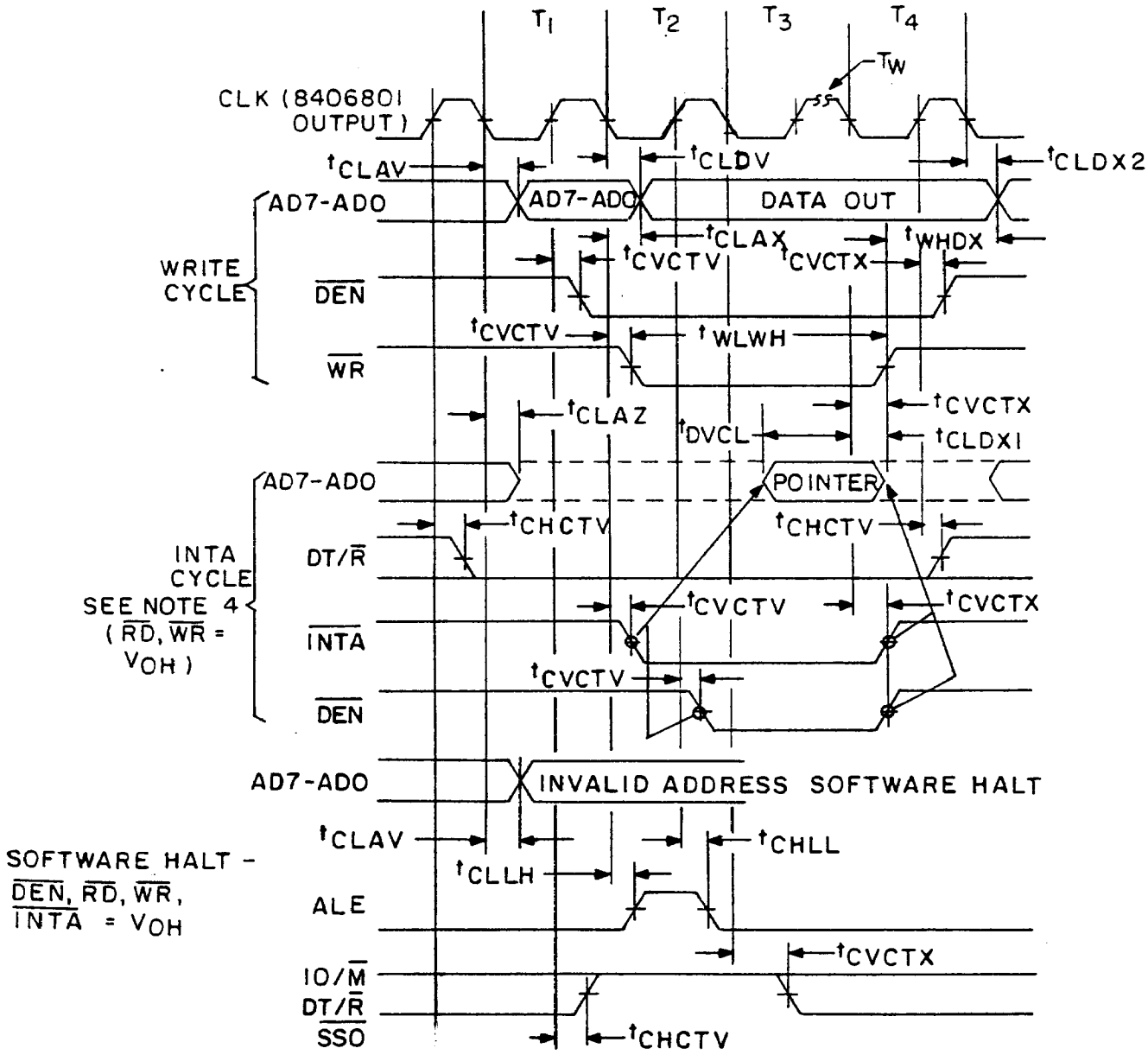
NOTE: All input signals (other than CLK) must switch between V_{IL} (max) -0.4 and V_{IH} (min) +0.4 V. CLK must switch between 0.4 V and V_{CC} -0.4 V. Input rise and fall times are driven at 1.0 ns/V.

FIGURE 3. Test circuit and switching waveforms.



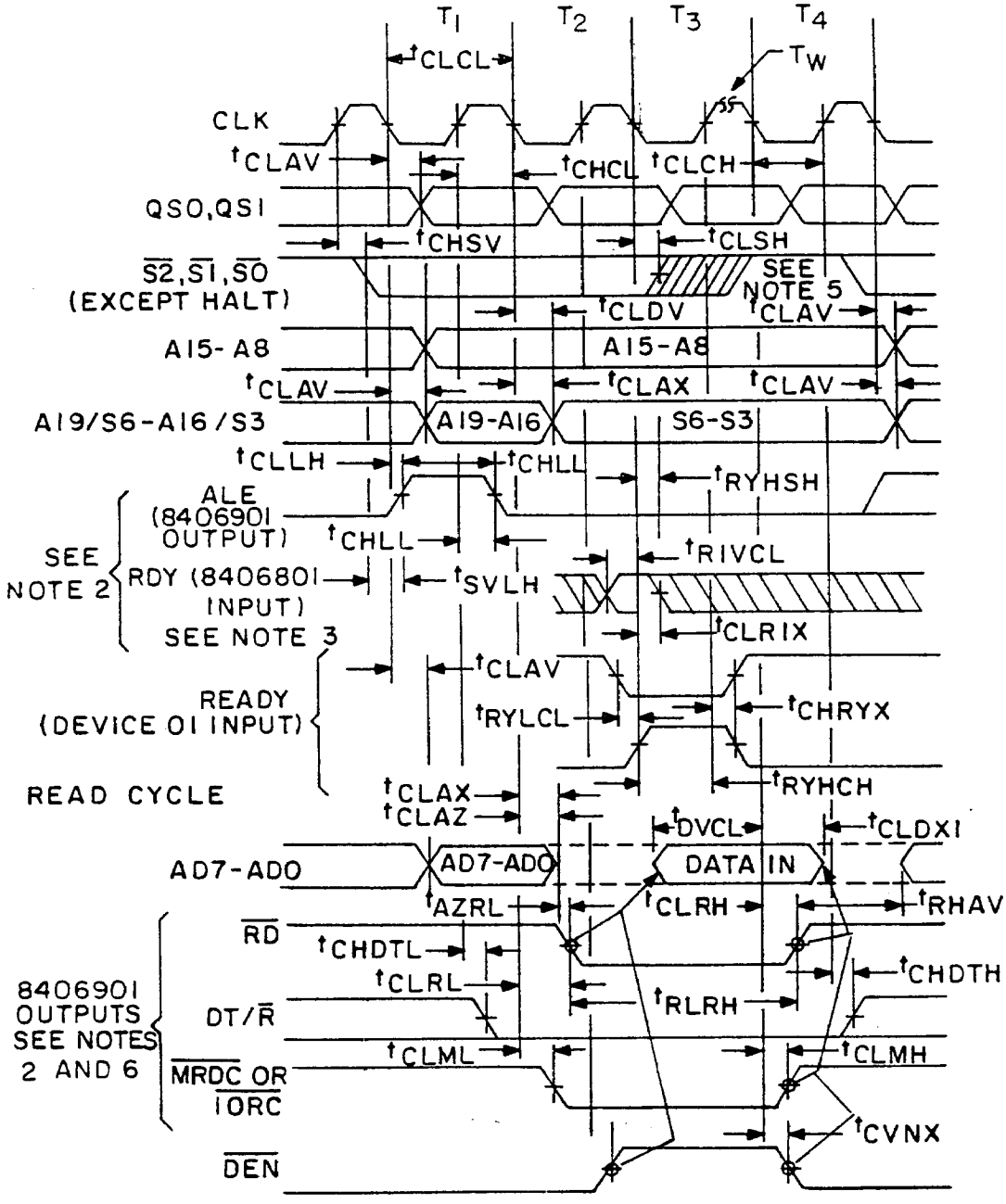
Bus timing (minimum mode system)

FIGURE 3. Test circuit and switching waveforms - Continued.



Bus timing (minimum mode system)

FIGURE 3. Test circuit and switching waveforms - Continued.



Bus timing (maximum mode)

FIGURE 3. Test circuit and switching waveforms - Continued.

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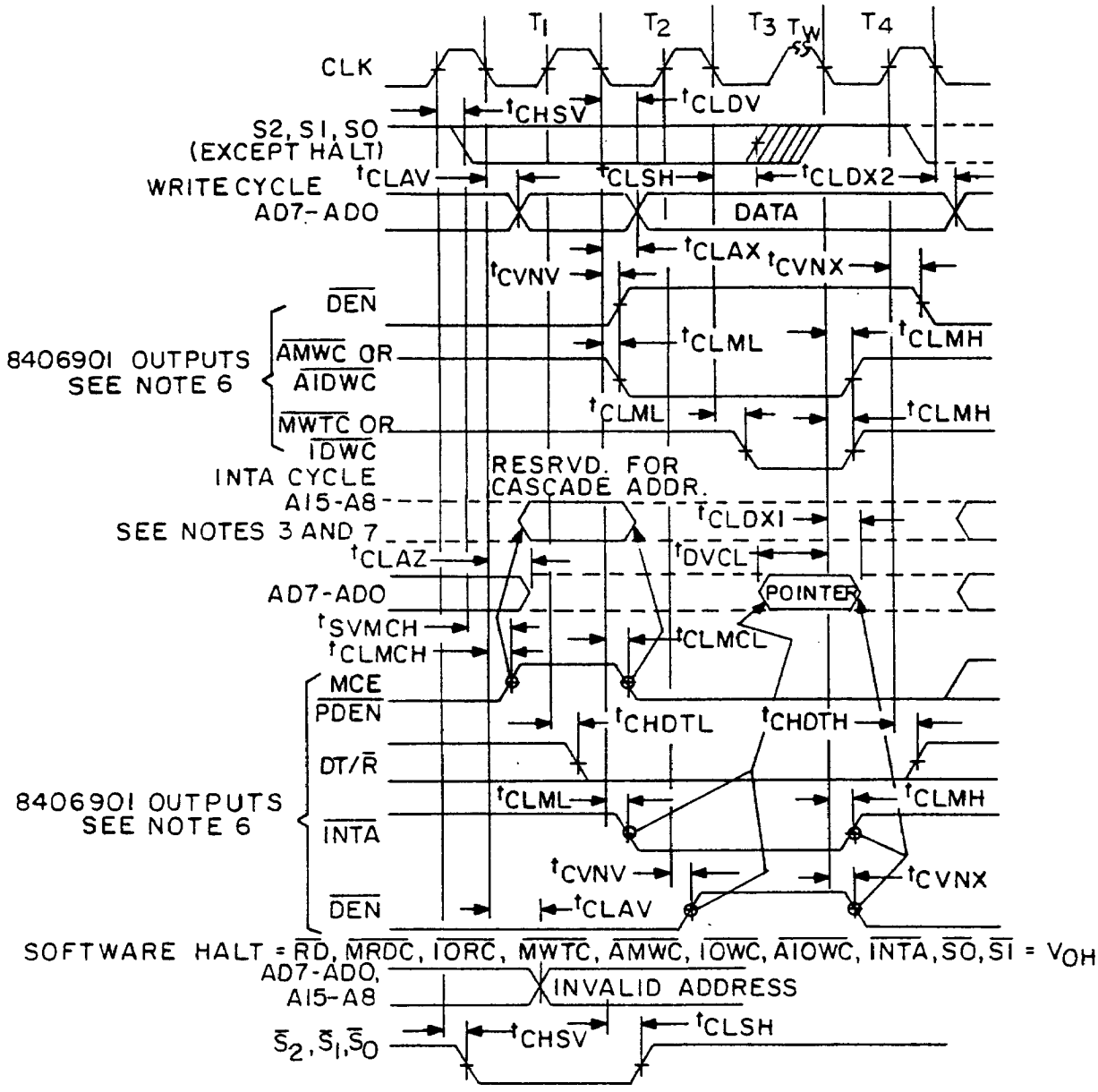
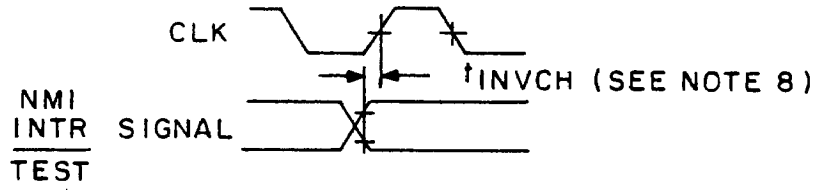
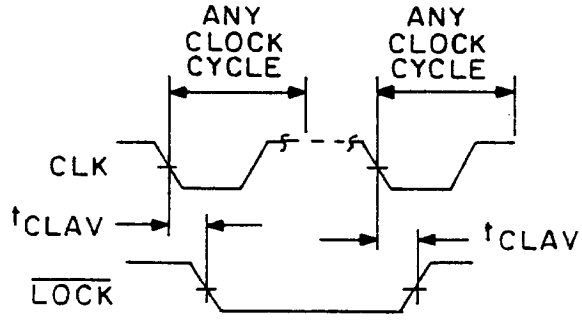


Bus timimg (maximum mode system)

FIGURE 3. Test circuit and switching waveforms - Continued.

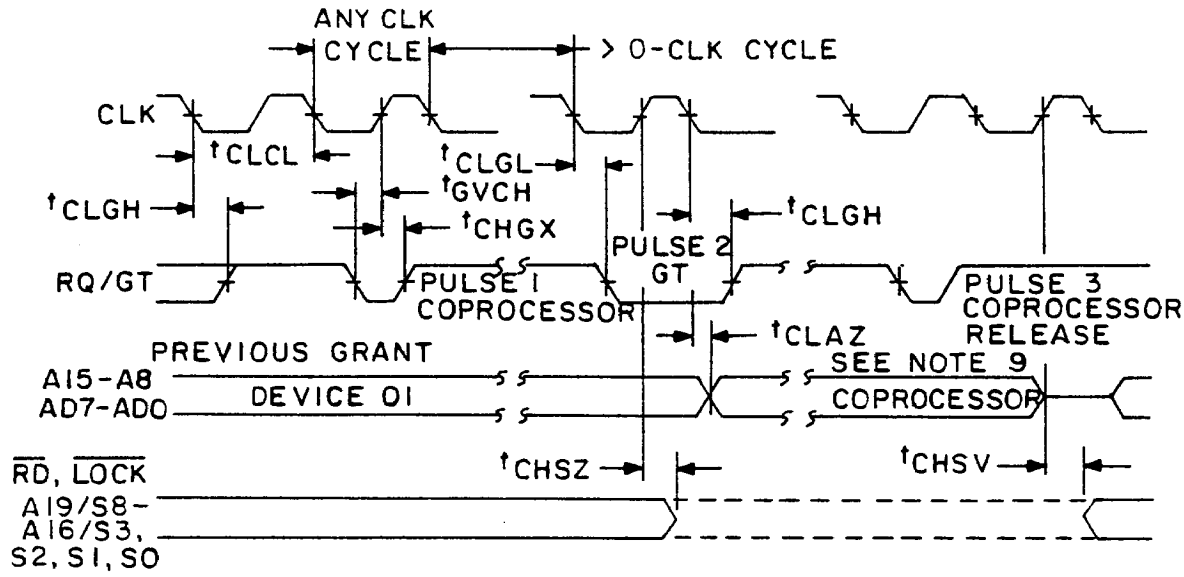


Asynchronous signal recognition

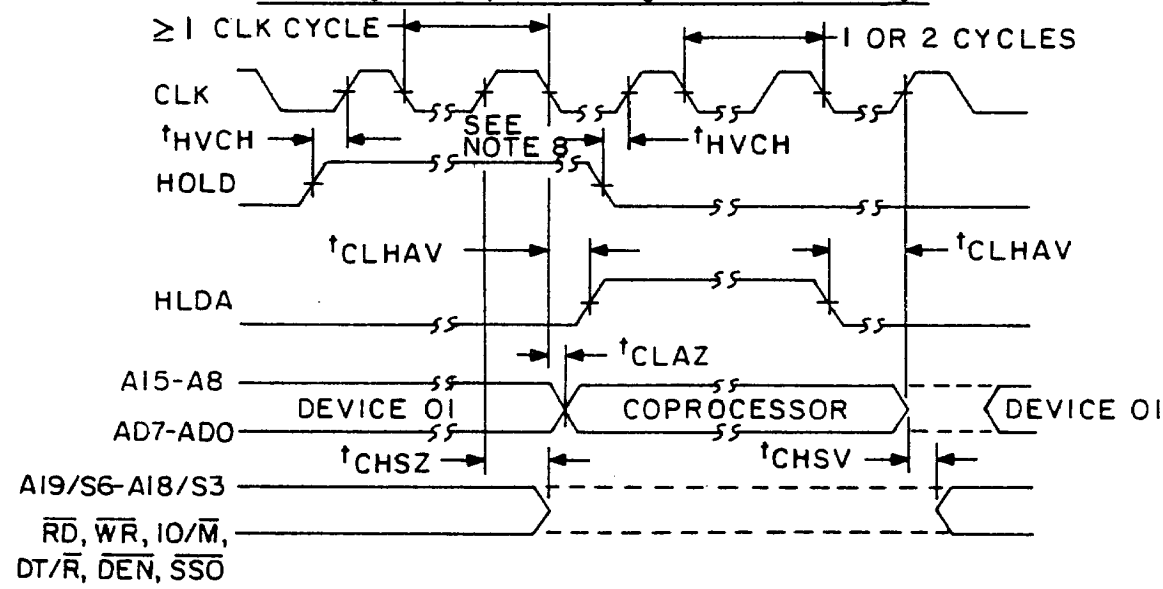


Bus lock signal timing (maximum mode only)

FIGURE 3. Test circuit and switching waveforms - Continued.

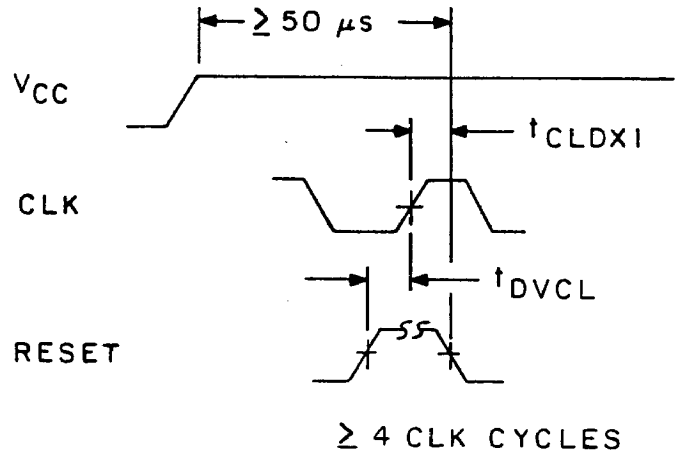


Request/grant sequence timing (maximum mode only)



Hold/hold acknowledge timing (minimum mode only)

FIGURE 3. Test circuit and switching waveforms - Continued.



Reset timing

NOTES:
1. All timing measurements are made at 1.5 V and all signals switch between V_{OH} and V_{OL}, unless otherwise specified.
2. Signals referencing military drawings 84068 or 84069 are shown only for informational purposes.
3. RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.
4. Two $\overline{\text{INTA}}$ cycles run back-to-back. Device 01 local ADDR/DATA bus is floating during both $\overline{\text{INTA}}$ cycles. Control signals are shown for the $\overline{\text{INTA}}$ cycle.
5. Status inactive in state just prior to T4.
6. The issuance of drawing 84069 command and control signals ($\overline{\text{MDRC}}$, $\overline{\text{MWTC}}$, $\overline{\text{AMWC}}$, $\overline{\text{IORC}}$, $\overline{\text{IOWC}}$, $\overline{\text{AIOWC}}$, $\overline{\text{INTA}}$ and DEN) lags the active high 84069 CEN.
7. Cascade address is valid between first and second $\overline{\text{INTA}}$ cycles.
8. Setup requirements for asynchronous signals only to guarantee recognition at next CLK.
9. The coprocessor may not drive the busses outside the region shown without risking contention.

FIGURE 3. Test circuit and switching waveforms - Continued.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}, C_{OUT}, and $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A sample size of fifteen devices with zero rejects shall be required, and all input and output terminals shall be tested.

d. Subgroups 7 and 8 shall verify functionality of the device. These tests form a part of the manufacturers test tape and shall be maintained and available from the approved source of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8, 9,10,11
Group A test requirements (method 5005)	1,2,3,4,7,8,9 10,11
Group C and D end-point electrical parameters (method 5005)	1,7,9

* PDA applies to subgroup 1.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.6 Pin functions. Microcircuits conforming to this drawing shall have pin functions as specified in table III herein.

TABLE III. Pin functions.

<table>
<tr><td colspan="3">Minimum and maximum system mode

The following pin descriptions are for device 01 system in either minimum or maximum mode. The "local bus" in these descriptions is the direct multiplexed bus interface connection to device 01 (without regard to additional bus buffers).</td></tr>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>AD7-AD0</td><td>I/O</td><td>Address data bus. These lines constitute the time multiplexed memory/IO ADDRESS (T1) and data (T2, T3, TW, and T4) bus. These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".</td></tr>
<tr><td>A15-A8</td><td>O</td><td>Address bus. These lines provide address bits 8 through 15 for the entire bus cycle (T1-T4). These lines do not have to be latched by ALE to remain valid. A15-A8 are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".</td></tr>
<tr><td>A19/S6,
A18/S5,
A17/S4,
A16/S3</td><td>O</td><td>Address/status. During T1, these are the four most significant address lines for memory operations. During I/O operations, these lines are LOW. During memory and I/O operations, status information is available on these lines during T2, T3, TW, and T4. S6 is always LOW. The status of the interrupt enable flat bit (S5) is updated at the beginning of each clock cycle. S4 and S3 are encoded as shown.

This information indicates which segment register is presently being used for data accessing.

These lines float to 3-state OFF during local bus "hold acknowledge".
<table>
<tr><th>S4</th><th>S3</th><th>Characteristics</th></tr>
<tr><td>0</td><td>0</td><td>Alternate data</td></tr>
<tr><td>0</td><td>1</td><td>Stack</td></tr>
<tr><td>1</td><td>0</td><td>Code or none</td></tr>
<tr><td>1</td><td>1</td><td>Data</td></tr>
</table>
</td></tr>
</table>

TABLE III. Pin functions - Continued.

Minimum and maximum system mode - Continued		
Name	I/O	Description
$\overline{RD}$	O	Read. Read strobe indicates that the processor is performing a memory or I/O read cycle depending on the state of the IO/$\overline{M}$ pin or S2. This signal is used to read devices which reside on device 01 local bus. $\overline{RD}$ is active LOW during T2, T3, and TW of any read cycle, and is guaranteed to remain HIGH in T2 until device 01 local bus has floated. This signal floats to 3-state OFF in "hold acknowledge".
READY	I	READY. The acknowledgment from the addressed memory or I/O device that it will complete the data transfer. The RDY signal from memory or I/O is synchronized by military drawing PIN 8406801 clock generator to form READY. This signal is active HIGH . Device 01 READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met.
INTR	I	Interrupt request. A level-triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.
$\overline{TEST}$	I	$\overline{TEST}$. Input is examined by the "wait for test" instruction. If the $\overline{TEST}$ input is LOW, execution continues; otherwise, the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	I	Nonmaskable interrupt. An edge-triggered input which causes a type 2 interrupt. A subroutine is vectored via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	I	RESET. Causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the instruction set description, when RESET returns LOW. RESET is internally synchronized.

TABLE III. Pin functions - Continued.

Minimum and maximum system mode - Continued		
Name	I/O	Description
CLK	I	Clock. Provides the basic timing for the processor and bus controller. It is asymmetric with a 33 percent duty cycle to provide optimized internal timing.
V_{CC}		V_{CC}. The +5.0 V ±10% power supply pin.
GND		GND. The ground pins.
MN/$\overline{MX}$		Minimum/maximum. Indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

Minimum system mode

The following pin descriptions are for device 01 system in minimum mode (i.e., MN/$\overline{MX}$ = V_{CC}). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described previously.

Name	I/O	Description
IO/$\overline{M}$	O	Status line. An inverted maximum mode $\overline{S2}$. It is used to distinguish a memory access from an I/O access. IO/$\overline{M}$ becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (I/O = HIGH, M = LOW). IO/$\overline{M}$ floats to 3-state OFF in local bus "hold acknowledge".
$\overline{WR}$	O	Write. Strobe indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the IO/$\overline{M}$ signal. $\overline{WR}$ is active for T2, T3, and TW of any write cycle. It is active LOW and floats to 3-state OFF in local bus "hold acknowledge".
$\overline{INTA}$	O	INTA. Used as a read strobe for interrupt acknowledge cycles. It is active LOW during T2, T3, and TW of each interrupt acknowledgment cycle.
ALE	O	Address latch enable. Provided by the processor to latch the address into military drawing PIN 8406701 or 8406702 address latch. It is a HIGH pulse active during clock low of T1 of any bus cycle. Note that ALE is never floated.

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TABLE III. Pin functions - Continued.

Minimum system mode - Continued		
Name	I/O	Description
DT/$\overline{R}$	O	Data transmit/receive. Needed in a minimum system that desires to use military drawing PIN's 5962-8757701 or 5962-8757702 data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically DT/$\overline{R}$ is equivalent to $\overline{S1}$ in the maximum mode, and its timing is the same as for IO/$\overline{M}$ (T-HIGH, R-LOW). This signal floats to 3-state OFF in local bus "hold acknowledge".
$\overline{DEN}$	O	Data enable. Provided as an output enable for military drawing PIN's 5962-8757701 or 5962-8757702 in a minimum system that uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle, it is active from the middle of T2 until the middle of T4; while for a write cycle, it is active from the beginning of T2 until the middle of T4. $\overline{DEN}$ floats to 3-state OFF during local bus "hold acknowledge".
HOLD, HLDA	I O	HOLD. Indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgment, in the middle of a T4 or T1 clock cycle. Simultaneous with the issuance of HLDA, the processor will float the local bus and control the lines. After HOLD is detected as being LOW, the processor lowers HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. Hold is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the set up time.
$\overline{SSO}$	O	STATUS LINE. Logically equivalent to $\overline{S0}$ in the maximum mode. The combination of $\overline{SSO}$, IO/$\overline{M}$ and DT/$\overline{R}$ allows the system to completely decode the current bus cycle status. $\overline{SSO}$ is held to high impedance logic one during local bus "hold acknowledge".

IO/$\overline{M}$	DT/$\overline{R}$	$\overline{SSO}$	CHARACTERISTICS
1	0	0	Interrupt acknowledge
1	0	1	Read I/O port
1	1	0	Write I/O port
1	1	1	Halt
0	0	0	Code access
0	0	1	Read memory
0	1	0	Write memory
0	1	1	Passive

TABLE III. Pin functions - Continued.

Maximum system mode

The following pin descriptions are for device 01 system in maximum mode (i.e., MN/$\overline{MX}$ = GND). Only the pin functions which are unique to maximum mode are described; all other pin functions are as described previously

Name	I/O	Description
$\overline{S0}$ $\overline{S1}$ $\overline{S2}$	0 0 0	STATUS. Active during clock high of T4, T1, and T2, and is returned to the passive state (1, 1, 1) during T3 or during TW when READY is HIGH. This status is used by military drawing PIN 8406901 bus controller to generate all memory and I/O access control signals. Any change by S2, S1, or S0 during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or TW is used to indicate the end of a bus cycle. These signals are held at a high impedance logic one state during "grant sequence".
$\overline{RQ/GT0}$, $\overline{RQ/GT1}$	I/O	REQUEST/GRANT. Pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ/GT0}$ having higher priority than $\overline{RQ/GT1}$. $\overline{RQ/GT}$ has internal bus-hold high circuitry and, if unused, may be left unconnected. The request/grant sequence is as follows (see $\overline{RQ/GT}$ timing sequence): 1. A pulse of one CLK wide from another local bus master indicates a local bus request ("hold") to device 01 (pulse 1). 2. During a T4 or T1 clock cycle, a pulse one clock wide from device 01 to the requesting master (pulse 2), indicates that device 01 has allowed the local bus to float and that it will enter the "grant sequence" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "grant sequence".

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	CHARACTERISTICS
0	0	0	Interrupt acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	Code access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive

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TABLE III. Pin functions - Continued.

Maximum system mode - Continued		
Name	I/O	Description
$\overline{RQ/GT0}$, $\overline{RQ/GT1}$ (continued)		3. A pulse one CLK wide from the requesting master indicates to device 01 (pulse 3) that the "hold" request is about to end and that device 01 can reclaim the local bus at the next CLK. The CPU then enters T4 (or T1 if no bus cycles pending). Each master-master exchange of the local bus is a sequence of three pulses. There must be one idle CLK cycle after bus exchange. Pulses are active LOW. If the request is made while the CPU is performing a memory cycle, it will release the local bus during the T4 of the cycle when all the following conditions are met: 1. Request occurs on or before T2. 2. Current cycle is not the low bit of a word. 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. If the local bus is idle when the request is made, the two possible events will follow: 1. Local bus will be released during the next clock. 2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.
$\overline{LOCK}$	0	LOCK. Indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active (LOW). The $\overline{LOCK}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and is held at a high impedance logic one state during "grant sequence". In Max Mode, $\overline{LOCK}$ is automatically generated during T2 of the first $\overline{INTA}$ cycle and removed during T2 of the second $\overline{INTA}$ cycle.

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TABLE III. Pin functions - Continued.

<table>
<tr><th colspan="3">Maximum system mode - Continued</th></tr>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>QS1,
QS0</td><td>O</td><td>QUEUE STATUS. Provide status to allow external tracking of the internal device 01 instruction queue.

The queue status is valid during the CLK cycle after which the queue operation is performed. Note that the queue status never goes to a high impedance state (floated).

<table>
<tr><th>QS1</th><th>QS0</th><th>Characteristics</th></tr>
<tr><td>0</td><td>0</td><td>No operation</td></tr>
<tr><td>0</td><td>1</td><td>First byte of Opcode from queue</td></tr>
<tr><td>1</td><td>0</td><td>Empty the queue</td></tr>
<tr><td>1</td><td>1</td><td>Subsequent byte from queue</td></tr>
</table>
</td></tr>
<tr><td>HIGH</td><td>O</td><td>Pin 34 is always a logic one in the maximum mode and is held at a high impedance logic one during a "grant sequence".</td></tr>
</table>

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 7 DECEMBER 1990

Approved sources of supply for SMD 5962-86016 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECS. The bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar part PIN 1/
5962-8601601QX	34371	MD80C88/883
5962-8601601XX	34371	MR80C88/883

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Harris Semiconductor P.O. Box 883 Melbourne, FL 32901

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.