REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Add packages J and 3 for device type 02. Editorial changes throughout.	93-02-16	Monica L. Poelking

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV	A																		
SHEET	15																		

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

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AMSC N/A

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DRAWING APPROVAL DATE
86-10-06

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, ADVANCED, SCHOTTKY TTL, ARITHMETIC LOGIC UNIT, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-86710
A	67268	

SHEET 1 OF 15

DESC FORM 193
JUL 91

5962-E100-93

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1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54F381	4-bit arithmetic logic unit
02	54F181	4-bit arithmetic logic unit

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line package
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line package
S	GDFP2-F20 or CDFP3-F20	20	Flat package
2	CQCC1-N20	20	Square leadless chip carrier
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish shall be as specified in MIL-M-38510. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Supply voltage range . . . . . -0.5 V dc to +7.0 V dc
Input voltage range . . . . . -1.5 V dc at -18 mA to +7.0 V dc
Storage temperature . . . . . -65°C to +150°C
Maximum power dissipation (P_D) per device 1/ . . . . . 490 mW
Lead temperature (soldering, 10 seconds) . . . . . +300°C
Thermal resistance, junction-to-case (Θ_{JC}) . . . . . See MIL-STD-1835
Junction temperature (T_J) . . . . . +175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) . . . . . +4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage (V_{IH}) . . . . . +2.0 V dc
Maximum low level input voltage (V_{IL}) . . . . . +0.8 V dc
Case operating temperature range (T_C) . . . . . -55°C to +125°C

1/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V I_{OH} = -1.0 mA V_{IN} = 0.8 V or 2.0 V		1,2,3	All	2.5		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V I_{OL} = 20 mA V_{IN} = 0.8 V or 2.0 V		1,2,3	All		0.5	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V I_{IN} = -18 mA T_C = +25°C		1	All		-1.2	V
High level input current	I_{IH1}	V_{CC} = 5.5 V V_{IN} = 2.7 V		1,2,3	All		20	µA
	I_{IH2}	V_{CC} = 5.5 V V_{IN} = 7.0 V		1,2,3	All		100	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V V_{IN} = 0.5 V	S_0-S_2 inputs	1,2,3	01		-0.6	mA
			Other inputs				-2.4	
			M input	1,2,3	02		-0.6	
			A_n, B_n inputs				-1.8	
			S_n inputs				-2.4	
			C_n inputs				-3.0	
Short circuit output current	I_{OS}	V_{CC} = 5.5 V V_{OUT} = 0.0 V 1/		1,2,3	All	-60	-150	mA
Supply current	I_{CC}	V_{CC} = 5.5 V S_0-S_3 = GND Other inputs high		1,2,3	01		89	mA
					02		65	
Functional tests		See 4.3.1c		7	All			

See note at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Propagation delay time, C_n to F_1	t_{PLH1}	V_{CC} = 5.0 V R_L = 500Ω C_L = 50 pF minimum See figure 4.	9	01		12	ns
			10,11			15	
	t_{PHL1}		9	01		8	ns
			10,11			12	
Propagation delay time, C_n to F_n	t_{PLH2}		9	02	3.0	8.5	ns
			10,11		2.5	16.0	
	t_{PHL2}		9	02	3.0	8.5	ns
			10,11		2.5	12.0	
Propagation delay time, any A or B to any F	t_{PLH3}		9	01		15	ns
			10,11			19	
	t_{PHL3}		9	01		13	ns
			10,11			16	
Propagation delay time, any A or B to any F (mode = sum)	t_{PLH4}		9	02	4.0	10.5	ns
			10,11		3.5	16.5	
	t_{PHL4}		9	02	4.0	10.0	ns
			10,11		4.0	13.5	
Propagation delay time, any A or B to any F (mode = dif)	t_{PLH5}		9	02	4.0	12.0	ns
			10,11		3.5	17.5	
	t_{PHL5}		9	02	3.0	12.0	ns
			10,11		3.0	14.0	
Propagation delay time, S_1 to F_1	t_{PLH6}		9	01		20	ns
			10,11			24	
	t_{PHL6}		9	01		14	ns
			10,11			17	
Propagation delay time, A_1 or B_1 to G	t_{PLH7}		9	01		12	ns
			10,11			14	
	t_{PHL7}		9	01		10	ns
			10,11			14	

See note at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Propagation delay time, A or B to G (mode = sum)	t_{PLH8}	V_{CC} = 5.0 V R_L = 500Ω C_L = 50 pF minimum See figure 4.	9	02	2.5	7.5	ns
			10,11		2.5	9.0	
	t_{PHL8}		9	02	2.5	7.5	ns
			10,11		2.5	9.5	
Propagation delay time, A or B to G (mode = dif)	t_{PLH9}		9	02	3.0	9.0	ns
			10,11		2.5	11.5	
	t_{PHL9}		9	02	2.5	9.5	ns
			10,11		2.5	11.0	
Propagation delay time, A_1 or B_1 to P	t_{PLH10}		9	01		11	ns
			10,11			15	
	t_{PHL10}		9	01		10	ns
			10,11			13	
Propagation delay time, A or B to P (mode = sum)	t_{PLH11}		9	02	2.5	7.0	ns
			10,11		2.5	8.5	
	t_{PHL11}		9	02	3.0	7.5	ns
			10,11		3.0	9.5	
Propagation delay time, A or B to P (mode = dif)	t_{PLH12}		9	02	2.5	8.0	ns
			10,11		2.5	11.0	
	t_{PHL12}		9	02	3.0	8.5	ns
			10,11		3.0	11.0	
Propagation delay time, S_1 to G or P	t_{PLH13}		9	01		14	ns
			10,11			19	
	t_{PHL13}		9	01		14	ns
			10,11			19	
Propagation delay time, A or B to A=B (mode = dif)	t_{PLH14}		9	02	11	27	ns
			10,11		8	35	
	t_{PHL14}		9	02	5.5	13.5	ns
			10,11		5.5	21.0	

See note at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay time, A_i or B_i to F_i (mode = sum)	t_{PLH15}	V_{CC} = 5.0 V R_L = 500Ω C_L = 50 pF minimum See figure 4.	9	02	3.0	9.0	ns
			10,11		3.0	14.5	
	t_{PHL15}		9	02	3.0	10.0	ns
			10,11		3.0	14.5	
Propagation delay time, A_i or B_i to F_i (mode = dif)	t_{PLH16}		9	02	3.0	11.0	ns
			10,11		3.0	17.5	
	t_{PHL16}		9	02	3.0	11.0	ns
			10,11		3.0	14.5	
Propagation delay time, A or B to C_{n+4} (mode = sum)	t_{PLH17}		9	02	5.0	13.0	ns
			10,11		5.0	15.5	
	t_{PHL17}		9	02	3.5	12.0	ns
			10,11		3.5	16.5	
Propagation delay time, A or B to C_{n+4} (mode = dif)	t_{PLH18}		9	02	5.0	14.0	ns
			10,11		5.0	17.0	
	t_{PHL18}		9	02	5.0	13.0	ns
			10,11		4.0	15.0	
Propagation delay time, C_n to C_{n+4}	t_{PLH19}		9	02	3.0	8.5	ns
			10,11		3.0	10.0	
	t_{PHL19}		9	02	3.0	8.0	ns
			10,11		3.0	9.5	
Propagation delay time, A or B to F (mode = logic)	t_{PLH20}		9	02	3.5	9.5	ns
			10,11		3.5	14.5	
	t_{PHL20}		9	02	3.0	10.0	ns
			10,11		3.0	15.5	

1/ Not more than one output should be shorted at one time, and the duration of the short circuit condition should not exceed 1 second.

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Device type	02	01	02
Case outline	J	R, S, and 2	3
Terminal number	Terminal symbol		
1	$\overline{B}_0$	A_1	NC
2	A_0	B_1	$\overline{B}_0$
3	S_3	A_0	A_0
4	S_2	B_0	S_3
5	S_1	S_0	S_2
6	S_0	S_1	S_1
7	C_n	S_2	S_0
8	$\overline{M}$	F_0	NC
9	$\overline{F}_0$	F_1	C_n
10	$\overline{F}_1$	GND	$\overline{M}$
11	F_2	F_2	$\overline{F}_0$
12	GND	$\overline{F}_3$	$\overline{F}_1$
13	F_3	$\overline{G}$	F_2
14	$\overline{A=B}$	P	GND
15	P	C_n	NC
16	$\overline{C}_{n+4}$	B_3	F_3
17	$\overline{G}$	A_3	$\overline{A=B}$
18	$\overline{B}_3$	B_2	P
19	$\overline{A}_3$	A_2	$\overline{C}_{n+4}$
20	$\overline{B}_2$	V_{CC}	$\overline{G}$
21	$\overline{A}_2$	---	B_3
22	$\overline{B}_1$	---	NC
23	A_1	---	$\overline{A}_3$
24	V_{CC}	---	$\overline{B}_2$
25	---	---	$\overline{A}_2$
26	---	---	$\overline{B}_1$
27	---	---	A_1
28	---	---	V_{CC}

NC = No connection

FIGURE 1. Terminal connections.

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Device type 01

	Inputs						Outputs					
Function	S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	$\overline{G}$	$\overline{P}$
Clear	0	0	0	X	X	X	0	0	0	0	0	0
B minus A	1	0	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	1	1	1	0	0
				0	1	0	0	0	0	0	1	1
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	1	0
				1	0	1	1	1	1	1	0	0
				1	1	0	1	0	0	0	1	1
				1	1	1	0	0	0	0	1	0
A minus B	0	1	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	0	0	0	1	1
				0	1	0	0	1	1	1	0	0
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	1	0
				1	0	1	1	0	0	0	1	1
				1	1	0	1	1	1	1	0	0
				1	1	1	0	0	0	0	1	0
A plus B	1	1	0	0	0	0	0	0	0	0	1	1
				0	0	1	1	1	1	1	1	0
				0	1	0	1	1	1	1	1	0
				0	1	1	0	1	1	1	0	0
				1	0	0	1	0	0	0	1	1
				1	0	1	0	0	0	0	1	0
				1	1	0	0	0	0	0	1	0
				1	1	1	1	1	1	1	0	0
A $\oplus$ B	0	0	1	X	0	0	0	0	0	0	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	0
				X	1	1	0	0	0	0	0	0
A + B	1	0	1	X	0	0	0	0	0	0	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0
AB	0	1	1	X	0	0	0	0	0	0	0	0
				X	0	1	0	0	0	0	1	1
				X	1	0	0	0	0	0	0	0
				X	1	1	1	1	1	1	1	0
Preset	1	1	1	X	0	0	1	1	1	1	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0

1 = High voltage level
0 = Low voltage level
X = Immaterial

FIGURE 2. Truth tables.

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Device type 02

Selection				Active low data and F_n outputs		
				Logic function (M = H)	Arithmetic operations (M = H)	
S3	S2	S1	S0		C_n = inactive (no carry)	C_n = active (carry)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{AB}$	F = $A\overline{B}$ MINUS 1	F = $A\overline{B}$
L	L	H	L	F = A + B	F = AB MINUS 1	F = AB
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{A}$ + B	F = A PLUS ($A + \overline{B}$)	F = A PLUS ($A + \overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + B)	F = AB PLUS (A + B) PLUS 1
L	H	H	L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = $A\overline{B}$ + B	F = A + B	F = (A + B) PLUS 1
H	L	L	L	F = AB	F = A PLUS(A + B)	F = A PLUS(A + B) PLUS 1
H	L	L	H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = AB PLUS (A + B)	F = AB PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A	F = A PLUS A PLUS 1
H	H	L	H	F = AB	F = $A\overline{B}$ PLUS A	F = $A\overline{B}$ PLUS A PLUS 1
H	H	H	L	F = AB	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

Selection				Active high data and F_n outputs		
				Logic function (M = H)	Arithmetic operations (M = H)	
S3	S2	S1	S0		C_n = inactive (no carry)	C_n = active (carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A}$ + B	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	L	F = $\overline{AB}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $A\overline{B}$	F = A PLUS $A\overline{B}$	F = A PLUS $A\overline{B}$ PLUS 1
L	H	L	H	F = B	F = (A + B) PLUS $\overline{AB}$	F = (A + B) PLUS $\overline{AB}$ PLUS 1
L	H	H	L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = $A\overline{B}$	F = AB MINUS 1	F = AB
H	L	L	L	F = $\overline{A + B}$	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

H = High voltage level
L = Low voltage level

FIGURE 2. Truth tables - Continued.

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Device type 01

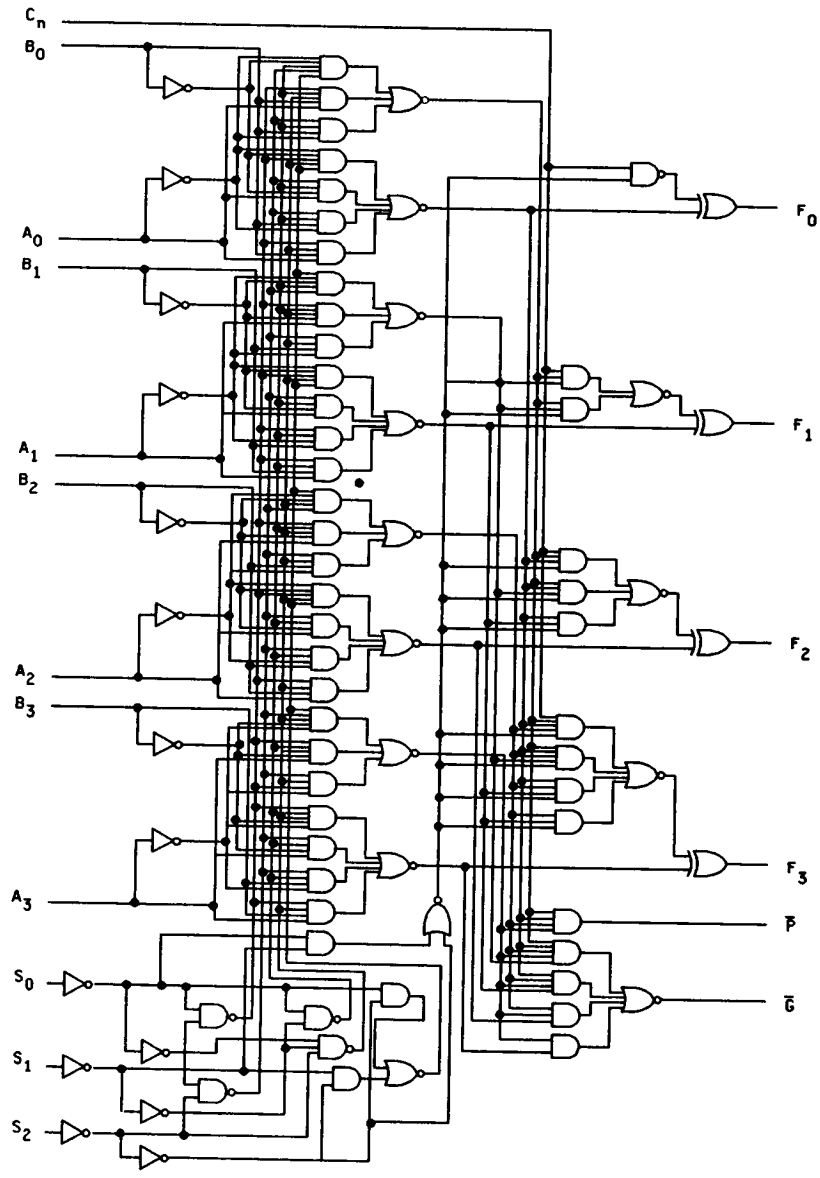

FIGURE 3. Logic diagrams.

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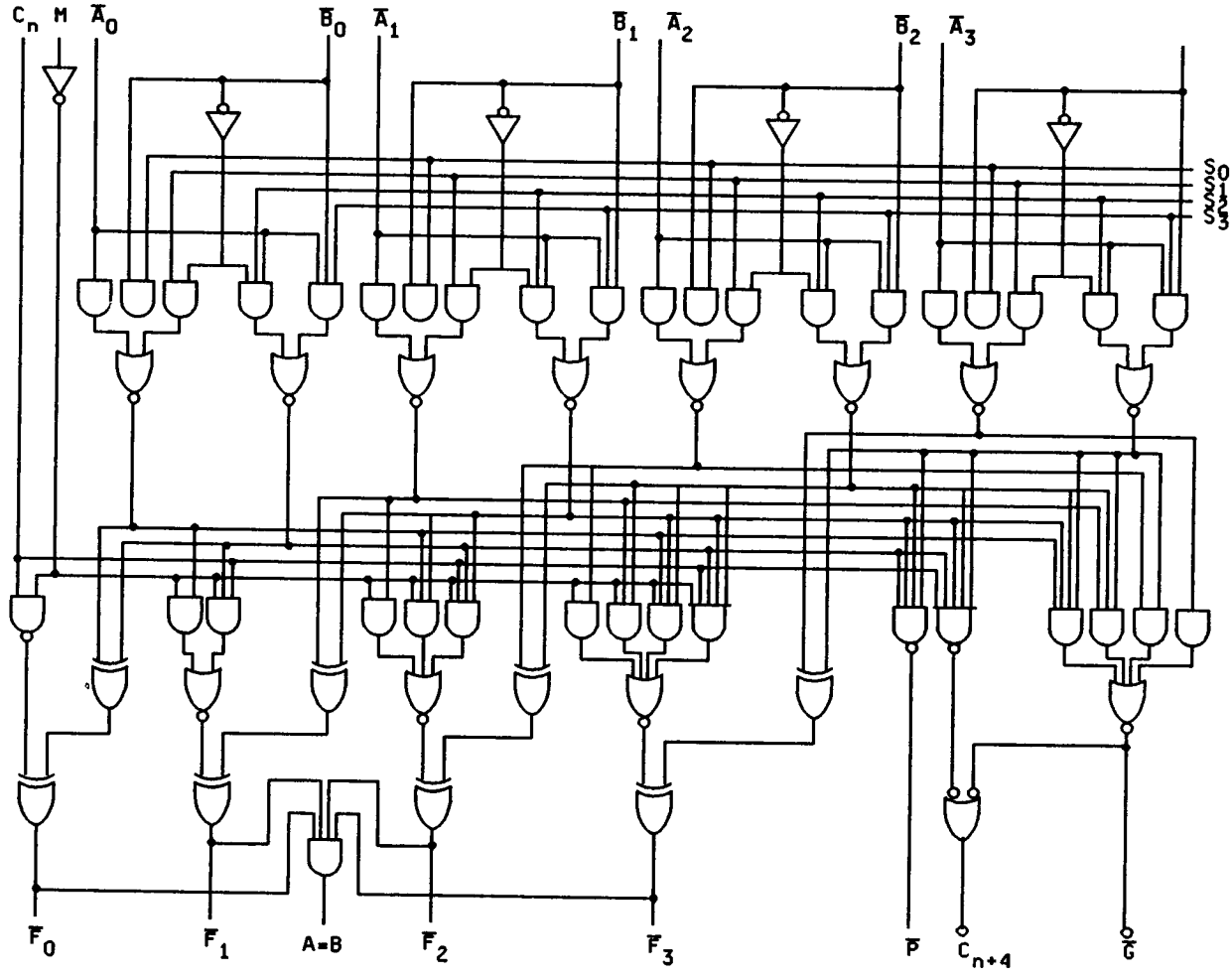

FIGURE 3. Logic diagrams - Continued.

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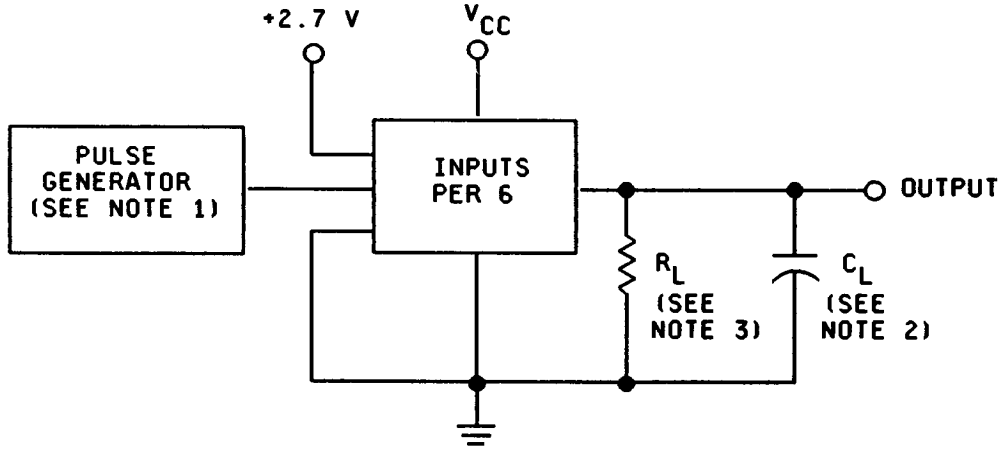
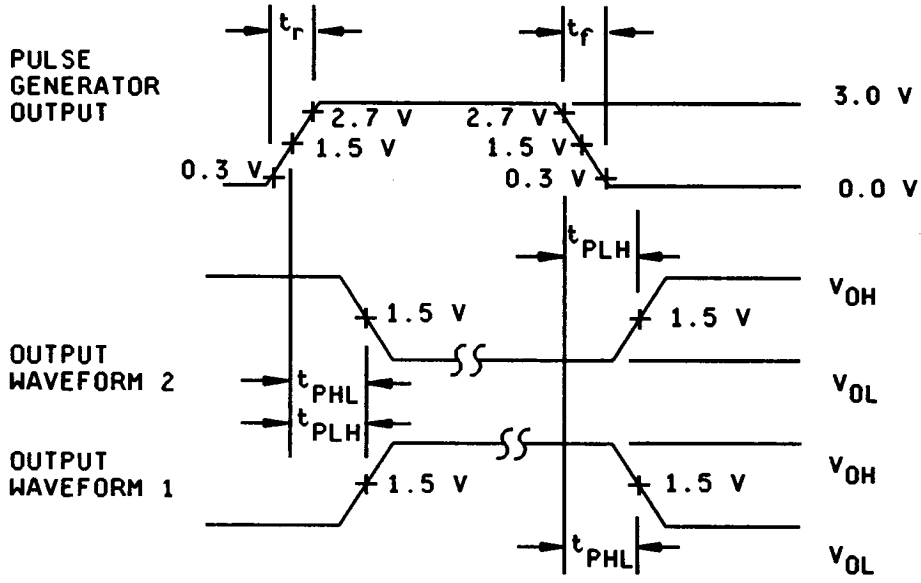
Device type 01 and 02





NOTES:
1. Pulse generator has the following characteristics: $t_r = t_f \leq 1$ MHz, $Z_{OUT} = 50\Omega$.
2. C_L includes jig and probe capacitance. C_L = 50 pF.
3. $R_L = 500\Omega$.

FIGURE 4. Test circuit and switching waveforms.

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3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall include the requirements for inputs, outputs, biases, and power dissipation, as applicable, in accordance with the specified purpose of method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

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4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall include the requirements for inputs, outputs, biases, and power dissapation, as applicable, in accordance with the specified purpose of method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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