REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 03 through 05 for vendor cage 34335. Alter electrical performance characteristics . Add additional load circuit (figure 5) for device types 03 through 05. Add device type 06 for vendor cage 61772. Inactivate case Z. Editorial changes throughout.	89/06/30	M.A. Frye
B	Changes in accordance with NOR 5962-R073-92	91/11/30	M. L. Poelking
C	Add device type 07 for vendor cage 61772. Add case outline T. Editorial changes throughout.	94/04/20	M. L. Poelking

REV																			
SHEET																			
REV																			
SHEET																			
REV	C	C	C	C	C	C	C	C	C										
SHEET	15	16	17	18	19	20	21	22	23										

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
2 JUNE 1988

REVISION LEVEL
C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, ERROR DETECTION AND CORRECTION UNIT, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-88533
A	67268	

SHEET 1 OF 24

DESC FORM 193
JUL 91

5962-E400-93

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0001156 323

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-88533	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Detect time	Correct time
01	49C460A	32-bit EDCU	33 ns	39 ns
02	49C460B	32-bit EDCU	28 ns	33 ns
03	29C660A	32-bit EDCU	33 ns	39 ns
04	29C660B	32-bit EDCU	28 ns	33 ns
05	29C660C	32-bit EDCU	21 ns	29 ns
06	49C460C	32-bit EDCU	21 ns	29 ns
07	49C460D	32-bit EDCU	16 ns	22 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
U	CMGA3-68	68	pin grid array
X	See figure 1	68	dual-in-line package
Y	CQCC1-N84	68	square chip carrier
Z	See figure 2	68	square chip carrier
T	See figure 3	68	quad flat package

1.3 Absolute maximum ratings. 1/

Voltage on any pin relative to ground	-0.5 V dc to +7.0 V dc 2/
DC output current into outputs	30 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W 3/ 4/
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (O_{JC}):	
Cases U and Y	See MIL-STD-1835
Case X	38°C/W 5/
Case Z	35°C/W 5/
Case T	20°C/W
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Minimum input high voltage (V_{IH})	2.0 V dc
Maximum input low voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Stresses greater than those listed may cause permanent damage to the device.
2/ V_{IL} minimum = -3.0 V for pulse width less than 20 ns.
3/ Maximum power dissipation can only be achieved by excessive I_{OL} or I_{OH}.
4/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.
5/ When a thermal resistance value for this case is included in MIL-STD-1835, that value shall supersede the value indicated herein.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein and as specified on figures 1, 2, and 3.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 4.

3.2.3 Block diagram. The block diagram shall be as specified on figure 5.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full (case or ambient) operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, V_{CC} = 4.5 V to 5.5 V unless otherwise specified		Group A subgroups	Device types	Limits Min	Limits Max	Unit
Input high voltage	V_{IH}	Guaranteed input logical high voltage for all inputs 2/		1,2,3	All	2.0		V
Input low voltage	V_{IL}	Guaranteed input logical low voltage for all inputs 2/		1,2,3	All		0.8	
Input high current	I_{IH}	V_{CC} = 5.5 V, V_{IN} = 5.5 V		1,2,3	All		10	µA
Input low current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = GND		1,2,3	All		-10	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300 µA	1,2,3	All	V_{CC}-0.2 V		V
			I_{OH} = -12 mA	1,2,3	01,02 06,07	2.4		
			I_{OH} = -8 mA	1,2,3	03,04 05	2.4		
Output low voltage	V_{OL}	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300 µA	1,2,3	All		0.2	
			I_{OL} = 12 mA	1,2,3	01,02 06,07		0.5	
			I_{OL} = 8 mA	1,2,3	03,04 05		0.5	
Off state (high impedance) output current	I_{OZ}	V_{CC} = 5.5 V	V_O = 0 V	1,2,3	All		-20	µA
			V_O = 5.5 V	1,2,3	All		20	
Output short circuit current 3/	I_{OS}	V_{CC} = 4.5 V, V_{OUT} = 0 V		1,2,3	All	-30		mA
Quiescent power supply current (CMOS inputs)	I_{CCQ}	V_{CC} = 5.5 V, $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$, f_{OP} = 0 MHz		1,2,3	All		5.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, V_{CC} = 4.5 V to 5.5 V unless otherwise specified		Group A subgroups	Device types	Limits Min	Limits Max	Unit
Quiescent input power supply current (per input at TTL high) 4/	I_{CCT}	V_{CC} = 5.5 V, V_{IN} = 3.4 V, f_{OP} = 0 MHz		1,2,3	All		0.75	mA/ input
Dynamic power supply current	I_{CCD}	V_{CC} = 5.5 V, $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$, outputs open, $\overline{OE}$ = low		1,2,3	All		10	mA/ MHz
Total power supply current 5/	I_{CC}	V_{CC} = 5.5 V, f_{OP} = 10 MHz, outputs open, $\overline{OE}$ = low, 50% duty cycle	$V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$	1,2,3	All		110	mA
			V_{IH} = 3.4 V, V_{IL} = 0.4 V	1,2,3	All		125	
Input capacitance	C_{IN}	See 4.3.1c 6/		4	All		12	pF
Output capacitance	C_{OUT}	See 4.3.1c 6/		4	All		15	
I/O capacitance	$C_{I/O}$	See 4.3.1c 6/		4	All		15	
Functional testing		See 4.3.1d		7,8	All			
Combinational delay, 1-4 Input: $DATA_{0-31}$ Output:		C_L = 50 pF, see figure 6		9,10,11				ns
SC_{0-7}	t_{PD1}				01,03		30	
					02,04		28	
					05,06		22	
					07		17	
$DATA_{0-31}$	t_{PD2} 8/				01,03		39	
					02,04		33	
					05,06		29	
					07		22	
$\overline{ERROR}$	t_{PD3}				01,03		33	
					02,04		28	
					05,06		21	
					07		16	
$\overline{MULT\ ERROR}$	t_{PD4}				01,03		36	
					02,04		30	
					05,06		24	
					07		18	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Combinational delay, 5-8 Input: CB_{0-7} (code ID 00,11) Output:		C_L = 50 pF, see figure 6	9,10,11				ns
SC_{0-7}	t_{PD5}			01,03		19	
				02,04,		17	
				05,06		17	
				07		13	
$DATA_{0-31}$	t_{PD6}			01,03		37	
				02,04		33	
				05,06		23	
				07		17	
$\overline{ERROR}$	t_{PD7}			01,03		22	
				02,04		20	
				05,06		16	
				07		12	
$\overline{MULT\ ERROR}$	t_{PD8}			01,03		26	
				02,04		23	
				05,06		18	
				07		14	
Combination delay, 9-12 Input: CB_{0-7} (code ID 10) Output:							
SC_{0-7}	t_{PD9}			01-04		19	
				05,06		17	
				07		13	
$DATA_{0-31}$	t_{PD10}			01-04		23	
				05,06		18	
				07		14	
$\overline{ERROR}$ 7/ 8/	t_{PD11}			01,02		22	
$\overline{MULT\ ERROR}$ 7/ 8/	t_{PD12}			01,02		24	
Combination delay, 13-16 Input: GENERATE Output:							
SC_{0-7}	t_{PD13}			01-04		24	
				05,06		20	
				07		15	
$DATA_{0-31}$ 7/ 8/	t_{PD14}			01,02		26	
$\overline{ERROR}$	t_{PD15}			01,03		28	
				02,04		26	
				05,06		10	
				07		08	
$\overline{MULT\ ERROR}$	t_{PD16}			01,03		28	
				02,04		26	
				05,06		12	
				07		9	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Combinational delay, 17 Input: CORRECT (not internal control mode)		C_L = 50 pF, see figure 6	9,10,11				ns
Output:							
$DATA_{0-31}$	t_{PD17}			01-04		26	
				05,06		17	
				07		13	
Combinational delay, 18-21 Input: DIAG $MODE_{0,1}$ (not internal control mode)							
Output:							
SC_{0-7}	t_{PD18}			01-04		20	
				05,06		18	
				07		14	
$DATA_{0-31}$	t_{PD19}			01-06		29	
				07		22	
$\overline{ERROR}$	t_{PD20}			01-04		23	
				05,06		12	
				07		12	
$\overline{MULT\ ERROR}$	t_{PD21}			01-04		27	
				05,06		23	
				07		17	
Combinational delay, 22-25 Input: CODE $ID_{0,1}$							
Output:							
SC_{0-7}	t_{PD22} 8/			01-06		21	
				07		16	
$DATA_{0-31}$	t_{PD23} 7/			01-04		29	
				05,06		26	
				07		20	
$\overline{ERROR}$	t_{PD24}			01-04		24	
				05,06		20	
				07		15	
$\overline{MULT\ ERROR}$	t_{PD25}			01-04		29	
				05,06		24	
				07		18	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Combinational delay, 26-29 Input: LE_{IN} (from latched to transparent)		C_L = 50 pF, see figure 6	9,10,11				ns
Output:							
SC_{0-7}	t_{PD26}			01-04 05,06 07		30 24 18	
$DATA_{0-31}$	t_{PD27} 7/			01-04 05,06 07		41 32 24	
$\overline{ERROR}$	t_{PD28}			01-04 05,06 07		33 21 16	
$\overline{MULT\ ERROR}$	t_{PD29}			01-04 05,06 07		36 25 19	
Combinational delay, 30 Input: LE_{OUT} (from latched to transparent)							
Output: $DATA_{0-31}$	t_{PD30}			01-04 05,06 07		15 13 10	
Combinational delay, 31-34 Input: LE_{DIAG} (from latched to transparent; not internal control mode)							
Output:							
SC_{0-7}	t_{PD31} 8/			01-06 07		18 14	
$DATA_{0-31}$	t_{PD32}			01-04 05,06 07		32 27 20	
$\overline{ERROR}$	t_{PD33}			01-04 05,06 07		22 17 13	
$\overline{MULT\ ERROR}$	t_{PD34}			01-04 05,06 07		25 21 16	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Combinational delay, 35-38 Input: Internal control mode, LE_{DIAG} (from latched to transparent)		C_L = 50 pF, see figure 6	9,10,11				ns
Output:							
SC_{0-7}	t_{PD35} 8/			01-06		19	
				07		14	
$DATA_{0-31}$	t_{PD36}			01-04		35	
				05,06		25	
				07		19	
$\overline{ERROR}$	t_{PD37}			01-04		22	
				05,06		18	
				07		14	
$\overline{MULT\ ERROR}$	t_{PD38}			01-04		27	
				05,06		21	
				07		16	
Combinational delay, 39-42 Input: Internal control mode, $DATA_{0-31}$ (via diagnostic latch)							
Output:							
SC_{0-7}	t_{PD39}			01-04		19	
				05,06		18	
				07		14	
$DATA_{0-31}$	t_{PD40} 8/			01,02		35	
				03-06		29	
				07		22	
$\overline{ERROR}$	t_{PD41}			01-04		23	
				05,06		14	
				07		11	
$\overline{MULT\ ERROR}$	t_{PD42}			01-04		28	
				05,06		18	
				07		14	
Setup time 1 Hold time 1 Input: $DATA_{0-31}$ To: LE_{IN}	t_{s1}	Setup and hold times relative to latch enables		01,03	5.0		
				02,04	4.0		
				05,06	3.0		
				07	3.0		
	t_{h1}	C_L = 50 pF, see figure 6		01-06	4.0		
				07	3.0		
Setup time 2 Hold time 2 Input: CB_{0-7} To: LE_{IN}	t_{s2}			01,03	5.0		
				02,04	4.0		
				05,06	2.0		
				07	2.0		
	t_{h2}			01-06	4.0		
				07	3.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Setup time 3 Hold time 3 8/ Input: $DATA_{0-31}$ To: LE_{OUT}	t_{s3}	Setup and hold times relative to latch enables C_L = 50 pF, see figure 6	9,10,11	01,03 02,04 05,06 07	27 23 7 6		ns
	t_{h3}			All	0		
Setup time 4 Hold time 4 Input: CB_{0-7} (CODE ID 00,11) To: LE_{OUT}	t_{s4}			01-04 05,06 07	18 16 12		
	t_{h4}			All	0		
Setup time 5 Hold time 5 Input: CB_{0-7} (CODE ID 10) To: LE_{OUT}	t_{s5}			01-04 05,06 07	18 10 8		
	t_{h5}			All	0		
Setup time 6 Hold time 6 Input: CORRECT To: LE_{OUT}	t_{s6}			01-04 05,06 07	14 9 7		
	t_{h6}			All	0		
Setup time 7 Hold time 7 Input: $DIAG\ MODE_{0,1}$ To: LE_{OUT}	t_{s7}			01-04 05,06 07	20 19 14		
	t_{h7}			All	0		
Setup time 8 Hold time 8 Input: $CODE\ ID_{0,1}$ To: LE_{OUT}	t_{s8}			01-04 05,06 07	20 12 9		
	t_{h8}			All	0		
Setup time 9 Hold time 9 Input: LE_{IN} To: LE_{OUT}	t_{s9}			01,03 02,04 05,06 07	28 23 21 16		
	t_{h9} 7/			All	0		
Setup time 10 8/ Hold time 10 Input: $DATA_{0-31}$ To: LE_{DIA}	t_{s10}			01,03 02,04 05,06 07	5.0 4.0 3.0 3.0		
	t_{h10}			All	3.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Enable time 1 Disable time 1 From: $\overline{OE}$ $BYTE_{0-3}$ To: $DATA_{0-31}$	t_{en1}	C_L = 5.0 pF 8/ 9/ See figure 6	9,10,11	01,02, 06	0	12	ns
				03,04, 05	10	25	
				07	0	10	
	t_{dis1}			01,02, 06	0	14	
				03,04, 05	10	21	
				07	0	12	
Enable time 2 Disable time 1 From: $\overline{OE}_{SC}$ To: SC_{0-7}	t_{en2}			01,02, 06	0	12	
				03,04, 05	10	27	
				07	0	10	
	t_{dis2}			01,02, 06	0	14	
				03,04, 05	10	22	
				07	0	12	
Minimum pulse widths; 8/ LE_{IN}, LE_{OUT}, LE_{DIAG}	t_{pw}	C_L = 50 pF, see figure 6	9,10,11	01-04 05,06 07	12 6 5		

See footnotes on next page.

1/ $V_{HC} = V_{CC}-0.2$ V and $V_{LC} = 0.2$ V, unless otherwise specified. All testing to be performed using worst-case test conditions unless otherwise specified.

2/ These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

3/ Not more than one output should be shorted at a time. Duration of short circuit test should not exceed 1 second.

4/ I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4 V, subtracting out I_{CCQ}, then dividing by the total number of inputs.

5/ Total supply current is the sum of the quiescent current and the dynamic current (at either CMOS or TTL input levels). For all conditions, the total supply current can be calculated by using the following equation:

$I_{CC} = I_{CCQ} + I_{CCT} (N_T \times D_H) + I_{CCD} (f_{OP})$, where;

D_H = Data duty cycle TTL high period ($V_{IN} = 3.4$ V).

N_T = Number of dynamic inputs driven at TTL levels.

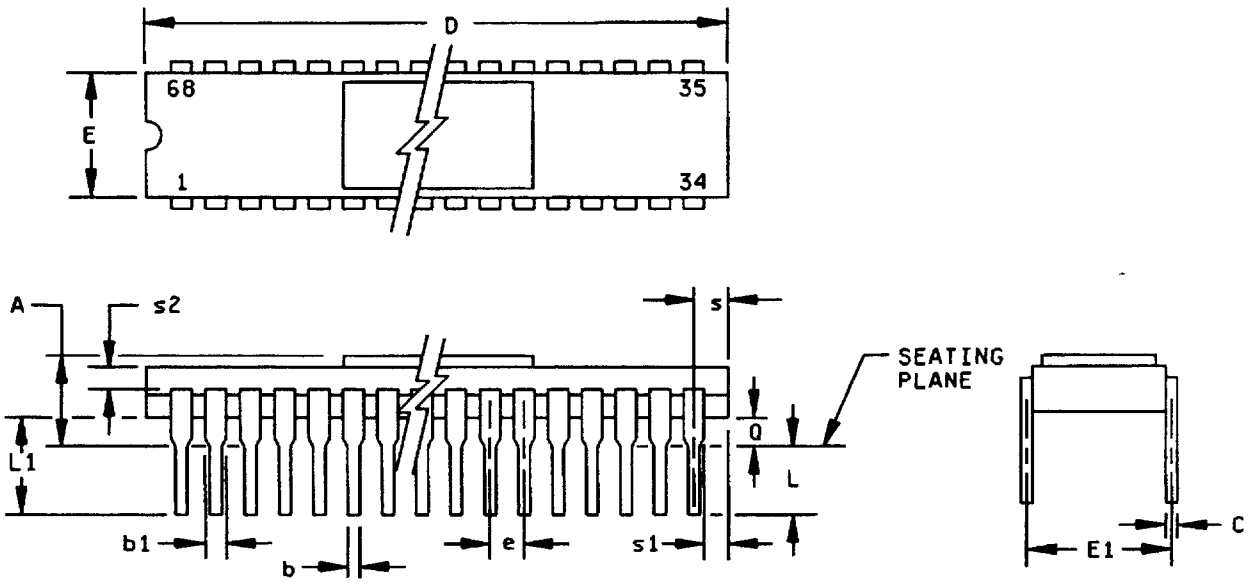
f_{OP} = Operating frequency in megahertz.

6/ The capacitance measurements shall be made between the indicated terminal and ground at a frequency of 1 MHz, and $T_C = +25°C$. The dc bias of the measuring instrument shall be less than ±0.1 V. The ac signal amplitude shall be less than 50 mV rms.

7/ Guaranteed to the limits specified herein for device types 03, 04, and 05.

8/ Guaranteed, if not tested, to the limits specified herein.

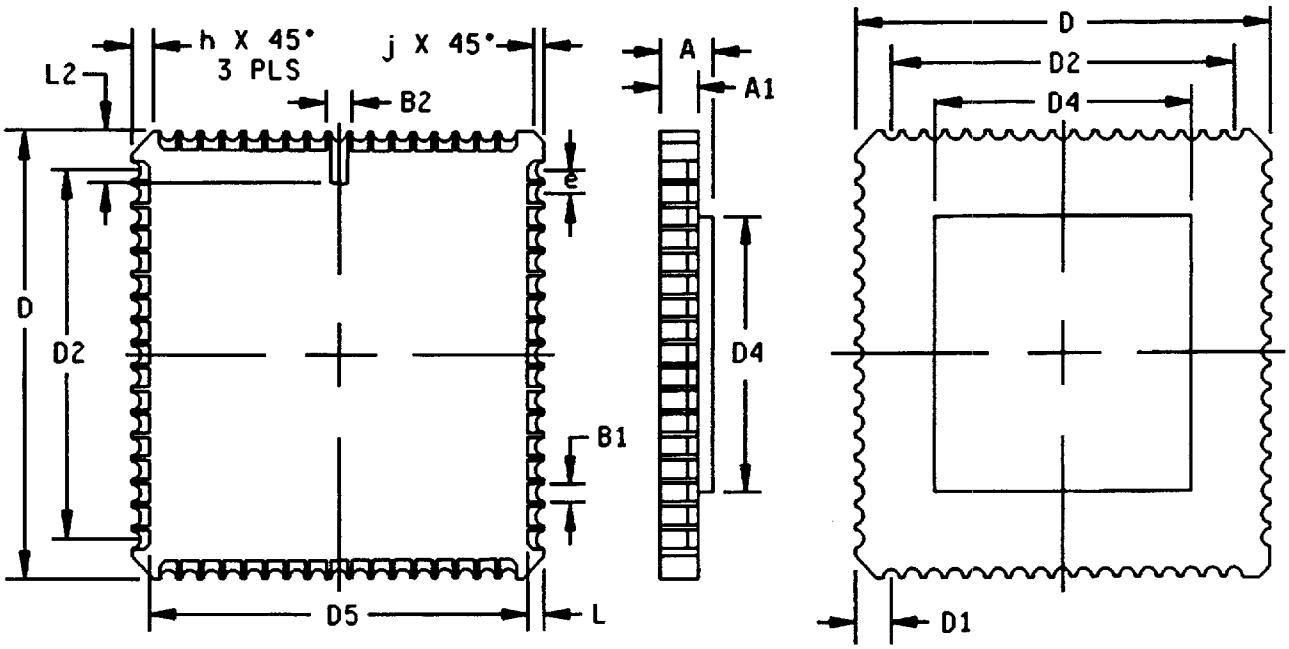
9/ Output disable tests are performed with $C_L = 5.0$ pF and are measured to 0.5 V change of output voltage level.



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.085	.190	2.16	4.826
b	.014	.023	0.36	0.58
b1	.030	.060	0.76	1.52
C	.008	.015	0.20	0.38
D	2.380	2.440	60.45	61.98
E	.580	.610	14.73	15.49
E1	.590	.620	14.99	15.75

Symbol	Inches		Millimeter	
	Min	Max	Min	Max
e	.070 BSC		1.78 BSC	
L	.125	.200	3.18	5.08
L1	.150		3.81	
Q	.020	.070	0.51	1.78
S	.030	.065	0.77	1.66
S1	.005		0.12	
S2	.005		0.12	

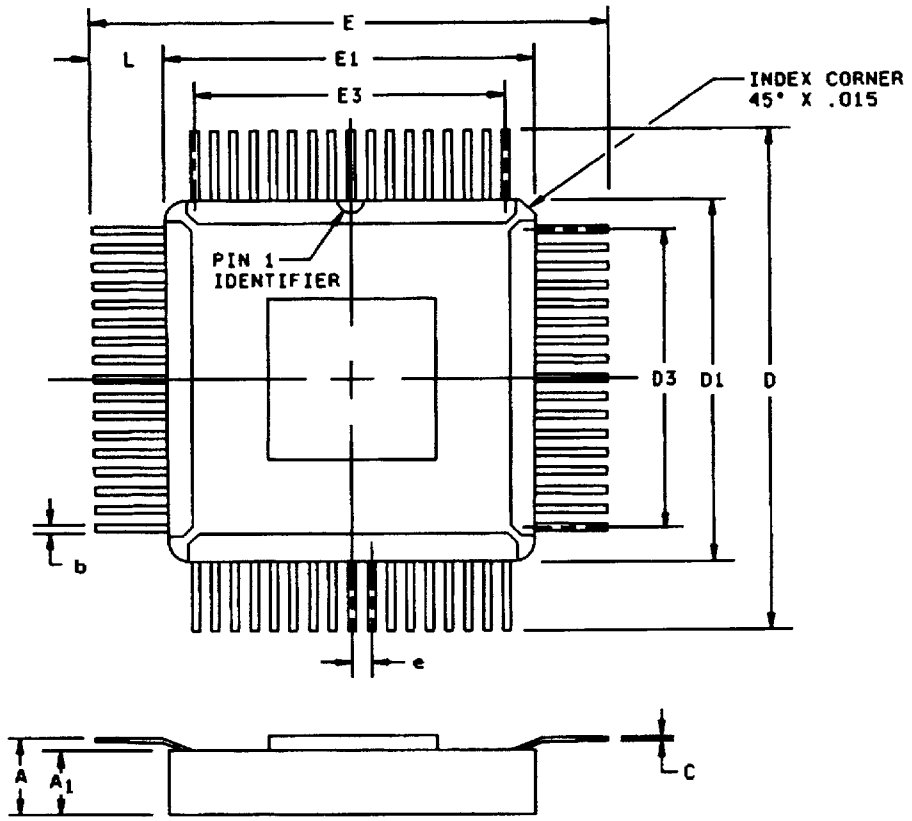
FIGURE 1. Case outline X.



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.065	.120	1.65	3.05
A1	.055	.075	1.40	1.91
B1	.008	.014	0.20	0.36
B2	.008	.024	0.20	0.61
D	.554	.566	14.07	14.38
D1	.080 REF		2.03 REF	
D2	.400 BSC		10.16 BSC	

Symbol	Inches		Millimeter	
	Min	Max	Min	Max
D4		.535		13.59
D5	.430 REF		10.92 REF	
e	.025 BSC		0.64 BSC	
h	.040 REF		1.02 REF	
j	.020 REF		0.51 REF	
L	.045	.055	1.14	1.40
L2	.077	.093	1.96	2.36

Figure 2. Case outline Z.



NOTE: Dimensions are in inches, BSC = Basic lead spacing between centers.

No of leads (N)	68			
Symbol	Min	Max	Min	Max
	INCHES		MILLIMETERS	
A	.064	.084	1.63	2.13
A1	.054	.070	1.37	1.78
b	.008	.013	0.20	0.33
c	.0045	.008	0.11	0.20
D/E	.860	1.100	21.84	27.94
D1/E1	.460	.500	11.68	12.70
D3/E3	.400 REF		10.16 REF	
e	.025 BSC		0.64 BSC	
L	.200	.300	5.08	7.62
ND/NE	17		17	

Figure 3. Case outline T.

Case T

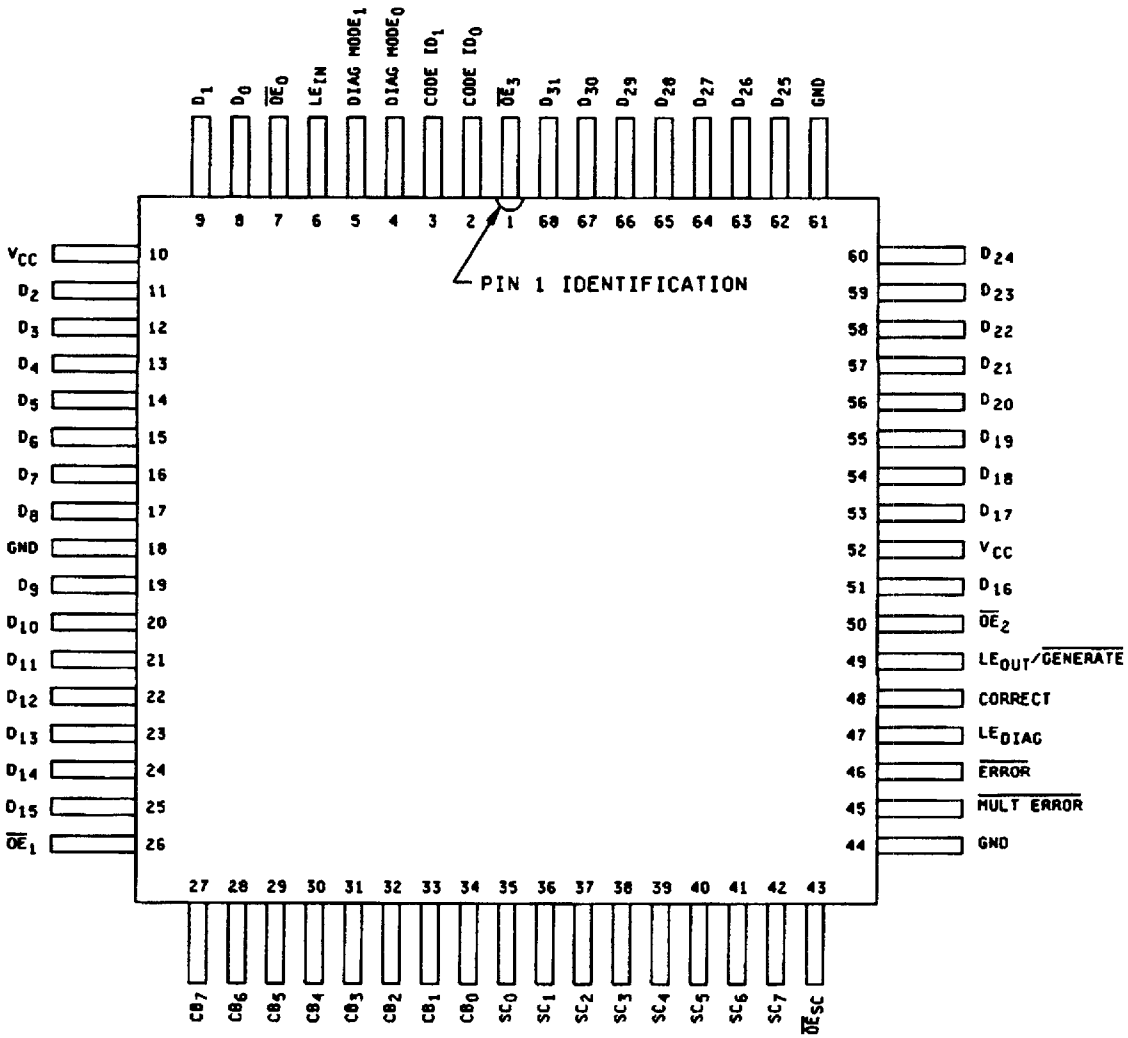


Figure 4. Terminal connections.

Case U

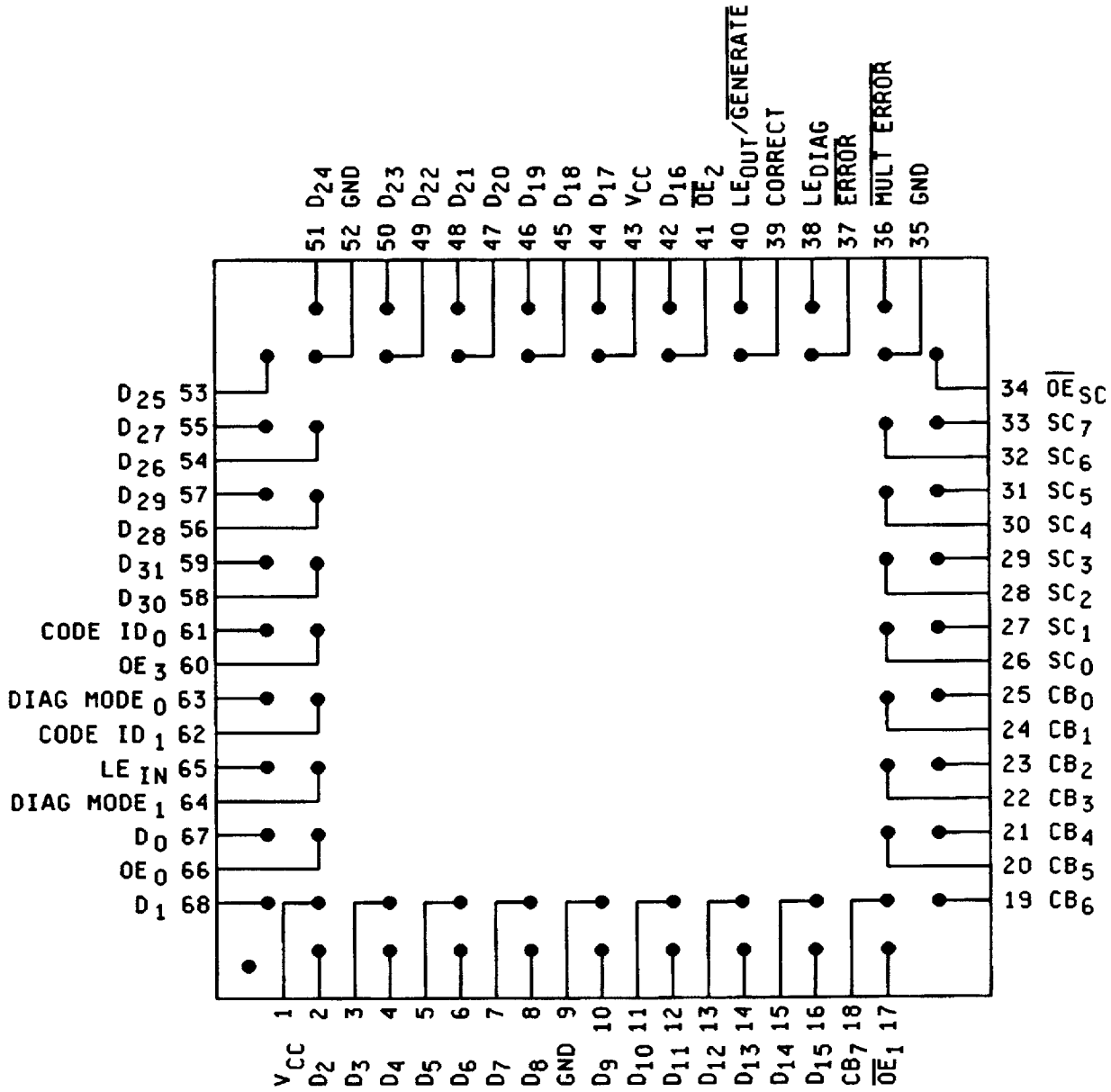


Figure 4. Terminal connections. - Continued

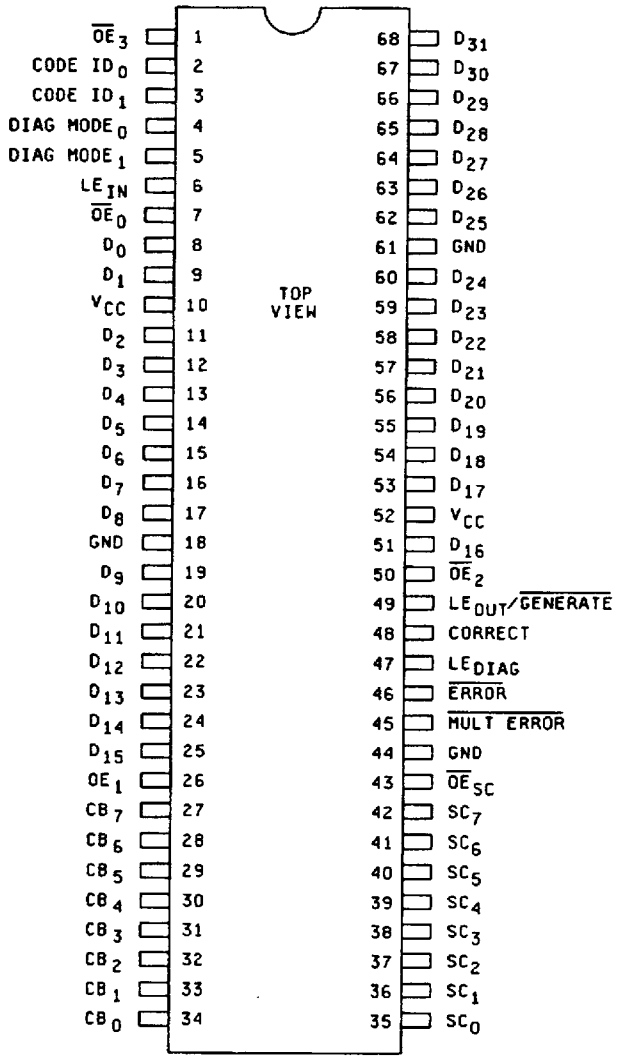


Figure 4. Terminal connections. - Continued

Case Y and Z

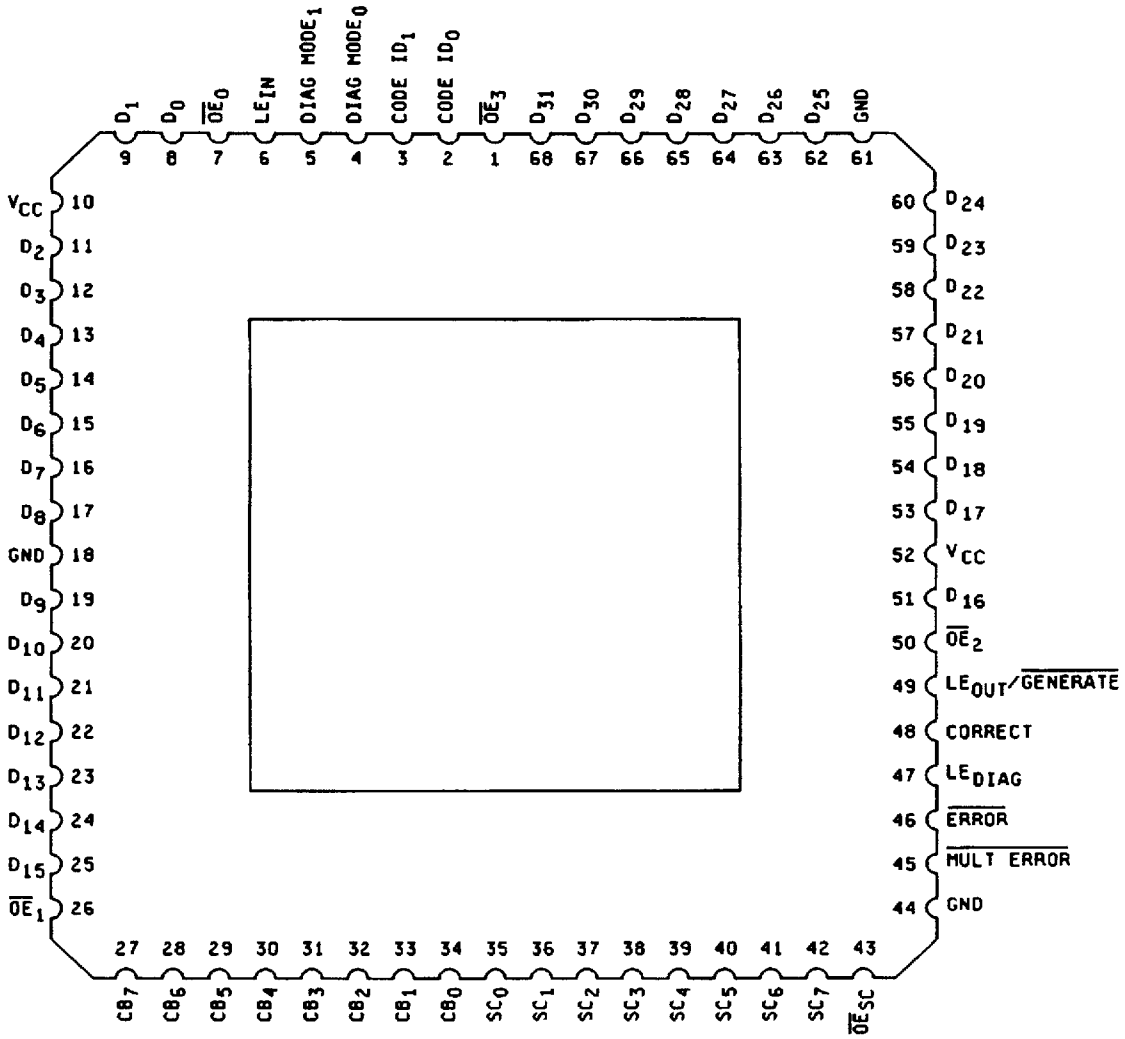


Figure 4. Terminal connections. - Continued

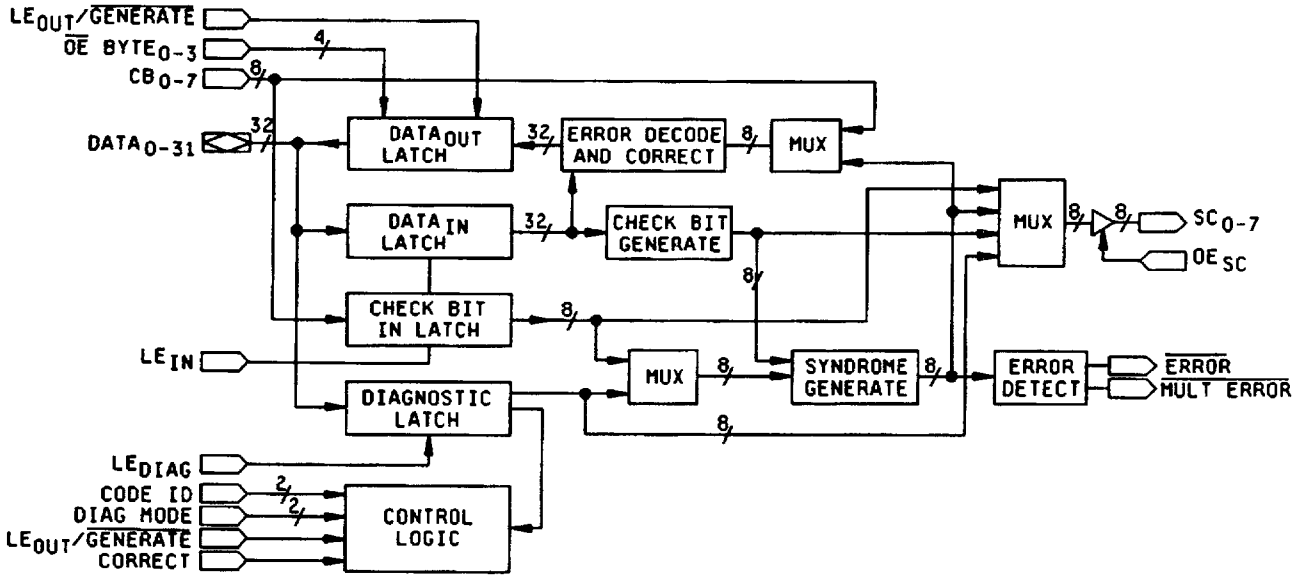
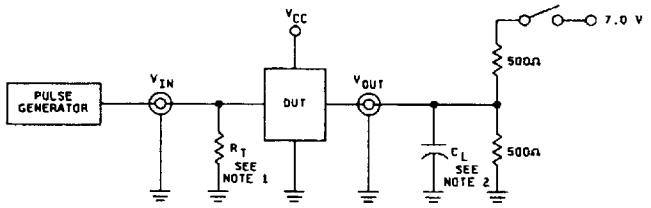


Figure 5. Block diagram.

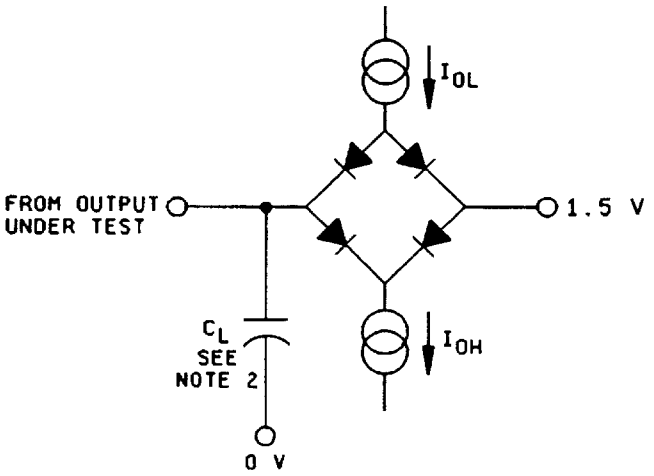
Load circuit, device types 01, 02, 06, and 07



Test	Switch
Open drain Disable low Enable low	Closed
All other output	Open

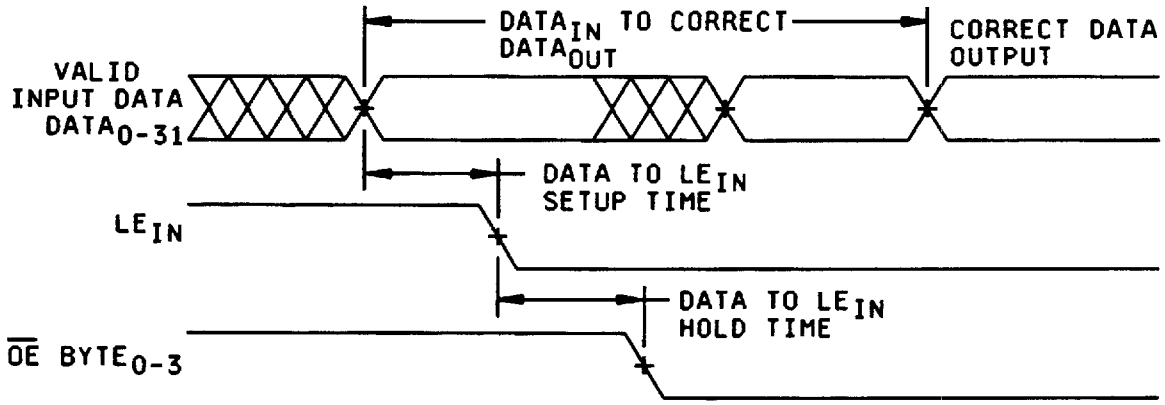
NOTES:
1. R_T = Termination resistor which should be equal to Z_{OUT} of pulse generator.
2. C_L = load capacitance; includes jig and probe capacitance.
3. All timing measurements are measured at the 1.5 V signal level.

Load circuit, device types 03 through 05



NOTES:
1. C_L = 50 P_F for all test except output enable/disable (includes scope probe, wiring, and stray capacitance without device in test fixture).
2. C_L = 5 P_F for output enable/disable test.

Figure 6. AC testing output load circuits and waveforms.



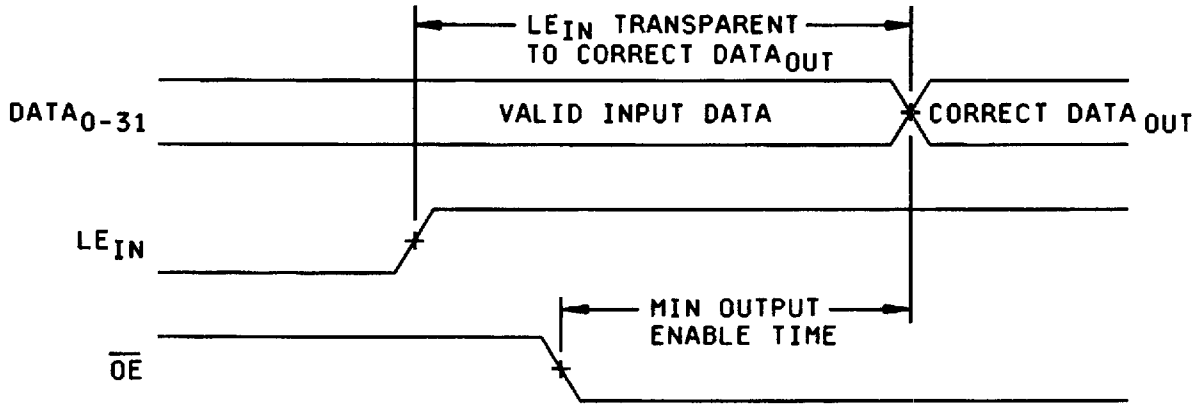


Figure 6. AC testing output load circuits and waveforms - Continued

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall include the requirements for inputs, outputs, biases, and power dissipation, as applicable, in accordance with the specified purpose of method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3 ,4, 7 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8a, 10

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}, C_{OUT} and $C_{I/O}$ measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance or output capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

d. Subgroups 7 and 8 testing shall be sufficient to verify functional operation of the device. These test form a part of the manufacturer's test tape and shall be maintained and available from the approved source of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.