REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
SHEET																								
REV																								
SHEET	22	23																						
REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21		

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY

CHECKED BY

APPROVED BY

DRAWING APPROVAL DATE
19 MAY 1989

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS, 16-BIT SLICE MICROPROCESSOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-89517

SHEET 1 OF 23

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1153

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-89517	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Cycle time
01	7C9101-45	16-bit microprocessor slice	45 ns
02	7C9101-35	16-bit microprocessor slice	35 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
U	See figure 1 (64-lead, .915" x .915" x .090"), quad flat package
X	See figure 2 (64-lead, 3.240" x .920" x .225"), dual-in-line package
Y	C-7 (68-terminal, .962" x .962" x .120"), square chip carrier package
Z	P-BC (68-pin, 1.135" x 1.135" x .345"), pin grid array

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs in high Z state	-0.5 V dc to +7.0 V dc
DC input voltage	-3.0 V dc to +7.0 V dc
DC output current	30 mA
Maximum power dissipation 1/	1.0 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case U	22°C/W
Case X	28°C/W
Cases Y and Z	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input high voltage range (V_{IH})	2.0 V dc to 6.0 V dc
Input low voltage range (V_{IL})	-0.5 V dc to +0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 3.

3.2.2 Functional block diagram. The functional block diagram shall be as specified on figure 4.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.5 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -3.4 mA	All	1, 2, 3	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 16.0 mA	All	1, 2, 3		0.4	V
Input high voltage	V_{IH}		All	1, 2, 3	2.0		V
Input low voltage	V_{IL}		All	1, 2, 3		0.8	V
Input leakage current	I_{IX}	V_{CC} = 5.5 V $GND \le V_{IN} \le V_{CC}$	All	1, 2, 3		±10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V $GND \le V_{OUT} \le V_{CC}$	All	1, 2, 3		±40	µA
Output short circuit current 1/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = GND	All	1, 2, 3		-85	mA
Operating supply current	I_{CC1}	V_{CC} = 5.5 V, f_{CP} = 10 MHz 3/ V_{IL} = 0.8 V, V_{IH} = 2.0 V CP = 50% duty cycle, $\overline{OE}$ = 2.0 V	All	1, 2, 3		85	mA
Quiescent supply current TTL levels	I_{CC2}	V_{CC} = 5.5 V V_{IL} = 0.8 V, V_{IH} = 2.0 V $\overline{OE}$ = 2.0 V	All	1, 2, 3		35	mA
Quiescent supply current CMOS levels	I_{CC3}	V_{CC} = 5.5 V V_{IL} = 0.4 V, V_{IH} = 3.85 V $\overline{OE}$ = 3.85 V	All	1, 2, 3		30	mA
Input capacitance	C_{IN}	See 4.3.1c, V_{CC} = 5.0 V	All	4		12	pF
Output capacitance	C_{OUT}					15	pF
Functional tests		See 4.3.1d	All	7, 8			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
A setup time to positive edge of clock 4/	t_{S1}	See figure 5 2/	01	9, 10, 11	45		ns
			02		35		
A setup time to negative edge of clock 4/	t_{S2}		01	9, 10, 11	17		ns
			02		12		
B (source) setup time to positive edge of clock 4/	t_{S3}		01	9, 10, 11	45		ns
			02		35		
B (source) setup time to negative edge of clock 4/	t_{S4}		01	9, 10, 11	17		ns
			02		12		
B (destination) setup time to negative edge of clock	t_{S5}		01	9, 10, 11	17		ns
			02		12		
Data setup time to positive edge of clock	t_{S6}		01	9, 10, 11	30		ns
			02		25		
C_n setup time to positive edge of clock	t_{S7}		01	9, 10, 11	24		ns
			02		19		
I_0, I_1, I_2 setup time to positive edge of clock	t_{S8}		01	9, 10, 11	37		ns
			02		30		
I_3, I_4, I_5 setup time to positive edge of clock	t_{S9}		01	9, 10, 11	40		ns
			02		33		
I_6, I_7, I_8 setup time to negative edge of clock	t_{S10}		01	9, 10, 11	16		ns
			02		12		
RAM_0, RAM_{15}, Q_0, Q_{15} setup time to positive edge of clock	t_{S11}		01	9, 10, 11	15		ns
			02		13		
A hold time from positive edge of clock	t_{H1}		01	9, 10, 11	0		ns
			02		0		

See footnotes at end of table.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—549-904

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
A hold time from negative edge of clock 5/	t_{H2}	See figure 5 2/	01	9, 10, 11	3		ns
			02		3		
B (source) hold time from positive edge of clock	t_{H3}		01	9, 10, 11	0		ns
			02		0		
B (source) hold time from negative edge of clock 5/	t_{H4}		01	9, 10, 11	3		ns
			02		3		
B (destination) hold time from positive edge of clock	t_{H5}		01	9, 10, 11	1		ns
			02		1		
Data hold time from positive edge of clock	t_{H6}		01	9, 10, 11	0		ns
			02		0		
C_n hold time from positive edge of clock	t_{H7}		01	9, 10, 11	0		ns
			02		0		
I_0, I_1, I_2 hold time from positive edge of clock	t_{H8}		01	9, 10, 11	0		ns
			02		0		
I_3, I_4, I_5 hold time from positive edge of clock	t_{H9}		01	9, 10, 11	0		ns
			02		0		
I_6, I_7, I_8 hold time from positive edge of clock	t_{H10}		01	9, 10, 11	0		ns
			02		0		
RAM_0, RAM_{15}, Q_0, Q_{15} hold time from positive edge of clock	t_{H11}		01	9, 10, 11	1		ns
			02		1		
Delay from A to Y	t_{p1}		01	9, 10, 11		52	ns
			02			41	
Delay from A to F_{15}	t_{p2}		01	9, 10, 11		51	ns
			02			40	

See footnotes at end of table.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—549-904

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Delay from A to C_{n+16}	t_{P3}	See figure 5 2/	01	9, 10, 11		48	ns
			02			38	
Delay from A to $\overline{G}$ and $\overline{P}$	t_{P4}		01	9, 10, 11		45	ns
			02			37	
Delay from A to F = 0	t_{P5}		01	9, 10, 11		48	ns
			02			40	
Delay from A to OVR	t_{P6}		01	9, 10, 11		46	ns
			02			36	
Delay from A to RAM_0, RAM_{15}	t_{P7}		01	9, 10, 11		43	ns
			02			36	
Delay from B to Y	t_{P8}		01	9, 10, 11		52	ns
			02			41	
Delay from B to F_{15}	t_{P9}		01	9, 10, 11		51	ns
			02			40	
Delay from B to C_{n+16}	t_{P10}		01	9, 10, 11		48	ns
			02			38	
Delay from B to $\overline{G}$ and $\overline{P}$	t_{P11}		01	9, 10, 11		45	ns
			02			37	
Delay from B to F = 0	t_{P12}		01	9, 10, 11		48	ns
			02			40	
Delay from B to OVR	t_{P13}		01	9, 10, 11		46	ns
			02			36	
Delay from B to RAM_0, RAM_{15}	t_{P14}		01	9, 10, 11		43	ns
			02			36	

See footnotes at end of table.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—549-904

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Delay from data to Y	t_{P15}	See figure 5 2/	01	9, 10, 11		37	ns
			02			31	
Delay from data to F_{15}	t_{P16}		01	9, 10, 11		36	ns
			02			31	
Delay from data to $C_n + 16$	t_{P17}		01	9, 10, 11		36	ns
			02			29	
Delay from data to $\overline{G}$ and $\overline{P}$	t_{P18}		01	9, 10, 11		32	ns
			02			28	
Delay from data to F = 0	t_{P19}		01	9, 10, 11		40	ns
			02			33	
Delay from data to OVR	t_{P20}		01	9, 10, 11		32	ns
			02			23	
Delay from data to RAM_0, RAM_{15}	t_{P21}		01	9, 10, 11		35	ns
			02			30	
Delay from C_n to Y	t_{P22}		01	9, 10, 11		30	ns
			02			25	
Delay from C_n to F_{15}	t_{P23}		01	9, 10, 11		29	ns
			02			24	
Delay from C_n to $C_n + 16$	t_{P24}		01	9, 10, 11		27	ns
			02			23	
Delay from C_n to F = 0	t_{P26}		01	9, 10, 11		29	ns
			02			24	
Delay from C_n to OVR	t_{P27}		01	9, 10, 11		27	ns
			02			23	

See footnotes at end of table.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—549-904

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Delay from C_n to RAM_0, RAM_{15}	t_{P28}	See figure 5 2/	01	9, 10, 11		31	ns
			02			26	
Delay from I_0, I_1, I_2 to Y	t_{P29}		01	9, 10, 11		44	ns
			02			36	
Delay from I_0, I_1, I_2 to F_{15}	t_{P30}		01	9, 10, 11		43	ns
			02			35	
Delay from I_0, I_1, I_2 to C_{n+16}	t_{P31}		01	9, 10, 11		41	ns
			02			33	
Delay from I_0, I_1, I_2 to $\overline{G}$ and $\overline{P}$	t_{P32}		01	9, 10, 11		38	ns
			02			31	
Delay from I_0, I_1, I_2 to F = 0	t_{P33}		01	9, 10, 11		46	ns
			02			38	
Delay from I_0, I_1, I_2 to OVR	t_{P34}		01	9, 10, 11		38	ns
			02			29	
Delay from I_0, I_1, I_2 to RAM_0, RAM_{15}	t_{P35}		01	9, 10, 11		38	ns
			02			30	
Delay from I_3, I_4, I_5 to Y	t_{P36}		01	9, 10, 11		48	ns
			02			38	
Delay from I_3, I_4, I_5 to F_{15}	t_{P37}		01	9, 10, 11		47	ns
			02			37	
Delay from I_3, I_4, I_5 to C_{n+16}	t_{P38}		01	9, 10, 11		46	ns
			02			37	
Delay from I_3, I_4, I_5 to $\overline{G}$ and $\overline{P}$	t_{P39}		01	9, 10, 11		38	ns
			02			31	

See footnotes at end of table.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—549-904

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Delay from I_3, I_4, I_5 to F = 0	t_{P40}	See figure 5 2/	01	9, 10, 11		45	ns
			02			38	
Delay from I_3, I_4, I_5 to OVR	t_{P41}		01	9, 10, 11		45	ns
			02			36	
Delay from I_3, I_4, I_5 to RAM_0, RAM_{15}	t_{P42}		01	9, 10, 11		41	ns
			02			33	
Delay from I_6, I_7, I_8 to Y	t_{P43}		01	9, 10, 11		24	ns
			02			21	
Delay from I_6, I_7, I_8 to RAM_0, RAM_{15}	t_{P44}		01	9, 10, 11		28	ns
			02			24	
Delay from I_6, I_7, I_8 to Q_0, Q_{15}	t_{P45}		01	9, 10, 11		28	ns
			02			24	
Delay from A (I = 2XX) to Y	t_{P46}		01	9, 10, 11		33	ns
			02			28	
Delay from CP to Y	t_{P47}		01	9, 10, 11		44	ns
			02			35	
Delay from CP to F_{15}	t_{P48}		01	9, 10, 11		43	ns
			02			34	
Delay from CP to C_{n+16}	t_{P49}		01	9, 10, 11		42	ns
			02			34	
Delay from CP to $\overline{G}$ and $\overline{P}$	t_{P50}		01	9, 10, 11		37	ns
			02			30	
Delay from CP to F = 0	t_{P51}		01	9, 10, 11		40	ns
			02			34	

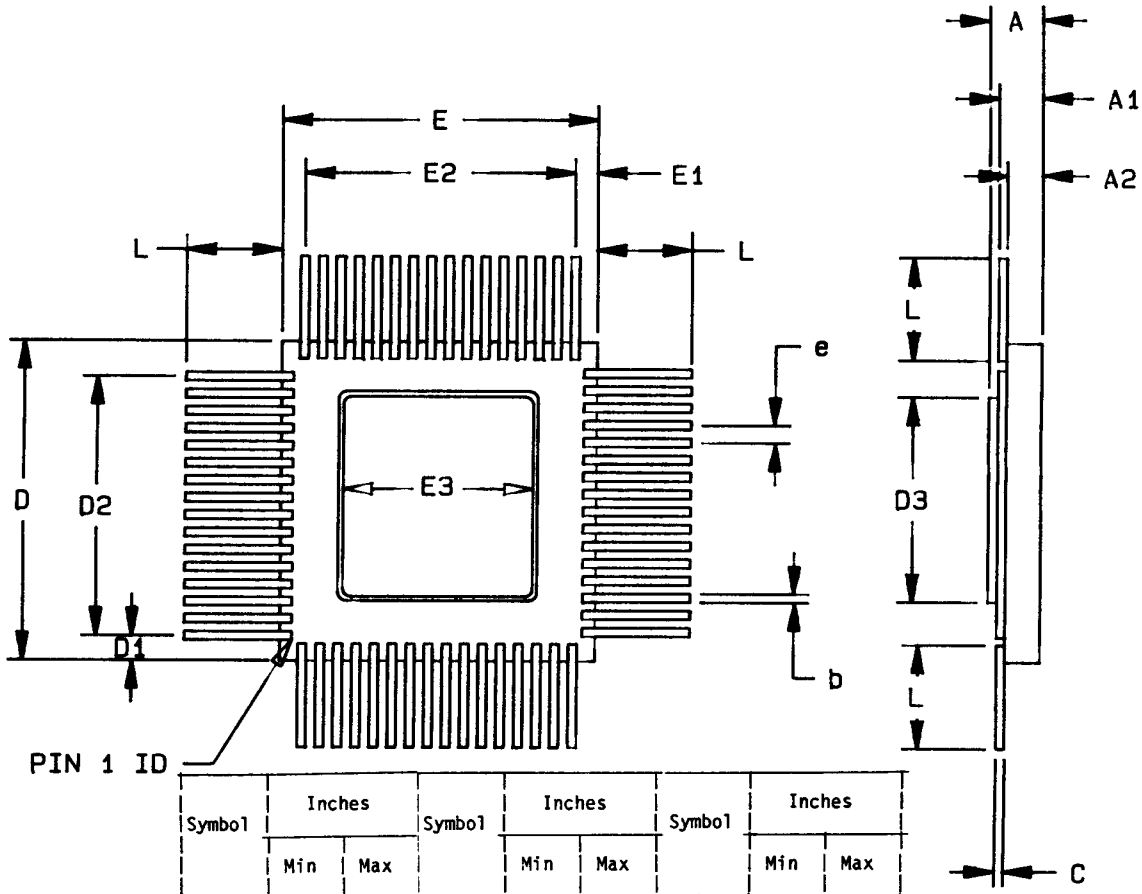
See footnotes at end of table.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—549-904

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Delay from CP to OVR	t_{P52}	See figure 5 2/	01	9, 10, 11		38	ns
			02			28	
Delay from CP to RAM_0, RAM_{15}	t_{P53}		01	9, 10, 11		37	ns
			02			30	
Delay from CP to Q_0, Q_{15}	t_{P54}		01	9, 10, 11		25	ns
			02			21	
Delay from $\overline{OE}$ to Y enable 6/ 7/	t_{PZL} t_{PZH}		01	9, 10, 11		23	ns
			02			20	
Delay from $\overline{OE}$ to Y disable 6/ 7/	t_{PLZ} t_{PHZ}		01	9, 10, 11		20	ns
			02			17	
Minimum clock low time	t_{PWL}		01	9, 10, 11		28	ns
			02			23	
Minimum clock high time	t_{PWH}		01	9, 10, 11		17	ns
			02			12	
Minimum clock period	t_{CP}		01	9, 10, 11		45	ns
			02			35	

1/ For test purposes, not more than one output should be shorted at one time. Duration of the short circuit should not exceed 1 second.
2/ AC parameters are tested using input rise and fall times of 5 ns and input pulse levels of GND to 3.0 V. Both input and output timing reference levels are 1.5 V, and the load is shown on figure 5.
3/ Two quiescent figures are given for different input voltage ranges. To calculate I_{CC} at any given clock frequency, use I_{CC2} or $I_{CC3} + I_{CC}(ac)$, where $I_{CC}(ac) = (5\ mA/MHz) \times$ clock frequency.
4/ The setup time prior to the clock low to high transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock low to high transition, regardless of when the clock high to low transition occurs.
5/ Source addresses must be stable prior to the clock high to low transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock low time.
6/ This parameter if not tested, shall be guaranteed to the limits specified in table I.
7/ Output disable tests performed with $C_L = 5$ pF and measured to 0.5 V change of output voltage level.



Symbol	Inches		Symbol	Inches		Symbol	Inches	
	Min	Max		Min	Max		Min	Max
A	.070	.090	D1	.075 REF		D2	.750 BSC	
A1	.060	.078	D2	.750 BSC		E3	.505	.535
A2	.030	.045	D3	.505	.535	L	.350	.450
b	.016	.020	e	.050 BSC		ND	16	
C	.009	.012	E	.885	.915	NE	16	
D	.885	.915	E1	.075 REF				

NOTES:
1. All dimensions are in inches unless otherwise stated.
2. BSC - Basic pin spacing between centers.

FIGURE 1. Case U (64-lead, .915" x .915" x .090".

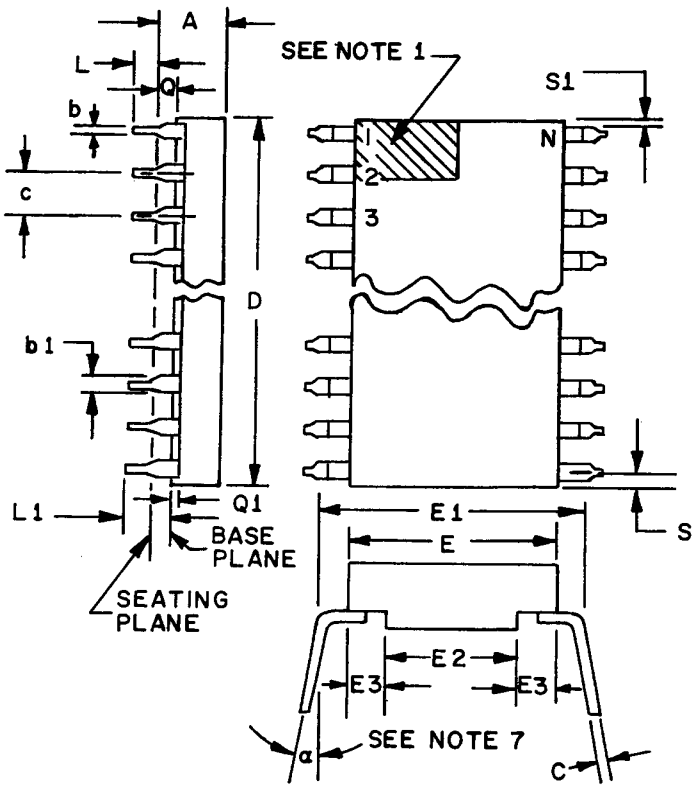


FIGURE 2. Case X (64-lead, 3.240" x 0.920" x 0.225"), dual-in-line package.

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	---	.225	---	5.72	
b	.014	.023	0.36	0.58	8
b1	.038	.065	0.96	1.65	2,8
c	.008	.015	0.20	0.38	8
D	---	3.24	---	82.30	4
E	.780	.820	19.81	20.83	4
E1	.870	.920	22.10	23.37	7
E2	.600	---	15.24	---	
E3	.050	---	1.27	---	

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
e	.100 BSC		2.54 BSC		5,9
L	.125	.200	3.18	5.08	
L1	.150	---	3.81	---	
Q	.080	.110	2.03	2.79	3
Q1	.020	---	.51	---	
S	---	.100	---	2.54	6
S1	.005	---	0.13	---	6
a	0°	15°	0°	15°	

NOTES:
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b1 may be .023 (0.58 mm) for lead numbers 1, 32, 33, and 64 only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus, and glass overrun.
5. The basic pin spacing is .100 (2.54 mm) between centerlines. Each lead centerline shall be located within +.010 (0.25 mm) of its exact longitudinal position relative to leads 1 and 64.
6. Applies to all four corners (lead numbers 1, 32, 33, and 64) shall apply.
7. Lead center when a is 0°. E1 shall be measured at the centerline of the leads.
8. All leads: Increase maximum limit by .003 (0.08 mm) measured at the center of the flat, when lead finish A or B is applied.
9. Sixty-two.
10. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

FIGURE 2. Case X (64-lead, 3.240" x 0.920" x 0.225"), dual-in-line package - Continued.

Device types	All				Device types	All			
Case outlines	U	X	Y	Z	Case outlines	U	X	Y	Z
Terminal number	Terminal symbol				Terminal number	Terminal symbol			
1	B_0	I_4	I_4	D_1	35	OVR	RAM_0	I_6	Y_{13}
2	B_1	I_5	I_3	D_2	36	$C_n + 16$	CP	I_7	Y_{12}
3	B_2	$\overline{P}$	Q_{15}	D_3	37	$\overline{G}$	B_3	I_8	Y_{11}
4	B_3	$\overline{G}$	RAM_{15}	D_4	38	$\overline{P}$	B_2	I_0	Y_{10}
5	CP	$C_n + 16$	A_3	D_5	39	I_5	B_1	I_1	Y_9
6	RAM_0	OVR	A_2	D_6	40	I_4	B_0	I_2	Y_8
7	Q_0	F_{15}	A_1	D_7	41	I_3	D_0	C_n	GND
8	I_6	Y_{15}	A_0	V_{CC}	42	Q_{15}	D_1	$F = 0$	NC
9	I_7	Y_{14}	D_{15}	NC	43	RAM_{15}	D_2	Y_0	GND
10	I_8	Y_{13}	NC	V_{CC}	44	A_3	D_3	Y_1	$\overline{OE}$
11	I_0	Y_{12}	D_{14}	D_8	45	A_2	D_4	Y_2	Y_7
12	I_1	Y_{11}	D_{13}	D_9	46	A_1	D_5	Y_3	Y_6
13	I_2	Y_{10}	D_{12}	D_{10}	47	A_0	D_6	Y_4	Y_5
14	C_n	Y_9	D_{11}	D_{11}	48	D_{15}	D_7	Y_5	Y_4
15	$F = 0$	Y_8	D_{10}	D_{12}	49	D_{14}	V_{CC}	Y_6	Y_3
16	Y_0	GND	D_9	D_{13}	50	D_{13}	D_8	Y_7	Y_2
17	Y_1	$\overline{OE}$	D_8	D_{14}	51	D_{12}	D_9	$\overline{OE}$	Y_1
18	Y_2	Y_7	V_{CC}	D_{15}	52	D_{11}	D_{10}	GND	Y_0
19	Y_3	Y_6	D_7	A_0	53	D_{10}	D_{11}	GND	$F = 0$
20	Y_4	Y_5	D_6	A_1	54	D_9	D_{12}	Y_8	C_n
21	Y_5	Y_4	D_5	A_2	55	D_8	D_{13}	Y_9	I_2
22	Y_6	Y_3	D_4	A_3	56	V_{CC}	D_{14}	Y_{10}	I_1
23	Y_7	Y_2	D_3	RAM_{15}	57	D_7	D_{15}	Y_{11}	I_0
24	$\overline{OE}$	Y_1	D_2	Q_{15}	58	D_6	A_0	Y_{12}	I_8
25	GND	Y_0	D_1	I_3	59	D_5	A_1	Y_{13}	I_7
26	Y_8	$F = 0$	D_0	I_4	60	D_4	A_2	Y_{14}	I_6
27	Y_9	C_n	NC	I_5	61	D_3	A_3	NC	Q_0
28	Y_{10}	I_2	B_0	$\overline{P}$	62	D_2	RAM_{15}	Y_{15}	RAM_0
29	Y_{11}	I_1	B_1	$\overline{G}$	63	D_1	Q_{15}	F_{15}	CP
30	Y_{12}	I_0	B_2	$Cn + 16$	64	D_0	I_3	OVR	B_3
31	Y_{13}	I_8	B_3	OVR	65	---	---	$C_n + 16$	B_2
32	Y_{14}	I_7	CP	F_{15}	66	---	---	$\overline{G}$	B_1
33	Y_{15}	I_6	RAM_0	Y_{15}	67	---	---	$\overline{P}$	B_0
34	F_{15}	Q_0	Q_0	Y_{14}	68	---	---	I_5	D_0

NC = no connection

FIGURE 3. Terminal connections.

Case Z

Top view

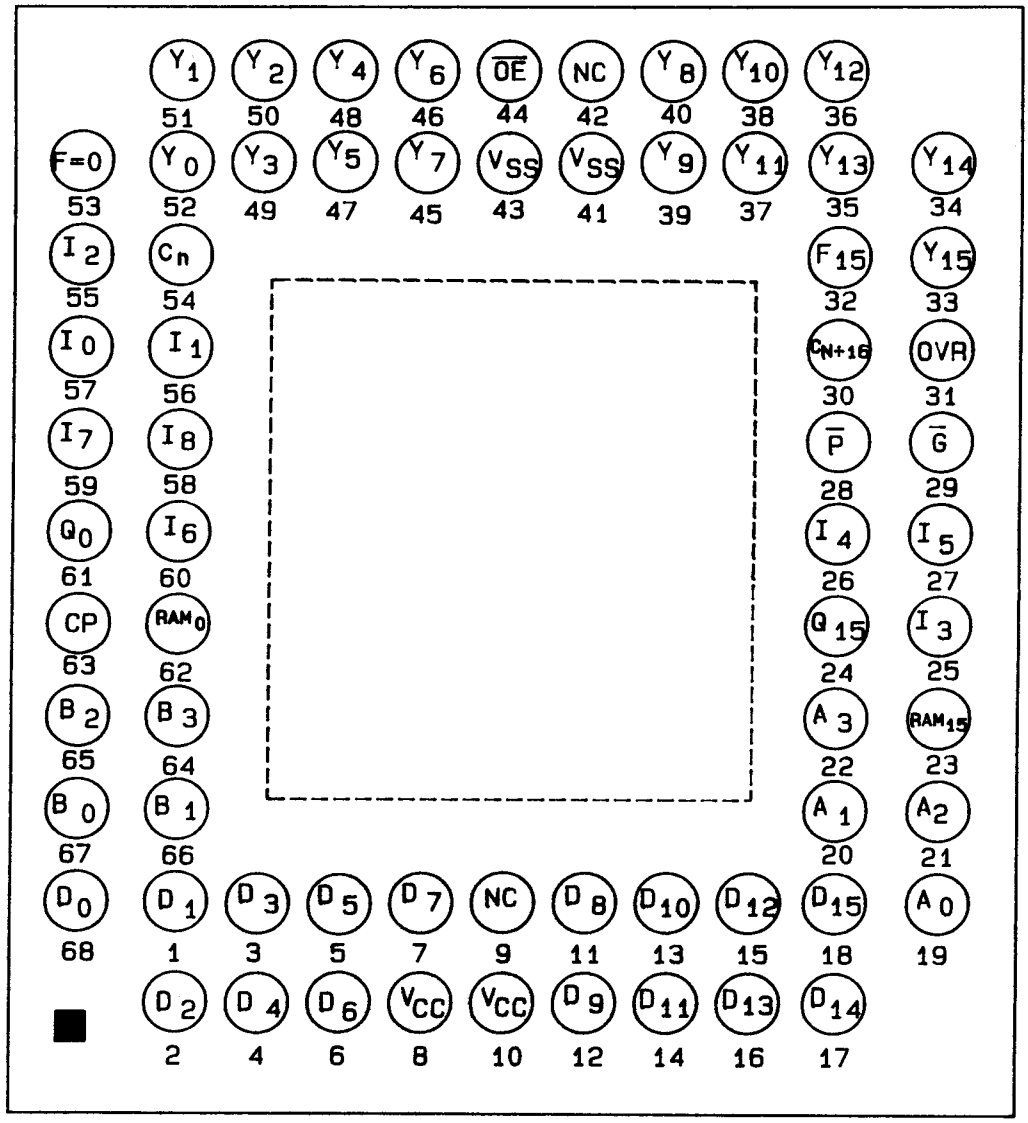


FIGURE 3. Terminal connections - Continued.

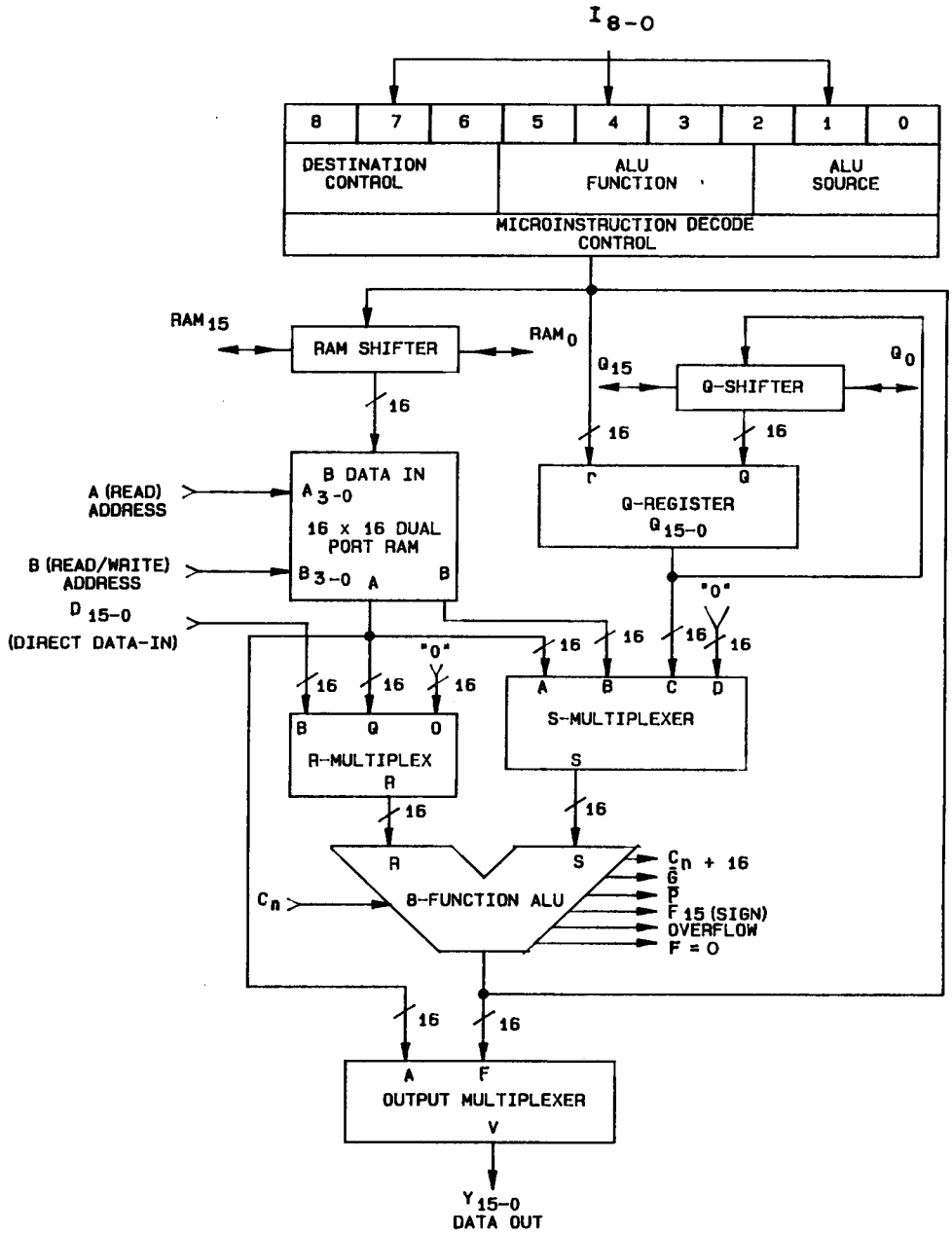
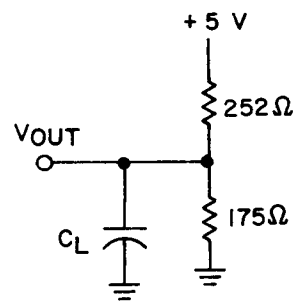


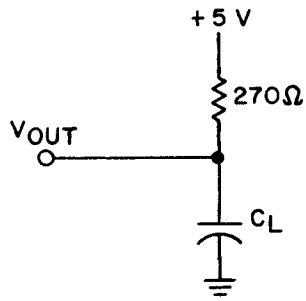
FIGURE 4. Block diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89517
		REVISION LEVEL	SHEET 17

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—550-547



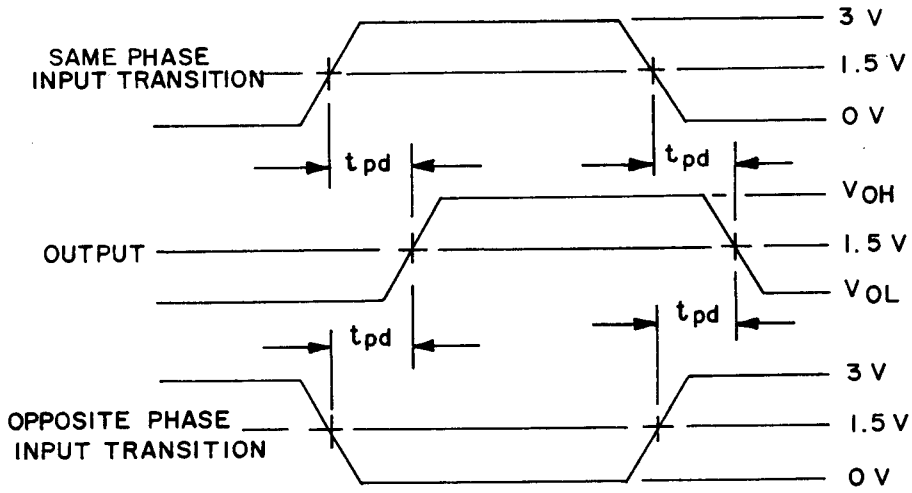
All outputs except open drain



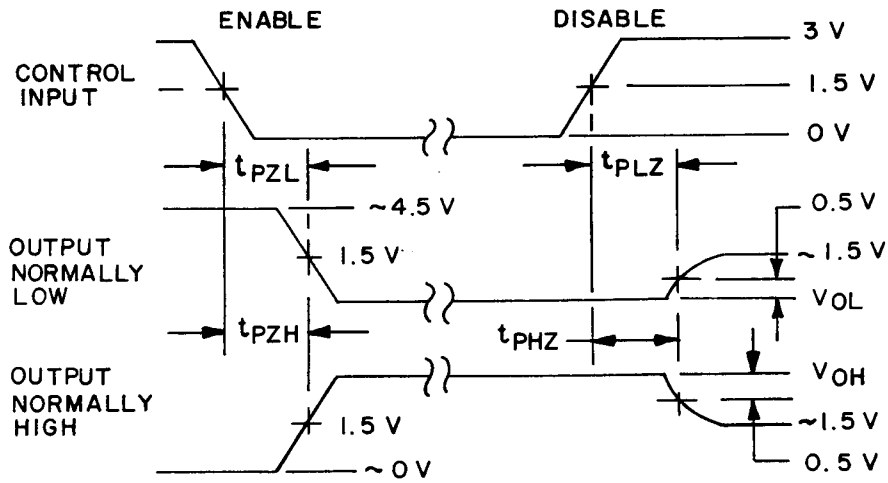
Open drain (F = 0)

NOTES:
1. C_L = 50 pF includes scope probe, wiring, and stray capacitance.
2. C_L = 5 pF for output disable tests.

FIGURE 5. AC loading test circuits and waveforms.



Propagation delay time waveforms.



NOTE: Diagram shown for input enable-low and input control disable-high.

Output enable and disable times waveforms.

FIGURE 5. AC loading test circuits and waveforms - Continued.

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}/C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input/output capacitance. A minimum sample size of five devices with zero rejects shall be required.

d. Subgroups 7 and 8 shall verify the instruction set. The instruction set forms a part of the of the vendor's test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883 conditions:

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8,9
Group A test requirements (method 5005)	1,2,3,4,7,8, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroups 1 and 7.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Pin descriptions.

Mnemonic	Type	Description
A_0 - A_3	I	RAM address A: These 4 address lines select one of the 16 registers in the stack and output its contents on the (internal) A port.
B_0 - B_3	I	RAM address B: These 4 address lines select one of the 16 registers in the stack and output its contents on the (internal) B port. This can also be the destination address when data is written back into the register file.
I_0 - I_8	I	Instruction word: These nine instruction lines select the ALU data sources (I_0, I_1, I_2), the operation to be performed (I_3, I_4, I_5), and what data is to be written back into either the Q register or the register file (I_6, I_7, I_8).
D_0 - D_{15}	I	Direct data input: These are 16 data input lines that may be selected by the I_0, I_1, I_2 lines as inputs to the ALU.
Y_0 - Y_{15}	O	Data output: These are three-state data output lines that, when enabled, output either the output of the ALU or the data in the A latch, as determined by the code on the I_6, I_7, I_8 lines.
$\overline{OE}$	I	Output enable: This is an active low input that controls the Y_0 - Y_{15} outputs. When this signal is low the Y outputs are enabled and when it is high they are in the high impedance state.
CP	I	Clock input: The low level of CP is used to write data to the RAM register file. A high level of CP writes data from the dual port RAM to the A and B latches. The operation of the Q register is similar; data is entered into the master latch on the low level of CP and transferred from master to slave during CP = high.
Q_{15}, RAM_{15}	I/O	These two lines are bidirectional and are controlled by the I_6, I_7, I_8 inputs. They are three-state output drivers connected to the TTL compatible CMOS inputs. Output mode: When the destination code on lines I_6, I_7, I_8 indicates a left shift (UP) operation, the three-state outputs are enabled and the MSB of the Q register is output on the Q_{15} pin and likewise, the MSB of the ALU output (F_{15}) is output on the RAM_{15} pin. Input mode: When the destination code indicates a right shift (down), the pins are the data inputs to the MSB of the Q register and the RAM, respectively.
Q_0, RAM_0	I/O	These two lines are bidirectional and function similar to the Q_{15} and RAM_{15} lines, except that they are the LSB of the Q register and RAM.
C_n	I	Carry in: The carry into the internal ALU.
C_{n+16}	O	Carry out: The carry out of the internal ALU.
$\overline{G}$, $\overline{P}$	O	Carry generate, carry propagate: The carry generate and propagate outputs of the ALU.

Mnemonic	Type	Description
OVR	O	Overflow: This pin indicates when the result of the ALU operation exceeds the capacity of the machines two's complement number range. It is valid only for the sign bit.
F = 0	O	Zero detect: Open drain output that goes high if the data on the ALU outputs (F_0 - F_{15}) are all low.
F_{15}	O	Sign: The most significant bit of the ALU output.

6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8951701XX	65786	CY7C9101-45DMB
5962-8951701YX	65786	CY7C9101-45LMB
5962-8951701ZX	65786	CY7C9101-45GMB
5962-8951701UX	65786	CY7C9101-45FMB
5962-8951702XX	65786	CY7C9101-35DMB
5962-8951702YX	65786	CY7C9101-35LMB
5962-8951702ZX	65786	CY7C9101-35GMB
5962-8951702UX	65786	CY7C9101-35FMB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65786	Cypress Semiconductor Corporation 3901 N. First Street San Jose, CA 95134