



Am81C453

CMOS Color Palette

DISTINCTIVE CHARACTERISTICS

- Plug-In Replacement for Bt453
- Macintosh II Compatible
- Available in 40 and 66 MHz versions
- Available in 44-Pin PLCC Package
- 256 x 4 Color Look-Up Table (LUT)
- Triple 8-bit DACs
- RS343A/RS-170A Compatible RGB Outputs
- 3 x 24 Dual-Port Overlay RAM
- Standard MPU Interface
- +5 V monolithic, high-performance CMOS

GENERAL DESCRIPTION

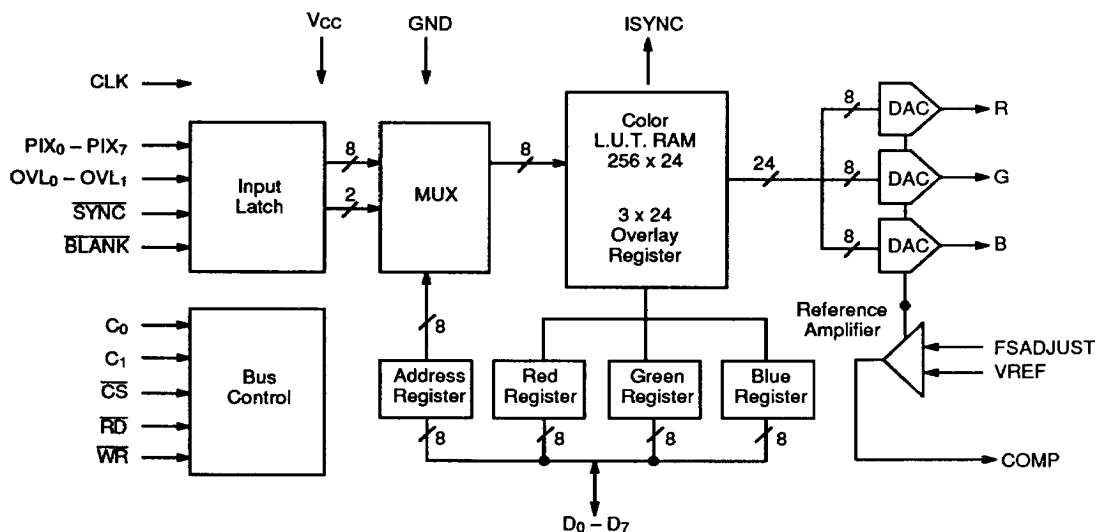
The Am81C453 CMOS Color Palette has been designed specifically for the Macintosh II market. Applications include high resolution color graphics, CAD/CAM/CAE, image processing and desktop publishing. The Am81C453 operates at speeds sufficient to support screen resolutions up to 1024 x 768.

The Am81C453 has an input latch, a 256 x 24 Look-Up Table, a 3 x 24 Overlay Table and triple 8-bit video DACs. It can simultaneously display 259 colors out of an available set of 16.8 million colors. Proprietary DAC decoding techniques minimize glitch energy and skew. It is available in versions with pixel rates as high as 66 MHz.

The Am81C453 generates RS-343A compatible outputs into doubly-terminated 75 Ω loads and RS-170 compatible output into a singly-terminated 75 Ω load, without external buffers. Overlaying cursors, text, grids, etc. can be implemented using the three overlay registers.

The Am81C453 is fabricated using AMD's state-of-the-art 1.2 μ CMOS process. The device is available in a 44-pin PLCC package. The Am81C453 is pin and functionally compatible with the Bt453.

BLOCK DIAGRAM

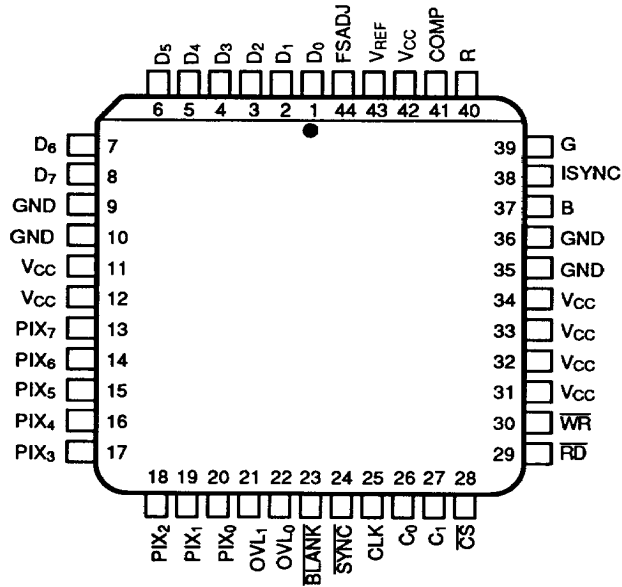


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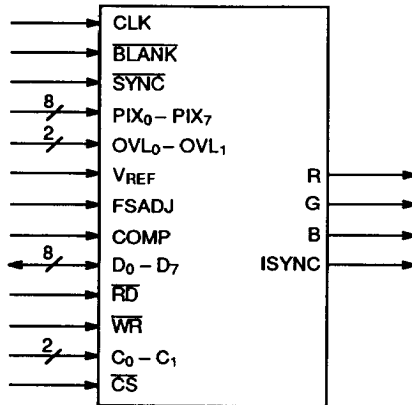
CONNECTION DIAGRAMS

PLCC



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LOGIC SYMBOL



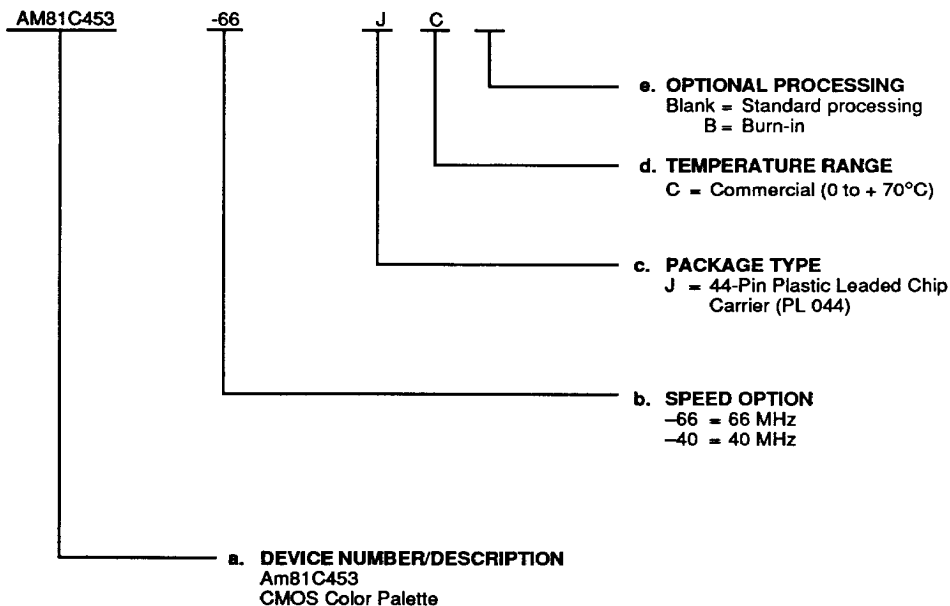
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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (If applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM81C453-66	JC
AM81C453-40	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

Timing Section

CLK

Clock Source Pin (TTL Compatible Input)

This input operates at the pixel clock rate of the system. It is to be driven by a dedicated TTL buffer. The rising edge of CLK latches the SYNC, BLANK, PIX₀–PIX₇ and OVL₀–OVL₁ inputs.

BLANK

Blank (TTL Compatible Input)

The BLANK input, when active, overrides the color pixel and overlay data to force the R, G, and B video outputs to their blank levels. This blank level is required during the monitor's vertical and horizontal retrace times. It is latched on the rising edge of CLK.

SYNC

SYNC (TTL Compatible Input)

The SYNC input, when active, switches off a 40 IRE current source on the ISYNC output. It is latched on the rising edge of CLK. Because SYNC does not override any other input or control pin, it should be asserted only during blanking intervals.

Bit Map Interface Section

PIX₀–PIX₇

Color Pixel Data Addresses (TTL Compatible Inputs)

These eight inputs select which of the 256 entries in the Color Look-Up Table is to be used to provide pixel color information. They are loaded into the input latch on the rising edge of CLK. PIX₀ is the least significant bit. Unused inputs should be grounded.

OVL₀–OVL₁

Overlay Data Address (TTL Compatible inputs)

These two inputs select which of the 3 Overlay Registers is to be used to provide color information, as illustrated in Table 5. They are loaded into the input latch on the rising edge of CLK. The PIX₀–PIX₇ inputs are ignored when the overlay palette is accessed. OVL₀ is the least significant bit. Unused inputs should be grounded.

MPU Interface Section

D₀–D₇

Data and Address Bus (TTL Compatible Bi-Directional)

These eight pins are used to load and read back the Color Look-Up Table and the internal control registers. D₀ is the least significant bit.

$\overline{RD}$

Read Control Input (TTL Compatible Input)

$\overline{RD}$ and $\overline{CS}$ must be a logical zero to read data from the Color Look-Up Table or any of the internal control registers. During Read operations, C₀–C₁ are latched on the falling edge of $\overline{RD}$.

$\overline{WR}$

Write Control Input (TTL Compatible Input)

$\overline{WR}$ and $\overline{CS}$ must be a logical zero to write data to the Color Look-Up Table or any of the internal control registers. During Write operations, C₀–C₁ are latched on the falling edge of $\overline{WR}$.

$\overline{CS}$

Chip Select (TTL-Compatible Input)

This signal enables the MPU interface. Data on D₀–D₇ is internally latched on the rising edge of $\overline{CS}$ during Write operations. R, G, and B outputs are forced to their Blank level when $\overline{CS}$ is a logical zero.

C₀–C₁

Address Control Inputs (TTL Compatible Inputs)

C₀–C₁ allow the MPU to address any location in the Color Look-Up Table or any of the internal control registers. These inputs determine the type of read or write operation to be performed.

Analog Output Section

R

Red Video Output (Analog Output)

Analog output of the red DAC. This output is capable of driving an RS-343A compatible doubly-terminated 75 Ω cable and an RS-170 compatible singly-terminated 75 Ω cable.

G

Green Video Output (Analog Output)

Analog output of the green DAC. This output is capable of driving an RS-343A compatible doubly-terminated 75 Ω cable and an RS-170 compatible singly-terminated 75 Ω cable.

B

Blue Video Output (Analog Output)

Analog output of the blue DAC. This output is capable of driving an RS-343A compatible doubly-terminated 75 Ω cable and an RS-170 compatible singly-terminated 75 Ω cable.

COMP

Compensation Capacitor Connection (Analog Input)

A 0.1 μF ceramic capacitor is connected between this pin and V_{CC}.

V_{REF}

Voltage Reference (Analog Input)

An external voltage reference circuit such as the one shown in Figure 1 must supply this input with a 1.235 V (typical) reference.

ISYNC

SYNC Current (Analog Output)

This high impedance sync current signal is used to encode sync information on the G output. When SYNC is a logical zero, ISYNC current is 0. When the sync information is not necessary on the G output, the ISYNC output should be grounded. The magnitude of this ISYNC current output during the active period of SYNC is defined by:

$$\text{ISYNC (mA)} = 1728 * V_{\text{REF}} (\text{V}) / R_{\text{SET}} (\Omega).$$

FSADJ

Full Scale Adjust (Analog Input)

Voltage Mode:

The magnitude of the full-scale video signal is controlled by a resistor (R_{SET}) connected between FSADJ and

GND. The relationship between the resistor and the full-scale output current is:

$$R_{\text{SET}} (\Omega) = 6047 * V_{\text{REF}} (\text{V}) / G (\text{mA}); \text{ with ISYNC connected to G.}$$

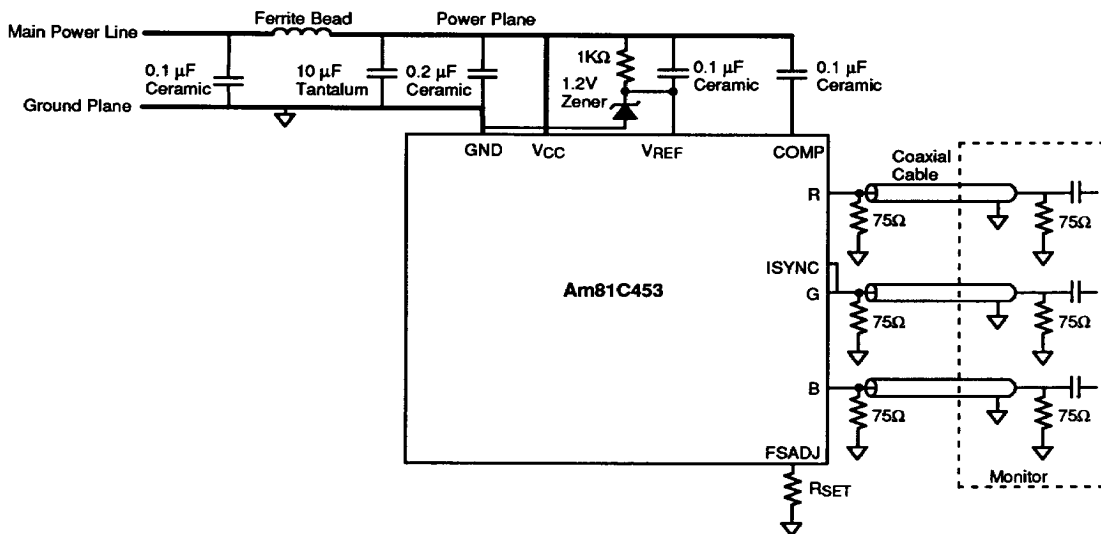
Power Supply Section

V_{CC}

+5 Volt Supply

GND

Ground



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Figure 1. Am81C453 Typical Circuit Connection

FUNCTIONAL DESCRIPTION

The Am81C453 CMOS Color Palette integrates all major functions required in the backend of a video system and supports pixel rates sufficient to drive most low-to-medium resolution monitors.

A programmable Look-Up Table maps the pixel data from a frame buffer into physical color and three Digital-to-Analog-Converters (DACs) convert the digital outputs of the Look-Up Table into RS-343A or RS-170 compatible RGB analog outputs.

Microprocessor Interface

The Am81C453 is designed to support a standard microprocessor bus interface with direct access to 256 Look-Up Table (LUT) RAM locations and 3 overlay registers. The microprocessor interface is asynchronous with respect to pixel clock. However, data transfers between the LUT RAM or overlay registers and the Red, Green and Blue DACs as shown in the block diagram are synchronized to pixel clock.

The nature of the microprocessor operation is determined by examining the $C_0 - C_1$ inputs. The $C_0 - C_1$ inputs select the MPU access type as detailed in Table 1.

Table 1. C_1, C_0 Decoding

C_1	C_0	Access Type
0	0	Address Register
0	1	Look-Up Table
1	0	Address Register
1	1	Overlay Registers

First Access to the Look-Up Table and to the Overlay Registers is achieved by means of two internal counters: an 8-bit Address Register ($AR_0 - AR_7$), which generates addresses for the Color Memory locations and the Overlay Registers, and a Modulo 3 Counter

(AR_a, AR_b) that controls which byte of the 24-bit Color Memory Word is accessed. Tables 2 and 3 illustrate the operation of these two counters.

Table 2. Address Register Operation

$AR_7 - AR_0$	C_1	C_0	Location/Register addressed by MPU
\$00-\$FF	0	1	Color Look-Up Table
\$00	1	1	Reserved
\$01	1	1	Overlay Register 1
\$02	1	1	Overlay Register 2
\$03	1	1	Overlay Register 3

Table 3. Modulo 3 Counter Operation

AR_b	AR_a	Color Byte Being Accessed
0	0	Red
0	1	Green
1	0	Blue

The Address Register, directly accessible by the MPU, auto-increments at the end of each third (Blue) access having $C_0 = 1$. This feature avoids the rewriting of the Address Register with consecutive values, saving MPU time and Bus bandwidth for transfers to or from consecutive Color Memory locations.

The Modulo 3 Counter, not accessible by the MPU, increments at the end of each MPU access with $C_0 = 1$ (color operations), and is reset to 0 at the end of each MPU access with $C_0 = 0$ (Control Register operations).

Table 4 illustrates the Read/Write access to the Am81C453 Palette.

Table 4. Read/Write Access to the Am81C453

RD	WR	C ₁	C ₀	ARb	ARa	Function
1	0	0	0	x	x	Write Address Register (LUT Write); AR(7:0) ← D(7:0); ARb, ARa ← 0.
1	0	0	1	0	0	Write Red Color; RREG(7:0) ← D(7:0); INC. ARb, ARa.
1	0	0	1	0	1	Write Green Color; GREG(7:0) ← D(7:0); INC. ARb, ARa.
1	0	0	1	1	0	Write Blue Color; BREG(7:0) ← D(7:0); ARb, ARa ← 0. Write Color Look-Up Table; R(7:0) ← RREG; G(7:0) ← GREG; B(7:0) ← BREG; INC. AR(7:0).
1	0	1	0	x	x	Write Address Register (Overlay Write); AR(7:0) ← D(7:0); ARb, ARa ← 0.
1	0	1	1	0	0	Write Red Color; RREG(7:0) ← D(7:0); INC. ARb, ARa.
1	0	1	1	0	1	Write Green Color; GREG(7:0) ← D(7:0); INC. ARb, ARa.
1	0	1	1	1	0	Write Blue Color; BREG(7:0) ← D(7:0); ARb, ARa ← 0. Write Overlay Register; R(7:0) ← RREG; G(7:0) ← GREG; B(7:0) ← BREG; INC. AR(7:0).
0	1	0	0	x	x	Read Address Register (LUT Read); D(7:0) ← AR(7:0); ARb, ARa ← 0.
0	1	0	1	0	0	Read Color LUT Red; D(7:0) ← RREG(7:0); INC. ARb, ARa.
0	1	0	1	0	1	Read Color LUT Green; D(7:0) ← GREG(7:0); INC. ARb, ARa.
0	1	0	1	1	0	Read Color LUT Blue; D(7:0) ← BREG(7:0); ARb, ARa ← 0. INC. AR(7:0).
0	1	1	0	x	x	Read Address Register (Overlay Read); D(7:0) ← AR(7:0); ARb, ARa ← 0.
0	1	1	1	0	0	Read Overlay Red; D(7:0) ← RREG(7:0); INC. ARb, ARa.
0	1	1	1	0	1	Read Overlay Green; D(7:0) ← GREG(7:0); INC. ARb, ARa.
0	1	1	1	1	0	Read Overlay Blue; D(7:0) ← BREG(7:0); ARb, ARa ← 0. INC. AR(7:0).

Display Memory Interface

When CS is a logical one, the pixel inputs, PIX₀ – PIX₇ and OVL₀ – OVL₁ are latched on the rising edge of CLK and are used as address to the 256 locations of the LUT RAM and the 3 Overlay Registers, respectively, as shown in Table 5.

The total pipeline delay from the digital inputs PIX₀ – PIX₇, OVL₀ – OVL₁, SYNC, and BLANK to the analog R, G, and B outputs is four clock cycles.

Table 5. Color LUT and Overlay Selection

OVL ₁	OVL ₀	PIX ₀ – PIX ₇	Addressed by Display Memory
0	0	\$00	Color Palette RAM location \$00
0	0	\$01	Color Palette RAM location \$01
0	0	\$FF	Color Palette RAM location \$FF
0	1	\$xx	Overlay Register 1
1	0	\$xx	Overlay Register 2
1	1	\$xx	Overlay Register 3

Video Generation

During each clock cycle, a 24-bit word from either the LUT RAM or the Overlay Registers is presented to the three DACs. The three DACs convert the digital color memory output into RGB RS-343A analog format.

The $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs are latched on the rising edge of CLK. These two inputs are responsible for adding weighted currents to RGB analog outputs as shown in Figure 2.

Table 6 shows how the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs change analog output levels.

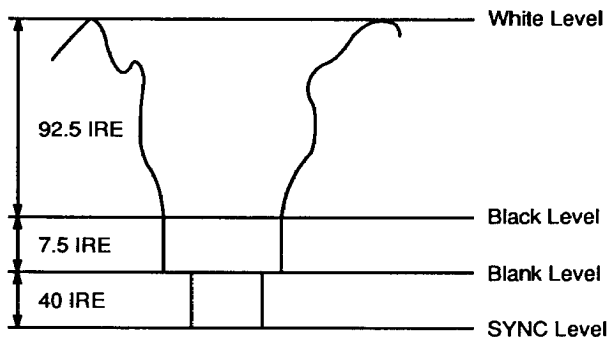
The $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs are routed to the DACs after a delay equal to four clock periods, identical to the delay incurred by the video stream to produce the relative Blank and Sync levels. $\overline{\text{BLANK}}$ is routed to all three DACs while $\overline{\text{SYNC}}$ is routed only to the Green DAC.

Table 6. Video Output Truth Table

Description	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	I _{OUT} (G) (mA)	I _{OUT} (R,B) (mA)	DAC Input Data
White	1	1	26.67	19.05	\$FF
Data	1	1	data + 9.05	data + 1.44	data
Data-SYNC	0	1	data + 1.44	data + 1.44	data
Black	1	1	9.05	1.44	\$00
Black-SYNC	0	1	1.44	1.44	\$00
Blank	1	0	7.62	0	\$xx
SYNC	0	0	0	0	\$xx

Note: Typical with full scale I_{OUT} (G) = 26.67 mA. R_{SET} = 280 Ω, V_{REF} = 1.235 V. ISYNC connected to G.

Red, Blue		Green	
V	mA	V	mA
0.714	19.05	1.000	26.67
0.054	1.44	0.340	9.05
0.000	0.00	0.286	7.62
		0.000	0.00



11916-005B

Figure 2. Composite Video Output Signals

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65 to +150°C
Ambient Temperature Under Bias	0 to +70°C
Supply Voltage to Ground	
Potential Continuous	−0.5 to 7.0 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 to V_{CC} +0.5 V
DC Input Voltage	−0.5 to V_{CC} +0.5 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES**Commercial (C) Devices**

Ambient Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.75 to +5.25 V
Reference Voltage	+1.14 to +1.26 V
Output Load	37.5 Ω
FSADJ Resistor (R_{SET})	280 Ω

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range with ISYNC connected to G

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
Digital Inputs						
V _{IH}	Input High Voltage		2.0		V _{CC} +0.5	V
V _{IL}	Input Low Voltage		GND-0.5		0.8	V
I _{IH}	Input High Current	V _{IN} = 2.4 V			1	μA
I _{IL}	Input Low Current	V _{IN} = 0.4 V			-1	μA
C _{IN}	Input Capacitance	f = 1 MHz, V _{IN} = 2.4 V		10		pF
Digital Outputs						
V _{OH}	Output High Voltage	I _{OH} = -0.4 mA	2.4			V
V _{OL}	Output Low Voltage	I _{OL} = +3.2 mA			.4	V
I _{oz}	Three-State Current	GND ≤ V _{IN} ≤ V _{CC}			10	μA
C _{OUT}	Output Capacitance			20		pF
Analog Outputs						
LIN _i	Resolution (each DAC)		8	8	8	Bits
	Integral Linearity Error				± 1	LSB
LIN _d	Differential Linearity Error				± 1	LSB
	Gray Scale Error				± 5	%Gray
	Monotonicity			Guaranteed		
	Coding	Binary				Binary
	Output Compliance		-1.0		1.2	V
	Gray Scale Current Range		15		22	mA
	DAC-to-DAC Matching			2	5	%
	Glitch Energy		50		50	pV-sec
	Output Current					
	White Level Relative to Blank		17.69	19.05	20.40	mA
	White Level Relative to Black		16.74	17.62	18.50	mA
	Black Level Relative to Blank		0.95	1.44	1.90	mA
	Blank Level on R, B		0	5	50	μA
	Blank Level on G		6.29	7.62	8.96	mA
	Sync Level on G		0	5	50	μA
	LSB Size			69.1		μA
I _{VREF}	Voltage Reference Input Current			10		μA
	Output Impedance			10		k Ω
	Output Capacitance	(Note 1)		20		pF
PSRR	Power Supply Rejection Ratio	(Note 2)		0.12	0.5	%/% ΔVAA

Notes:

1. f = 1 MHz, I_{OUT} = 0 mA
2. COMP = 0.1 μF, f = 1 kHz

SWITCHING CHARACTERISTICS

Parameter Number	Parameter Description	Min./Typ. Max.			Unit
	Clock Rate	Max.	66	40	MHz
1	$\overline{CS}$, C_0 - C_1 Setup Time	Min.	35	35	ns
2	$\overline{CS}$, C_0 - C_1 Hold Time	Min.	35	35	ns
3	$\overline{RD}$, $\overline{WR}$ High Time	Min.	25	25	ns
4	$\overline{RD}$ Asserted to Data Bus Driven	Min.	10	10	ns
5	$\overline{RD}$ Asserted to Data Valid	Max.	100	100	ns
6	$\overline{RD}$ Negated to Data Bus 3-stated	Max.	15	15	ns
7	$\overline{WR}$ Pulse Width Low	Min.	50	50	ns
8	Write Data Setup Time	Min.	35	35	ns
9	Write Data Hold Time	Min.	5	5	ns
10	Pixel/Control Setup Time	Min.	5	7	ns
11	Pixel/Control Hold Time	Min.	2	3	ns
12	Clock Cycle Time	Min.	15	25	ns
13	Clock Pulse Width High Time	Min.	5	7	ns
14	Clock Pulse Width Low Time	Min.	5	7	ns
15	Analog Output Delay	Max.	30	30	ns
		Typ.	20	20	ns
16	Analog Output Rise/Fall Time (Note 1)	Max.			ns
		Typ.	3	3	ns
17	Analog Output Settling Time (Note 1)	Max.			ns
		Typ.	25	25	ns
	Analog Output Skew	Max.	2	2	ns
		Typ.	1	1	ns
18	Pipeline Delay	Typ.	2	2	clocks
	V_{CC} Supply Current (Note 2)	Typ.	175	150	mA
	V_{CC} Supply Current (Note 2)	Max.	220	200	mA
	DAC to DAC Crosstalk	Typ.	-23	-23	dB
	Clock and Data Feedthrough	Typ.	-30	-30	dB

Notes:

- Clock and data feedthrough are not included
- Measured at maximum f_{CLK} ;
 $I_{CC}(\text{Max.}): V_{CC} = 5.25 \text{ V}, T_A = 0^\circ\text{C}$,
 $I_{CC}(\text{Typ.}): V_{CC} = 5.0 \text{ V}, T_A = +25^\circ\text{C}$

Test Conditions;

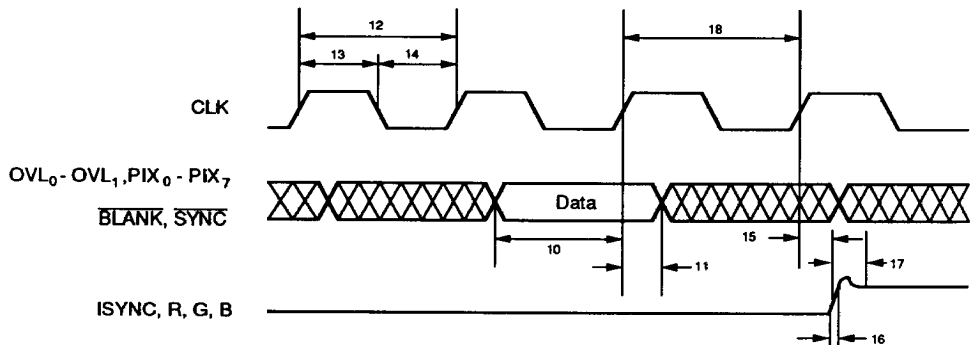
TTL Input Level: 0 to 3 V with t_R, t_F (10–90%) $\leq 3 \text{ ns}$
 Analog Output Load $\leq 10 \text{ pF}$; D_0 - D_7 Output Load $\leq 50 \text{ pF}$

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

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SWITCHING TEST WAVEFORMS



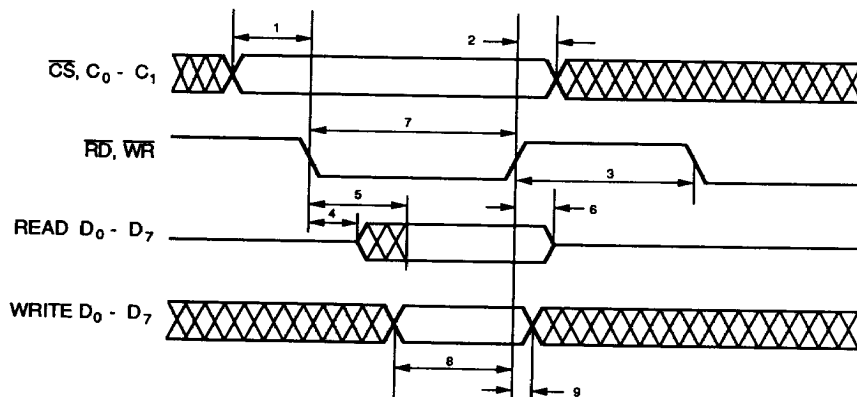
Note 1: Output delay measured from the 50% point of the rising edge of CLK to the 50% point of the full scale transition.

Note 2: Settling time measured from the 50% point of the full scale transition to the output remaining within ± 1 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Video Input/Output Timing

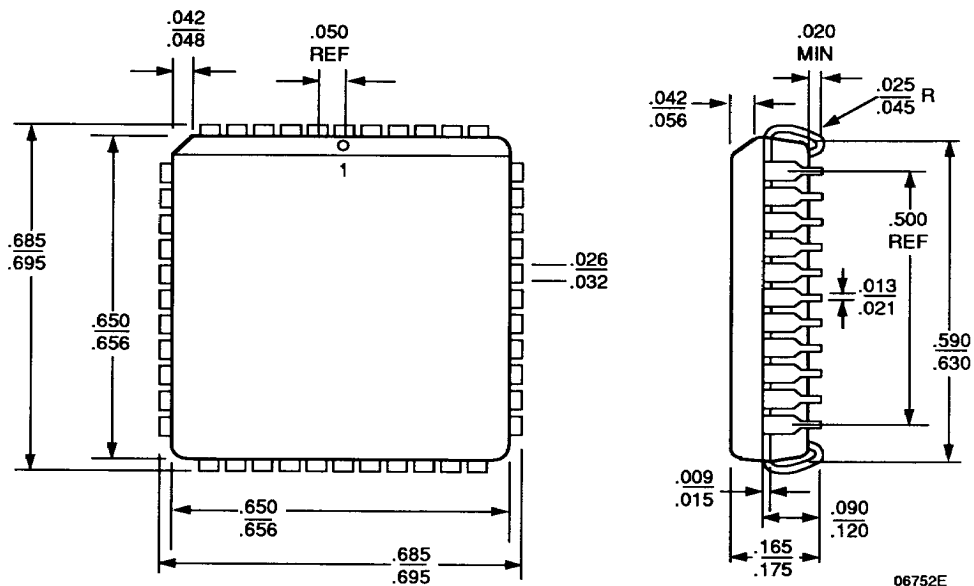
11916-006B



MPU Read/Write Timing

11916-007B

PHYSICAL DIMENSIONS **PL 044**



North American

ALABAMA	(205) 882-9122
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Newport Beach	(714) 752-6262
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San Jose	(408) 452-0500
Woodland Hills	(818) 992-4155
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NEW YORK	
Liverpool	(315) 457-5400
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OREGON	(503) 245-0080
PENNSYLVANIA	(215) 398-8006
SOUTH CAROLINA	(803) 772-6760
TEXAS	
Austin	(512) 346-7830
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International

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	FAX (02) 762-37-12
	TLX 846-61028
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	FAX (1) 49-75-10-13
	TLX 263282F
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	FAX (0511) 721254
	TLX 922850
München	TEL (089) 4114-0
	FAX (089) 406490
	TLX 523883
Stuttgart	TEL (0711) 62 33-77
	FAX (0711) 625187
	TLX 721882
HONG KONG, Wanchai	TEL 852-5-8654525
	FAX 852-5-8654335
	TLX 67955AMDAPHX
ITALY, Milan	TEL (02) 3390541
	FAX (02) 3533241
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	FAX 462-47-1729
Tokyo	TEL (03) 346-7550
	FAX (03) 342-5196
	TLX J24064AMDTKOJ
Osaka	TEL 06-243-3250
	FAX 06-243-3253

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KOREA, Seoul	TEL 822-784-0030
	FAX 822-784-8014
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	FAX (305) 485-9736
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