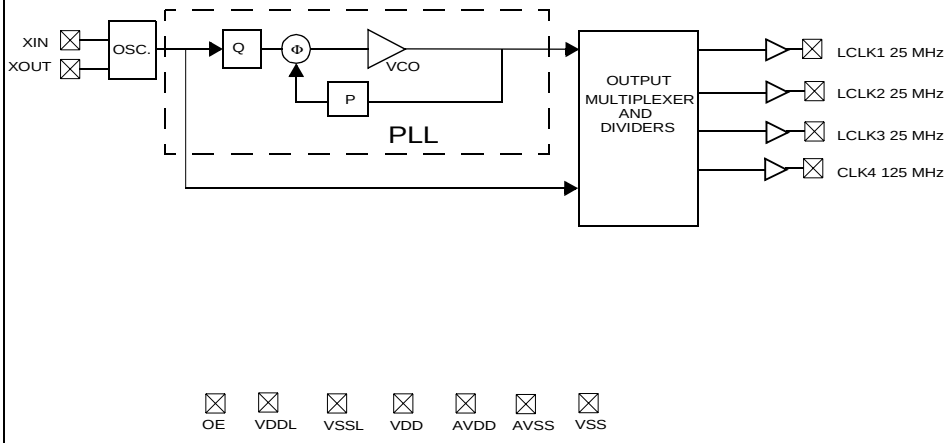
CY26111

One-PLL General Purpose Clock Generator

Features	Benefits
• **Integrated phase-locked loop**	Internal PLL with up to 333 MHz internal operation
• **Low skew, low jitter, high-accuracy outputs**	Meets critical timing requirements in complex system designs
• **3.3V Operation with 2.5V Output Option**	Enables application compatibility
• **16-TSSOP**	Industry standard package saves on board space

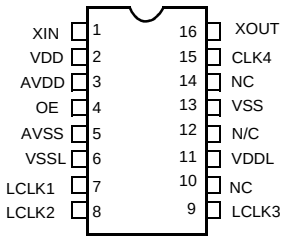
Part Number	Outputs	Input Frequency	Output Frequency Range
CY26111	4	25 MHz	3 x 25 MHz, 1 x 125 MHz

Logic Block Diagram



Pin Configurations

CY26111
16-pin TSSOP



Output	Pin	Default Frequency	Unit
LCLK1	7	25	MHz
LCLK2	8	25	MHz
LCLK3	9	25	MHz
CLK4	15	125	MHz

Summary

Name	Pin Number	Description
XIN	1	Reference Input
VDD	2	Voltage Supply
AVDD	3	Analog Voltage Supply
OE	4	Output Enable, OE = 0 three-state; OE = 1 active
AVSS	5	Analog Ground
VSSL	6	LCLK Ground
LCLK 1	7	Clock output 1–25 MHz at V_{DDL} level
LCLK 2	8	Clock output 2–25 MHz at V_{DDL} level
LCLK 3	9	Clock output 3–25 MHz at V_{DDL} level
NC	10	No Connect - Reserved
VDDL	11	LCLK Voltage Supply (2.5V or 3.3V)
NC	12	No Connect - Reserved
VSS	13	Ground
NC	14	No Connect - Reserved
CLK 4	15	Clock output 4 - 125 MHz
XOUT[1]	16	Reference Output

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	–0.5	7.0	V
V_{DDL}	I/O Supply Voltage		7.0	V
T_J	Junction Temperature		125	°C
	Digital Inputs	AV_{SS} – 0.3V	AV_{DD} + 0.3V	V
	Digital Outputs referred to V_{DD}	V_{SS} – 0.3V	V_{DD} + 0.3V	V
	Digital Outputs referred to V_{DDL}	V_{SS} – 0.3V	V_{DDL} +0.3V	V
	Electro-Static Discharge	2		kV

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	3.0	3.3	3.6	V
V_{DDL}	Operating Voltage	2.375	2.5	2.625	V
T_A	Ambient Temperature	0		70	°C
C_{LOAD}	Max. Load Capacitance			15	pF
f_{REF}	Driven Reference Frequency		25		MHz

Note:
1. Float XOUT if XIN is externally driven.

DC Electrical Characteristics

Parameter[1]	Name	Description	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5$, $V_{DD}/V_{DDL} = 3.3V$	12	24		mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD}/V_{DDL} = 3.3V$	12	24		mA
I_{OH}	Output High Current	$V_{OH} = V_{DDL} – 0.5$, $V_{DDL} = 2.5V$	8	16		mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DDL} = 2.5V$	8	16		mA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7			V_{DD}
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}			0.3	V_{DD}
C_{IN}	Input Capacitance	OE Pin			7	pF
I_{IZ}	Input Leakage Current	OE Pin		5		µA
I_{VDD}	Supply Current	AV_{DD}/V_{DD} Current			30	mA
I_{VDDL}	Supply Current	V_{DDL} Current (V_{DDL}=3.6V)			10	mA
I_{VDDL}	Supply Current	V_{DDL} Current (V_{DDL} = 2.625V)			8	mA

AC Electrical Characteristics

Parameter[1]	Name	Description	Min.	Typ.	Max.	Unit
DC		Duty Cycle is defined in Figure 1; t1/t2, 50% of V_{DD}	40	50	60	%
t_3	Rising Edge Slew Rate	Output Clock Rise Time, 20% – 80% of V_{DD}/V_{DDL} = 3.3V	0.8	1.4		V/ns
t_3	Rising Edge Slew Rate	Output Clock Rise Time, 20% – 80% of V_{DDL} = 2.5V	0.6	1.2		V/ns
t_4	Falling Edge Slew Rate	Output Clock Fall Time, 80% – 20% of V_{DD}/V_{DDL} = 3.3V	0.8	1.4		V/ns
t_4	Falling Edge Slew Rate	Output Clock Fall Time, 80% – 20% of V_{DDL} = 2.5V	0.6	1.2		V/ns
t5	Skew	Delay between related outputs at rising edge			200	ps
t9	Clock Jitter	Peak to Peak period jitter			250	ps
t10	PLL Lock Time				3	ms

Note:
2. Not 100% tested.

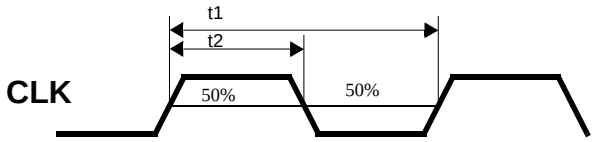


Figure 1. Duty Cycle Definition; DC = t2/t1.

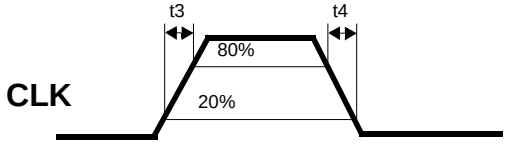
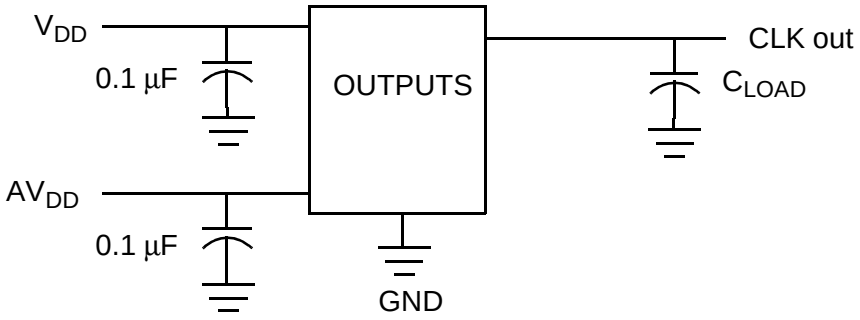


Figure 2. Rise and Fall Time Definitions.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY26111ZC	Z16	16-Pin TSSOP	Commercial	3.3V

Test Circuit



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