

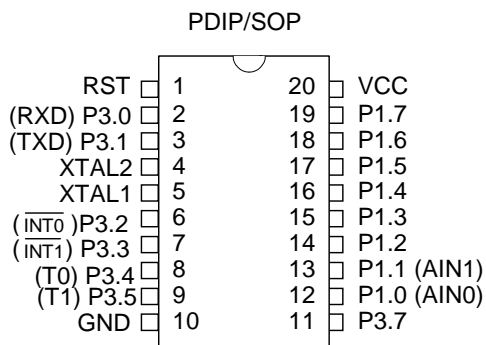
Features

- Compatible with MCS-51™ Products
- 2 Kbytes of programmable EPROM
- 4.25V to 5.5V Operating Range (GMS97C2051)
2.70V to 3.6V Operating Range (GMS97L2051)
- Version for 12MHz / 24 MHz Operating frequency (GMS97C2051)
Only 12MHz Operating frequency (GMS97L2051)
- Two-Level Program Memory Lock with encryption array
- 128 bytes SRAM
- 15 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Programmable serial USART
- Five Interrupt Sources
- Direct LED Drive Outputs
- On-Chip Analog Comparator
- Low Power Idle and Power Down Modes

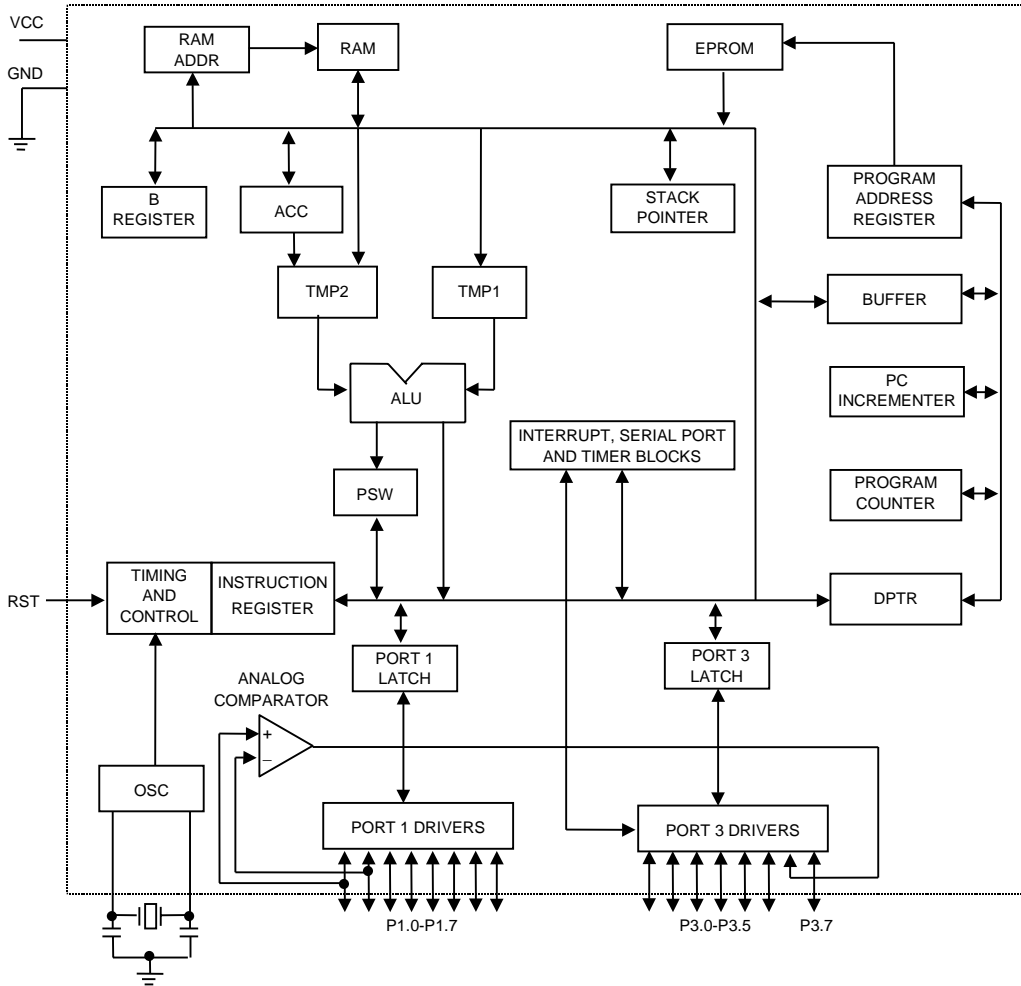
Description

The GMS97C2051/L2051 is a high-performance CMOS 8-bit microcontroller with 2Kbytes of programmable EPROM. The device is compatible with the industry standard MCS-51™ instruction set and pinout. The HYUNDAI MicroElectronics GMS97C2051/L2051 is a powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. The GMS97C2051/L2051 provides the following standard features: 2Kbytes of EPROM, 128 bytes of RAM, 15 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, a precision analog comparator, on-chip oscillator and clock circuitry. In addition, the GMS97C2051/L2051 supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

Pin Configuration



Block Diagram



Pin Description

Vcc
Supply voltage.

GND
Ground.

Port 1
Port 1 is an 8-bit bidirectional I/O port. Port pins P1.2 to P1.7 provide internal pullups. P1.0 and P1.1 require external pullups. P1.0 and P1.1 also serve as the positive input (AIN0) and the negative input (AIN1), respectively, of the on-chip precision analog comparator. The Port 1 output buffers can sink 10mA and can drive LED displays directly. When 1s are written to Port1 pins, they can be used as inputs. When pins P1.2 to P1.7 are used as inputs and are externally pulled low, they will source current (I_{IL}) because of the internal pullups.
Port 1 also receives code data during EPROM programming and program verification.

Port3
Port 3 pins P3.0 to P3.5, P3.7 are seven bidirectional I/O pins with internal pullups. P3.6 is hard-wired as an input to the output of the on-chip comparator and is not accessible as a general purpose I/O pin. The Port 3 output buffers can sink 10mA. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.
Port 3 also serves the functions of various special feature of the GMS97C2051 as listed below:

| Port Pin | Alternate Functions |
|----------|---|
| P3.0 | RXD (serial input port) |
| P3.1 | TXD (serial output port) |
| P3.2 | $\overline{\text{INT0}}$ (external interrupt 0) |
| P3.3 | $\overline{\text{INT1}}$ (external interrupt 1) |
| P3.4 | T0 (timer 0 external input) |
| P3.5 | T1 (timer 0 external input) |

Port 3 also receives some control signals for EPROM programming and programming verification.

RST
Reset input. All I/O pins are reset to 1s as soon as RST goes high. Holding the RST pin high for two machine cycles while the oscillator is running resets the device.

This pin is also receives the 12.75V programming supply voltage (V_{pp}) during EPROM programming.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

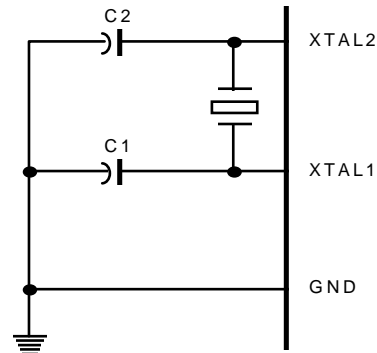
XTAL2

Output from the inverting oscillator amplifier.

Recommended Oscillator Circuit

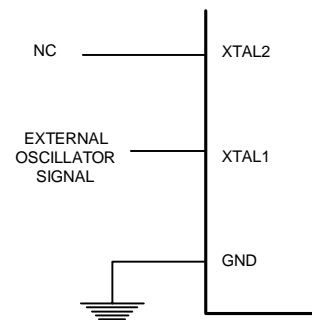
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in **Figure 1**. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in **Figure 2**.

Figure 1. Oscillator Connections



Notes: C1, C2 = 30pF± 10pF for Crystals
(include stray capacitance)

Figure 2. External Clock Drive Configuration



Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in the **Table 1**, **Table 2** and **Table 3**.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

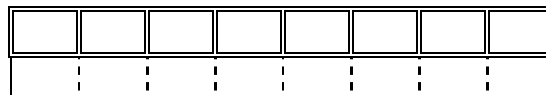
Table 1. GMS97C2051/L2051 SFR Map and Reset Values

| | | | | | | | | |
|------|------------------|------------------|-----------------|-----------------|-----------------|-----------------|------------------|------|
| 0F8H | | | | | | | | 0FFH |
| 0F0H | B 00000000 | | | | | | | 0F7H |
| 0E8H | | | | | | | | 0EFH |
| 0E0H | ACC 00000000 | | | | | | | 0E7H |
| 0D8H | | | | | | | | 0DFH |
| 0D0H | PSW 00000000 | | | | | | | 0D7H |
| 0C8H | | | | | | | | 0CFH |
| 0C0H | | | | | | | | 0C7H |
| 0B8H | IP XXX00000 | | | | | | | 0BFH |
| 0B0H | P3 11111111 | | | | | | | 0B7H |
| 0A8H | IE 0XX00000 | | | | | | | 0AFH |
| 0A0H | | | | | | | | 0A7H |
| 98H | SCON 00000000 | SBUF XXXXXXXX | | | | | | 9FH |
| 90H | P1 11111111 | | | | | | | 97H |
| 88H | TCON 00000000 | TMOD 00000000 | TL0 00000000 | TL1 00000000 | TH0 00000000 | TH1 00000000 | | 8FH |
| 80H | | SP 00001111 | DPL 00000000 | DPH 00000000 | | | PCON 0XXX0000 | 87H |

Table 2. Bit Assignment of SFRs

| Address | Register | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-----------------|----------|------|---------------|------|------|------|---------------|------|------|
| 81 _H | SP | | | | | | | | |
| 82 _H | DPL | | | | | | | | |
| 83 _H | DPH | | | | | | | | |
| 87 _H | PCON | SMOD | - | - | - | GF1 | GF0 | PD | IDLE |
| 88 _H | TCON | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 |
| 89 _H | TMOD | GATE | C / \bar{T} | M1 | M0 | GATE | C / \bar{T} | M1 | M0 |
| 8A _H | TL0 | | | | | | | | |
| 8B _H | TL1 | | | | | | | | |
| 8C _H | TH0 | | | | | | | | |
| 8D _H | TH1 | | | | | | | | |
| 90 _H | P1 | | | | | | | | |
| 98 _H | SCON | SM0 | SM1 | SM2 | REN | TB8 | RB8 | TI | RI |
| 99 _H | SBUF | | | | | | | | |
| A8 _H | IE | EA | - | - | ES | ET1 | EX1 | ET0 | EX0 |
| B0 _H | P3 | | | | | | | | |
| B8 _H | IP | - | - | - | PS | PT1 | PX1 | PT0 | PX0 |
| D0 _H | PSW | CY | AC | F0 | RS1 | RS0 | OV | F1 | P |
| E0 _H | ACC | | | | | | | | |
| F0 _H | B | | | | | | | | |

- : This Bit Location is reserved



Bit manipulation is available

Bit manipulation is not available

Table 3. SFR lists and their addresses

| Symbol | Name | Address |
|--------|----------------------------|-----------------|
| * ACC | Accumulator | E0 _H |
| * B | B Register | F0 _H |
| DPH | Data Pointer High Byte | 83 _H |
| DPL | Data Pointer Low Byte | 82 _H |
| * PSW | Program Status Word | D0 _H |
| SP | Stack Pointer | 81 _H |
| * IE | Interrupt Enable Control | A8 _H |
| * IP | Interrupt Priority Control | B8 _H |
| * P1 | Port 1 | 90 _H |
| * P3 | Port 3 | B0 _H |
| * SCON | Serial Control | 98 _H |
| SBUF | Serial Data Buffer | 99 _H |
| * TCON | Timer/Counter Control | 88 _H |
| TH0 | Timer/Counter 0 High Bytes | 8C _H |
| TH1 | Timer/Counter 1 High Bytes | 8D _H |
| TL0 | Timer/Counter 0 Low Bytes | 8A _H |
| TL1 | Timer/Counter 1 Low Bytes | 8B _H |
| * TMOD | Timer/Counter Mode Control | 89 _H |

* = Bit addressable SFR

Timer/Counter 0 and 1

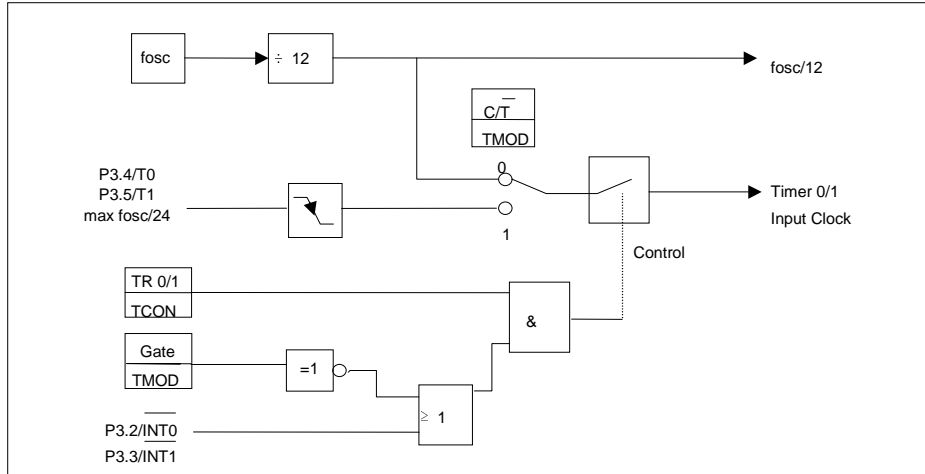
The GMS97C2051/L2051 has two 16-bit Timer/Counter register : Timer0 and Timer1 . As a Timer, the register is incremented every machine cycle. Thus, the register counts machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency. As a counter, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin P3.4/T0 and P3.5/T1. Since 2 machine cycles

are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. External inputs P3.2/INT0 and 3.3/INT1 can be programmed to function as a gate to facilitate pulse width measurements. Timer/Counter 0 and 1 can be used in four operating modes as listed in **Table 4.** **Figure 3** illustrates the input clock logic.

Table 4. Timer / Counter 0 and 1 Operating Modes

| Mode | Description | TMOD | | | |
|------|---|------|-------|----|----|
| | | Gate | C / T | M1 | M0 |
| 0 | 8-bit Timer/Counter with 5-bit prescaler | × | × | 0 | 0 |
| 1 | 16-bit timer/counter | × | × | 0 | 1 |
| 2 | 8-bit Auto-Reload Timer/Counter | × | × | 1 | 0 |
| 3 | (Timer 0) : TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits, TH0 is an 8-bit Timer and is controlled by Timer 1 (Timer 1) : stop | × | × | 1 | 1 |

Figure 3. Time/Counter 0 and 1 Input Clock Logic



Serial Interface (USART)

The serial port is full duplex, meaning it can transmit and receive simultaneously. And it can operate in four modes (one synchronous mode, three asynchronous mode) as illustrated in **table 5**. The possi-

ble baud rates can be calculated using the formulas given in **table 6**.

Table 5. USART Operating Modes

| Mode | SCON | | Baud Rate | Description |
|------|------|-----|-------------------------------------|--|
| | SM0 | SM1 | | |
| 0 | 0 | 0 | fosc / 12 (fixed) | Shift Register : Serial data enters and exits through RXD. TXD outputs the shift clock. Eight data bits are transmitted / received, with the LSB first. |
| 1 | 0 | 1 | Set by Timer (variable) | 8-bit UART : Ten bits are transmitted through TXD, or received through RXD → a start bit (0), 8 data bits (LSB first), and a stop bit (1) |
| 2 | 1 | 0 | fosc / 64 or fosc / 32 (fixed) | 9-bit UART : Eleven bits are transmitted through TXD, or received through RXD → a start bit (0), 8 data bits (LSB first), a programmable ninth data bit , and a stop bit (1) |
| 3 | 1 | 1 | Set by Timer (variable) | 9-bit UART : The same as Mode 2 except the variable baud rate. |

Table 6. Formulas for calculating Baud rates

| Baud Rate generated from | Serial Port Mode | Baud Rate |
|--------------------------|------------------|---|
| Oscillator | 0 2 | $f_{osc} / 12$ $(2^{SMOD} \times f_{osc}) / 64$ |
| Timer1 (Timer1 Mode2) | 1, 3 1, 3 | $(2^{SMOD} \times \text{Timer1 overflow rate}) / 32$ $(2^{SMOD} \times f_{osc}) / [32 \times 12 \times (256 - TH1)]$ |

Interrupt System

The GMS97C2051/L2051 provides 5 interrupt sources (two external interrupts, two timer interrupts and serial port interrupt) with two priority levels. **Figure 4** gives a general overview of the interrupt sources and illustrates the request and control flags.

A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low priority interrupt. A high-priority interrupt cannot

be interrupted by any other interrupt source. If two requests of different priority levels are received simultaneously, the request of higher priority is serviced. If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence like **Table 8**.

Figure 4. Interrupt Request Sources

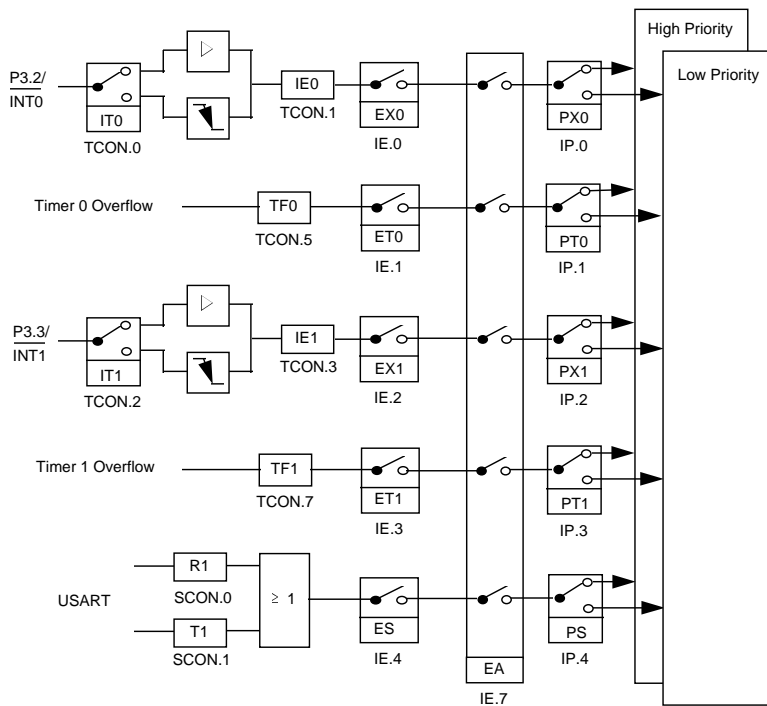


Table 7. Interrupt Sources and their corresponding Interrupt Vectors

| Interrupt | Source | Vector Address |
|-----------------------|---------|----------------|
| External interrupt 0 | IE0 | 0003H |
| Timer0 | TF0 | 000BH |
| External Interrupt 1 | IE1 | 0013H |
| Timer1 | TF1 | 001BH |
| Serial Port Interrupt | RI + TI | 0023H |
| System Reset | RST | 0000H |

Table 8. Interrupt Priority-Within-Level

| Interrupt Source | | Priority |
|-----------------------|---------|----------|
| External interrupt 0 | IE0 | Highest |
| Timer0 interrupt | TF0 | ↓ |
| External Interrupt 1 | IE1 | |
| Timer1 interrupt | TF1 | ↓ |
| Serial Port Interrupt | RI + TI | |

Restrictions on Certain Instructions

The GMS97C2051/L2051 is an economical and cost-effective member of HYUNDAI MicroElectronics growing family of microcontrollers. It contains 2Kbytes of EPROM program memory. It is fully compatible with the MCS-51 architecture, and can be programmed using the MCS-51 instruction set. However, there are a few considerations one must keep in mind when utilizing certain instructions to program this device.

1. Branching instructions:

LCALL, LJMP, ACALL, AJMP, SJMP, JMP @A+DPTR

These unconditional branching instructions will execute correctly as long as the programmer keeps in mind that the destination branching address must fall within the physical boundaries of the program memory size (locations 00H to 7FFH for the GMS97C2051/L2051). Violating the physical space limits may cause unknown program behavior.

CJNE [...], DJNZ [...], JB, JNB, JC, JNC, JBC, JZ, JNZ

With these conditional branching instructions the same

rule above applies. Again, violating the memory boundaries may cause erratic execution.

For applications involving interrupts the normal interrupt service routine address locations of the 80C51 family architecture have been preserved.

2. MOVX-related instructions, Data Memory:

The GMS97C2051/L2051 contains 128 bytes of internal data memory. Thus, in the GMS97C2051/L2051 the stack depth is limited to 128 bytes, the amount of available RAM. External DATA memory access is not supported in this device, nor is external PROGRAM memory execution. Therefore, no MOVX [...] instructions should be included in the program.

A typical 80C51 assembler will still assemble instructions, even if they are written in violation of the restrictions mentioned above. It is the responsibility of the controller user to know the physical features and limitations of the device being used and adjust the instructions used correspondingly.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset. P1.0 and P1.1 should be set to '0' if no external pullups are used, or set to '1' if external pullups are used.

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following one that invokes Idle should not be one that writes to a port pin or to external memory.

Power Down Mode

GMS97C2051/L2051 have two power saving modes, Idle and Power Down. The bits PD and IDLE of the register PCON select the Power Down mode and the Idle mode, respectively. If 1s are written to PD and IDLE at the same time, PD takes precedence. **Table 9** gives a general overview of the Power saving modes. In the Power Down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the Power Down mode is invoked, and that V_{CC} is restored to its normal operating level, before the Power Down mode is terminated. The reset signal that terminates the Power down mode also restarts the oscillator. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize. (similar to power-on reset).

Table 9. Power Saving Modes Overview

| Mode | Ex. instruction to enter | To terminate | Remarks |
|-----------------|--------------------------|--------------------------------------|---|
| Idle mode | ORL PCON, #01H | Enabled interrupt, Hardware Reset | - CPU is gated off - CPU status registers maintain their data. - Peripherals are active |
| Power-down Mode | ORL PCON, #02H | Hardware Reset | - Oscillator stops - Contents of on-chip RAM and SFRs are maintained - Reset redefines all the SFRs but does not change the on-chip RAM |

Programming The EPROM

The GMS97C2051/L2051 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the P3.2(\overline{PROG}).

The GMS97C2051/L2051 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an manufactured by HME .

Table 10 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the security bits. The circuit configuration and waveforms for quick-pulse programming are shown in **Figures 5** and **Figure 8**. **Figure 6** shows the circuit configuration for normal program memory verification.

EPROM Programming and Verification

Internal Address Counter :

The GMS97C2051/L2051 contains an internal EPROM address counter which is always set to 07FFH on the rising edge of RST after setting P3.0 to 'H' and is advanced by applying continuous level transition to pin P3.0.

Programming Algorithm :

To program the GMS97C2051/L2051, the following sequence is recommended.

1. Power-up Sequence
 - Apply power between V_{CC} and GND pins with crystal oscillation.
 - Set P3.0 to 'H'.
 - Set RST to GND.
 - With all other pins floating, wait for greater than 10ms.
2. Set pin RST to 'H' and pin P3.2 to 'H'.
3. Apply the appropriate combination of 'H' or 'L' logic levels to pins P3.3, P3.4, P3.5, P3.7 to select one of the programming operations shown in the EPROM Programming Modes. (**Table 10**). To program and verify the array
4. The P3.0 level is pulled 'L' and apply data for code byte at location 0000H to P1.0 to P1.7
5. Raise RST to 12.75V to enable programming.
6. The P3.2(\overline{PROG}) is pulsed low 10 times as shown in **Figure 8**. Each programming pulse is low for 100us(± 10 us) and high for a minimum of 10us.
7. To verify the programmed data, lower RST from 12.75V to logic 'H' level and set pins P3.3 to P3.7

to the appropriate levels. Output data can be read at the port P1 pins. At this time P3.0 should not be changed.

8. To program a byte at the next address location, P3.0 level transition is needed to advance the internal address counter. Apply new data to the port P1 pins.
9. Repeat step 5 through 8, changing data and advancing the address counter for the entire 2K bytes array.

Program Verify :

If lock bits LB1 and LB2 have not been programmed, code data can be read back via port P1 pins.

1. Set the internal address counter to 07FFH by bringing RST from 'L' to 'H' and reset the internal address counter to 0000H by bringing P3.0 from 'H' to 'L'.
2. Apply the appropriate control signals for Read Code data to pins P3.3, P3.4, P3.5, P3.7 and read the output data at the port P1 pins.
3. The P3.0 level transition is taken to advance the internal address counter.
4. Read the next code data byte at the port P1 pins.
5. Repeat step 3 and 4 until the entire array is read.

Program Memory Lock Bits

The two-level Program Lock system consists of 2 Lock bits and a 32-byte Encryption Array which are used to protect the program memory against software piracy.

Encryption Array :

Within the EPROM array are 32 bytes of Encryption Array that are initially unprogrammed (all 1s). Every time that a byte is addressed during a verify, address lines are used to select a byte of the Encryption array. This byte is then exclusive-NORed (XNOR) with the code byte, creating an Encrypted Verify byte.

The algorithm, with the array in the unprogrammed state (all 1s), will return the code in its original, unmodified form. It is recommended that whenever the Encryption Array is used, at least one of the Lock Bits be programmed as well.

Lock Bit Protection Modes

| Program Lock Bits | | | Protection Type |
|-------------------|-----|---|---|
| LB1 | LB2 | | |
| 1 | U | U | No program lock features. |
| 2 | P | U | Further programming of the EPROM is disabled. |
| 3 | P | P | Same as mode 2, also verify is disabled. |

Reading the Signature Bytes :

The signature bytes are read by the same procedure as a normal verification of locations 000H and 001H, except that P3.5 and P3.7 need to be pulled to a logic low.

Manufacturer ID:

(00H) = E0H (Indicates manufactured by HEI)





Device ID:

(01H) = 26H (Indicates GMS97C2051/L2051)

U : unprogrammed, P : programmed

EPROM Programming Modes

Table 10. EPROM Programming Modes

| Mode | RST | P3.2/ $\overline{\text{PROG}}$ | P3.3 | P3.4 | P3.5 | P3.7 |
|----------------------|-----|---|------|------|------|------|
| Read Signature | 1 | 1 | 0 | 0 | 0 | 0 |
| Program Code Data | Vpp |  | 0 | 1 | 1 | 1 |
| Verify Code Data | 1 | 1 | 0 | 0 | 1 | 1 |
| Pgm encryption table | Vpp |  | 0 | 1 | 0 | 1 |
| Pgm encryption bit1 | Vpp |  | 1 | 1 | 1 | 1 |
| Pgm encryption bit | Vpp |  | 1 | 1 | 0 | 0 |

Notes: 1. '0' = Valid low, '1' = Valid high for that pin.

2. Vpp = 12.75 V \pm 0.25 V

3. Vcc = 5 V \pm 10 % during programming and verification.

4. P3.2/ $\overline{\text{PROG}}$ receives 10 programming pulses while Vpp is held at 12.75V. Each programming pulse is low for 100uS (\pm 10uS) and high for a minimum of 10uS.

Figure 5. Programming the EPROM Memory

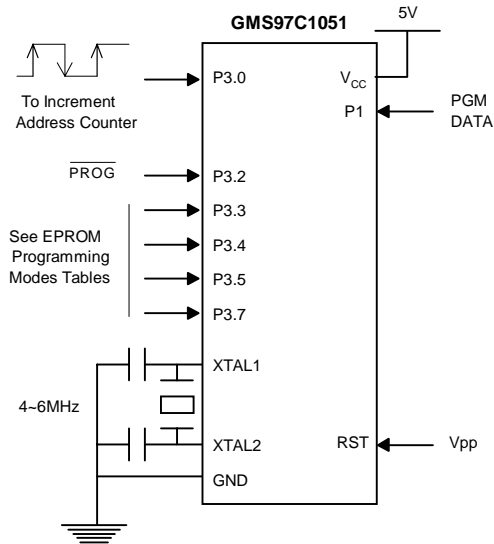
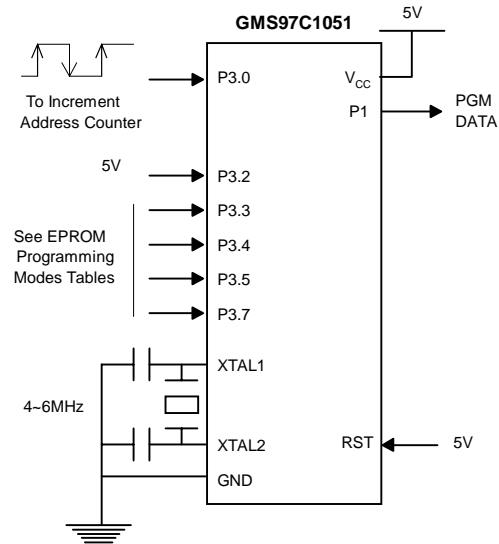


Figure 6. Verifying the EPROM Memory



EPROM Programming and Verification Characteristics

Table 11. EPROM Programming and Verification Characteristics

| Parameter | Symbol | Min | Max | Units |
|---|----------------|---------------|---------------|-------|
| Programming Supply Voltage | V_{PP} | 12.5 | 13.0 | V |
| Programming Supply Current | I_{PP} | | 50 | mA |
| Oscillator Frequency | $1 / t_{CLCL}$ | 4 | 6 | MHz |
| Address Setup to \overline{PROG} Low | t_{AVGL} | 48 t_{CLCL} | | |
| Data Setup to \overline{PROG} Low | t_{DVGL} | 48 t_{CLCL} | | |
| Data Hold after \overline{PROG} | t_{GHDX} | 48 t_{CLCL} | | |
| P3.4 (\overline{ENABLE}) High to V_{PP} | t_{EHS} | 48 t_{CLCL} | | |
| V_{PP} Setup to \overline{PROG} Low | t_{SHGL} | 10 | | us |
| V_{PP} Hold After \overline{PROG} | t_{GHSL} | 10 | | us |
| \overline{PROG} Width | t_{GLGH} | 90 | 110 | us |
| \overline{PROG} High to \overline{PROG} Low | t_{GHGL} | 10 | | us |
| P3.4 (\overline{ENABLE}) Low to Data Valid | t_{ELQV} | | 48 t_{CLCL} | |
| Data Float after P3.4 (\overline{ENABLE}) | t_{EHOZ} | 0 | 48 t_{CLCL} | |

$T_A = 21^\circ\text{C}$ to 27°C , $V_{CC} = 5.0 \pm 10\%$

EPROM Programming and Verification Waveforms

Figure 7. EPROM Programming and Verification

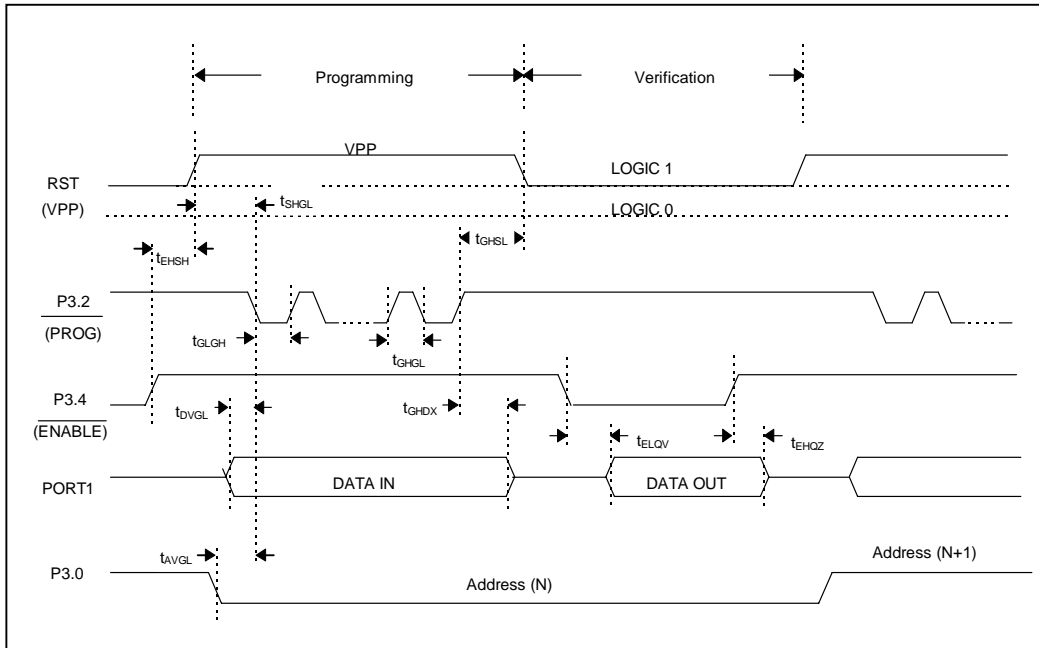
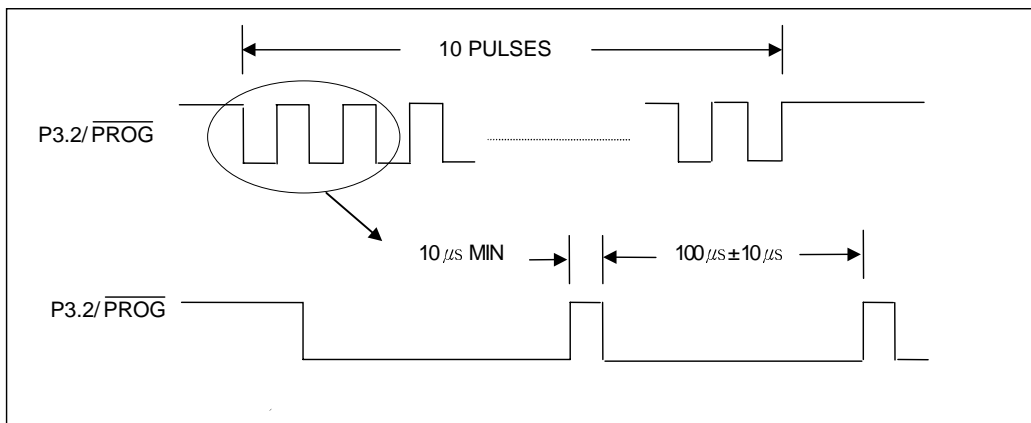


Figure 8. Programming Waveform



Absolute Maximum Ratings

| | |
|---|------------------------|
| Ambient temperature under bias (T_A)..... | - 40°C to + 85°C |
| Storage temperature (T_{ST}) | -65°C to + 150°C |
| Voltage on V_{CC} pin with respect to Ground(V_{SS})..... | -0.5V to 6.5V |
| Voltage on any pin with respect to Ground(V_{SS})... | -0.5V to $V_{CC}+0.5V$ |
| Input Current on any pin during overload condition..... | -10mA to +10mA |
| Absolute sum of all input current during overload condition..... | 100 mA |

NOTE : Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

D.C. Characteristics (5V Version)

$V_{CC} = 4.25V$ to $5.5V$, $V_{SS} = 0V$, $T_A = 0^{\circ}C$ to $70^{\circ}C$

for the

GMS97C2051/C1051

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|--|--------------|------------------------------------|-----------------|---------|---|
| | | Min | Max | | |
| Input Low Voltage | V_{IL} | -0.5 | $0.2V_{CC}-0.1$ | V | |
| Input High Voltage (Except XTAL1, RST) | V_{IH} | $0.5V_{CC}-0.1$ | $V_{CC}+0.5$ | V | |
| Input High Voltage (XTAL1, RST) | V_{IH1} | $0.7V_{CC}$ | $V_{CC}+0.5$ | V | |
| Output Low Voltage (ports 1,3) | V_{OL} | | 0.45 | V | $I_{OL}=10mA, V_{CC}=5V$ |
| Output High Voltage (ports 1,3) | V_{OH} | 2.4 $0.75V_{CC}$ $0.9V_{CC}$ | | V | $I_{OH} = -80\mu A, V_{CC}=5V \pm 10\%$ $I_{OH} = -30\mu A$ $I_{OH} = -12\mu A$ |
| Logical 0 Input Current (ports 1,3) | I_{IL} | | -50 | μA | $V_{IN}=0.45V$ |
| Logical 1-to-0 Transition Current (ports 1,3) | I_{TL} | | -750 | μA | $V_{IN}=2V$ |
| Input Leakage Current (Port P1.0, P1.1) | I_{LI} | | $\pm 1\mu A$ | μA | $0 < V_{IN} < V_{CC}$ |
| Comparator Input Offset Voltage | V_{OS} | | 200 | mV | $V_{CC}=5V$ |
| Comparator Input Common Mode Voltage | V_{CM} | 0 | V_{CC} | V | |
| Pin Capacitance | C_{IO} | | 10 | pF | Test Freq.=1MHz, $T_A=25^{\circ}C$ |
| Power supply current: Active mode, 12Mhz | I_{CC} | | 20 | mA | $V_{CC}=5.0V$ |
| Idle mode, 12Mhz | I_{CCidle} | | 12 | mA | $V_{CC}=5.0V, P1.0 \& P1.1=0$ or V_{CC} |
| Active mode, 24Mhz | I_{CC} | | 30 | mA | $V_{CC}=5.0V$ |
| Idle mode, 24Mhz | I_{CCidle} | | 15 | mA | $V_{CC}=5.0V, P1.0 \& P1.1=0$ or V_{CC} |
| Power Down mode | I_{PD} | | 100 | μA | $V_{CC}=5.0V, P1.0 \& P1.1=0$ or V_{CC} |

D.C. Characteristics (3V Version)

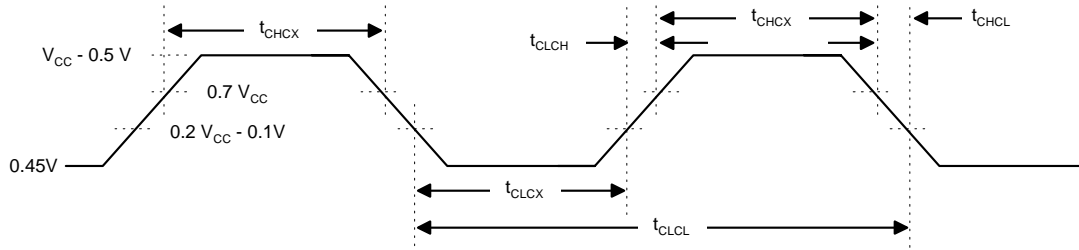
$V_{CC} = 2.7V$ to $3.6V$, $V_{SS} = 0V$, $T_A = 0^{\circ}C$ to $70^{\circ}C$

for the

GMS97L2051/L1051

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|--|--------------------------------------|-----------------------------|-----------------|---------------------|---|
| | | Min | Max | | |
| Input Low Voltage | V_{IL} | -0.5 | $0.2V_{CC}-0.1$ | V | |
| Input High Voltage (Except XTAL1, RST) | V_{IH} | $0.5V_{CC}-0.1$ | $V_{CC}+0.5$ | V | |
| Input High Voltage (XTAL1, RST) | V_{IH1} | $0.7V_{CC}$ | $V_{CC}+0.5$ | V | |
| Output Low Voltage (ports 1,3) | V_{OL} | | 0.45 | V | $I_{OL}=6mA, V_{CC}=2.7V$ |
| Output High Voltage (ports 1,3) | V_{OH} | $0.75V_{CC}$ $0.9V_{CC}$ | | V | $I_{OH} = -30\mu A$ $I_{OH} = -12\mu A$ |
| Logical 0 Input Current (ports 1,3) | I_{IL} | | -50 | μA | $V_{IN}=0.45V$ |
| Logical 1-to-0 Transition Current (ports 1,3) | I_{TL} | | -750 | μA | $V_{IN}=2V$ |
| Input Leakage Current (Port P1.0, P1.1) | I_{LI} | | $\pm 1\mu A$ | μA | $0 < V_{IN} < V_{CC}$ |
| Comparator Input Offset Voltage | V_{OS} | | 200 | mV | $V_{CC}=3V$ |
| Comparator Input Common Mode Voltage | V_{CM} | 0 | V_{CC} | V | |
| Pin Capacitance | C_{IO} | | 10 | pF | Test Freq.=1MHz, $T_A=25^{\circ}C$ |
| Power supply current: Active mode, 12Mhz Idle mode, 12Mhz Power Down mode | I_{CC} I_{CCidle} I_{PD} | | 10 5 50 | mA mA μA | $V_{CC}=3V$ $V_{CC}=3V, P1.0 \& P1.1=0$ or V_{CC} $V_{CC}=3V, P1.0 \& P1.1=0$ or V_{CC} |

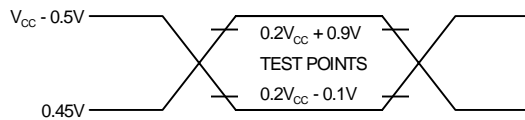
External Clock drive waveforms



External Clock Drive

| Symbol | Parameter | GMS97L2051/L1051 | | GMS97C2051/C1051 | | Units |
|--------------|----------------------|------------------|-----|------------------|-----|-------|
| | | Min | Max | Min | Max | |
| $1/t_{CLCL}$ | Oscillator Frequency | 0 | 12 | 0 | 24 | MHz |
| t_{CLCL} | Clock Period | 83.3 | | 41.6 | | ns |
| t_{CHCX} | High Time | 30 | | 15 | | ns |
| t_{CLCX} | Low Time | 30 | | 15 | | ns |
| t_{CLCH} | Rise Time | - | 20 | - | 20 | ns |
| t_{CHCL} | Fall Time | - | 20 | - | 20 | ns |

AC Testing Input/Output Waveforms⁽¹⁾



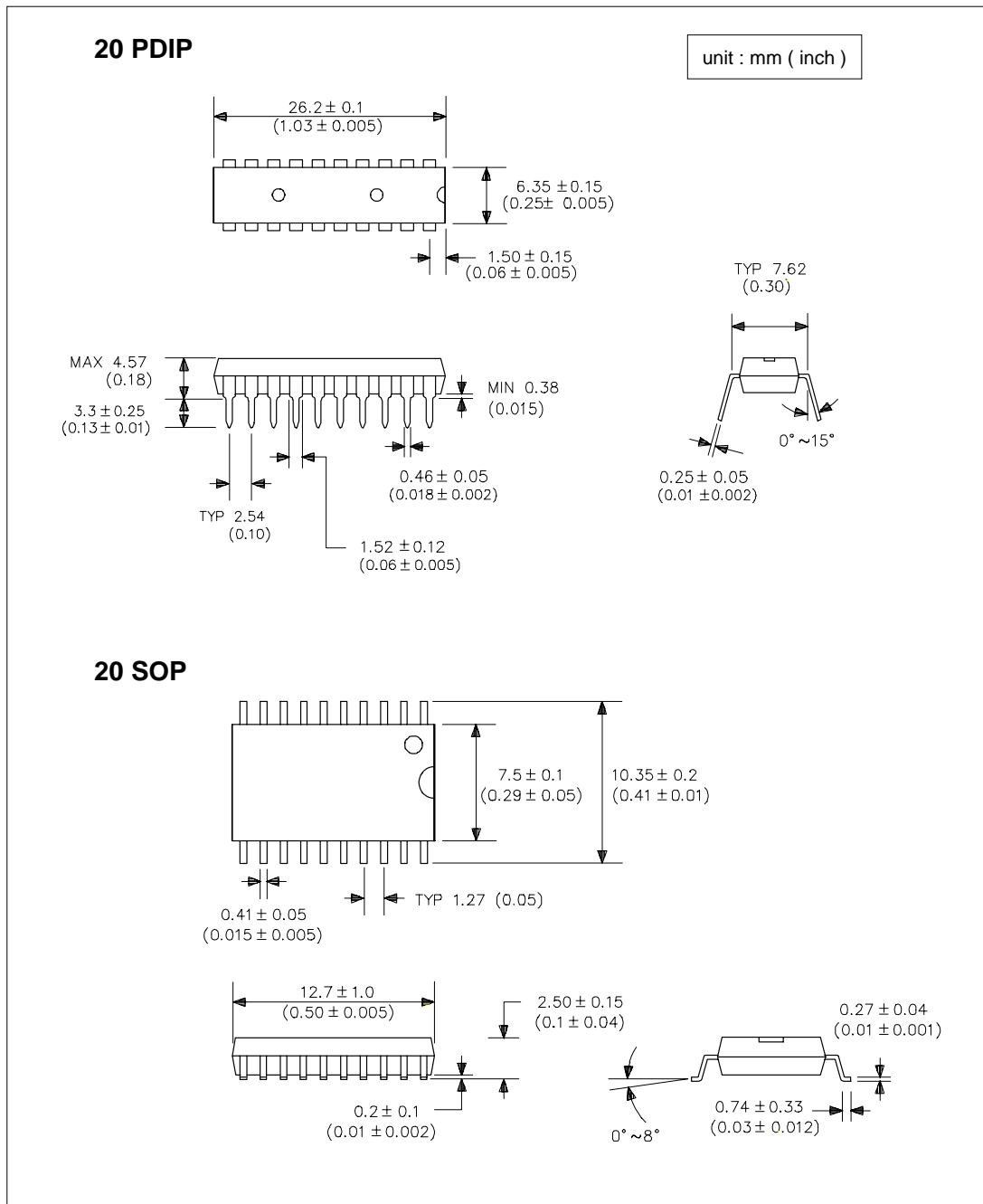
Note: 1. AC Inputs during testing are driven at $V_{CC} - 0.5V$ for a logic 1 and $0.45V$ for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms⁽¹⁾



Note: 1. For timing purposes, a port pin is no longer floating when a $100mV$ change from load voltage occurs. A port pin begins to float when a $100mV$ change from the loaded V_{OH}/V_{OL} level occurs.

Package Dimension



Ordering Information

| Speed (MHz) | Power Supply | Ordering Code | Package | Operation Range |
|--------------|---------------|----------------|---------|-----------------------------|
| 12 | 2.7V to 3.6V | GMS97L2051 | 20 PDIP | Commercial (0°C to 70°C) |
| | | GMS97L2051-D | 20 SOP | |
| | 4.25V to 5.5V | GMS97C2051 | 20 PDIP | |
| | | GMS97C2051-D | 20 SOP | |
| 24 | 4.25V to 5.5V | GMS97C2051-24 | 20 PDIP | |
| | | GMS97C2051-24D | 20 SOP | |

| Package Type | |
|----------------|---|
| 20 PDIP | 20 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 20 SOP | 20 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOP) |

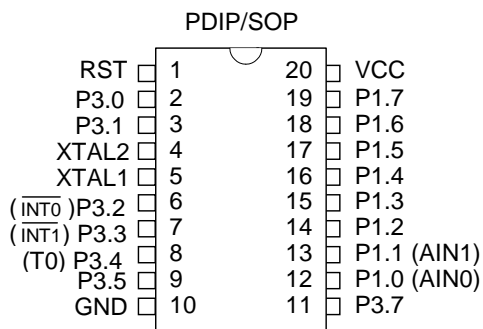
Features

- Compatible with MCS-51™ Products
- 1 Kbytes of programmable EPROM
- 4.25V to 5.5V Operating Range (GMS97C1051)
2.70V to 3.6V Operating Range (GMS97L1051)
- Version for 12MHz / 24 MHz Operating frequency (GMS97C1051)
Only 12MHz Operating frequency (GMS97L1051)
- Two-Level Program Memory Lock with encryption array
- 64 bytes SRAM
- 15 Programmable I/O Lines
- One 16-Bit Timer/Counter
- Three Interrupt Sources
- Direct LED Drive Outputs
- On-Chip Analog Comparator
- Low Power Idle and Power Down Modes

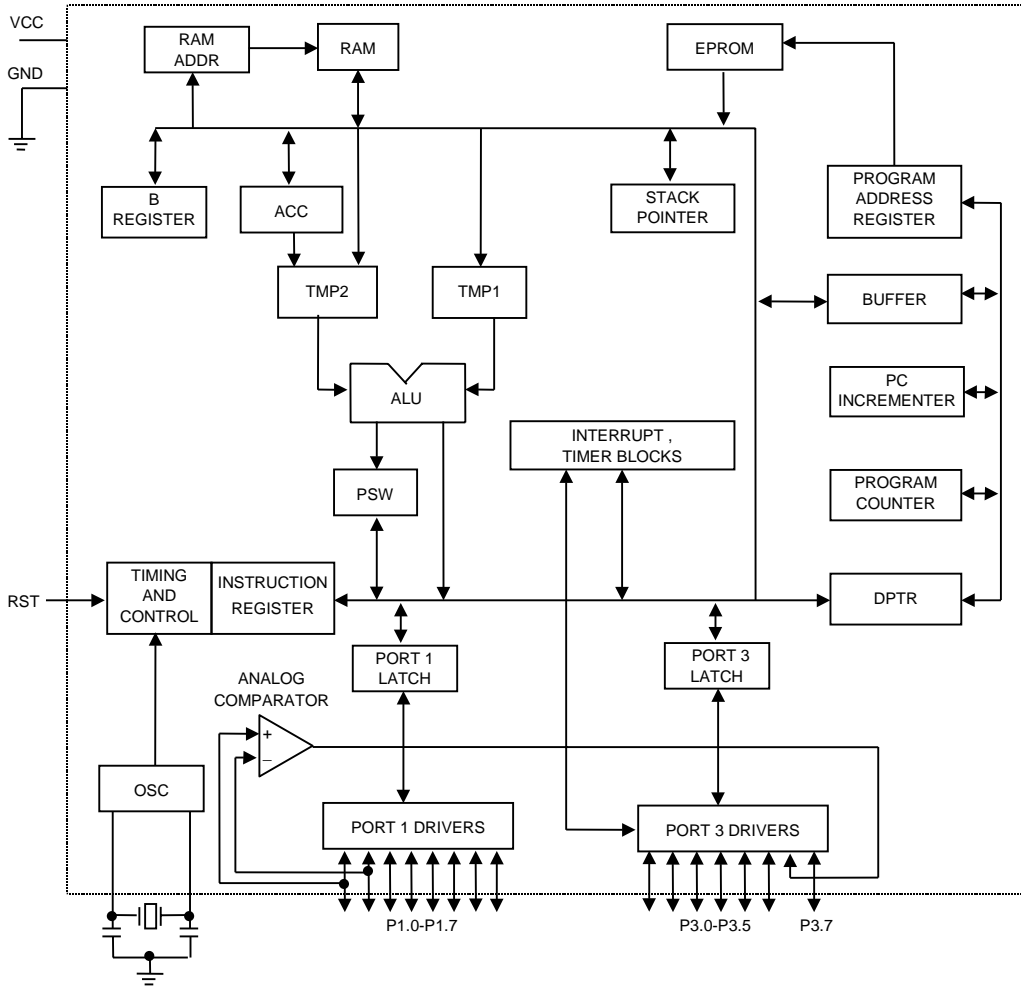
Description

The GMS97C1051/L1051 is a high-performance CMOS 8-bit microcontroller with 1Kbytes of programmable EPROM. The device is compatible with the industry standard MCS-51™ instruction set and pinout. The HYUNDAI MicroElectronics GMS97C1051/L1051 is a powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. The GMS97C1051/L1051 provides the following standard features: 1Kbytes of EPROM, 64 bytes of RAM, 15 I/O lines, 16-bit timer/counter, a three vector two-level interrupt architecture, a precision analog comparator, on-chip oscillator and clock circuitry. In addition, the GMS97C1051/L1051 supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

Pin Configuration



Block Diagram



Pin Description

V_{CC}

Supply voltage.

GND

Ground.

Port 1

Port 1 is an 8-bit bidirectional I/O port. Port pins P1.2 to P1.7 provide internal pullups. P1.0 and P1.1 require external pullups. P1.0 and P1.1 also serve as the positive input (AIN0) and the negative input (AIN1), respectively, of the on-chip precision analog comparator. The Port 1 output buffers can sink 10mA and can drive LED displays directly. When 1s are written to Port1 pins, they can be used as inputs. When pins P1.2 to P1.7 are used as inputs and are externally pulled low, they will source current (I_{IL}) because of the internal pullups.

Port 1 also receives code data during EPROM programming and program verification.

Port3

Port 3 pins P3.0 to P3.5, P3.7 are seven bidirectional I/O pins with internal pullups. P3.6 is hard-wired as an input to the output of the on-chip comparator and is not accessible as a general purpose I/O pin. The Port 3 output buffers can sink 10mA. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special feature of the GMS97C1051/L1051 as listed below:

| Port Pin | Alternate Functions |
|----------|---|
| P3.2 | $\overline{\text{INT0}}$ (external interrupt 0) |
| P3.3 | $\overline{\text{INT1}}$ (external interrupt 1) |
| P3.4 | T0 (timer 0 external input) |

Port 3 also receives some control signals for EPROM programming and programming verification.

RST

Reset input. All I/O pins are reset to 1s as soon as RST goes high. Holding the RST pin high for two machine cycles while the oscillator is running resets the device.

This pin is also receives the 12.75V programming supply voltage (V_{pp}) during EPROM programming.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

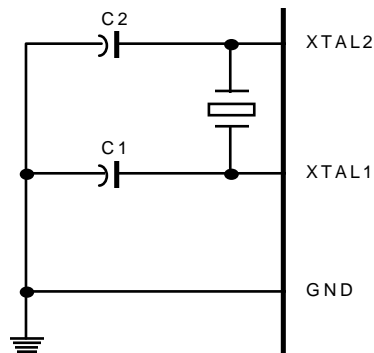
XTAL2

Output from the inverting oscillator amplifier.

Recommended Oscillator Circuit

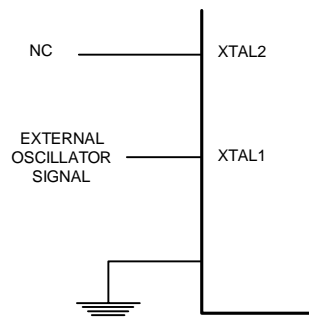
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in **Figure 1**. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in **Figure 2**.

Figure 1. Oscillator Connections



Notes: C1, C2 = 30pF± 10pF for Crystals (include stray capacitance)

Figure 2. External Clock Drive Configuration



Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in the **Table 1**, **Table 2** and **Table 3**.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

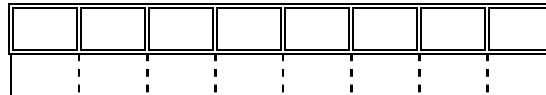
Table 1. GMS97C1051/L1051 SFR Map and Reset Values

| | | | | | | | | |
|------|------------------|------------------|-----------------|-----------------|-----------------|--|------------------|------|
| 0F8H | | | | | | | | 0FFH |
| 0F0H | B 00000000 | | | | | | | 0F7H |
| 0E8H | | | | | | | | 0EFH |
| 0E0H | ACC 00000000 | | | | | | | 0E7H |
| 0D8H | | | | | | | | 0DFH |
| 0D0H | PSW 00000000 | | | | | | | 0D7H |
| 0C8H | | | | | | | | 0CFH |
| 0C0H | | | | | | | | 0C7H |
| 0B8H | IP XXX00000 | | | | | | | 0BFH |
| 0B0H | P3 11111111 | | | | | | | 0B7H |
| 0A8H | IE 0XX00000 | | | | | | | 0AFH |
| 0A0H | | | | | | | | 0A7H |
| 98H | | | | | | | | 9FH |
| 90H | P1 11111111 | | | | | | | 97H |
| 88H | TCON 00000000 | TMOD 00000000 | TL0 00000000 | | TH0 00000000 | | | 8FH |
| 80H | | SP 00000111 | DPL 00000000 | DPH 00000000 | | | PCON 0XXX0000 | 87H |

Table 2. Bit Assignment of SFRs

| Address | Register | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-----------------|----------|------|------|------|------|------|---------------|------|------|
| 81 _H | SP | | | | | | | | |
| 82 _H | DPL | | | | | | | | |
| 83 _H | DPH | | | | | | | | |
| 87 _H | PCON | - | - | - | - | GF1 | GF0 | PD | IDLE |
| 88 _H | TCON | - | - | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 |
| 89 _H | TMOD | - | - | - | - | GATE | C / \bar{T} | M1 | M0 |
| 8A _H | TL0 | | | | | | | | |
| 8C _H | TH0 | | | | | | | | |
| 90 _H | P1 | | | | | | | | |
| A8 _H | IE | EA | - | - | - | - | EX1 | ET0 | EX0 |
| B0 _H | P3 | | | | | | | | |
| B8 _H | IP | - | - | - | - | - | PX1 | PT0 | PX0 |
| D0 _H | PSW | CY | AC | F0 | RS1 | RS0 | OV | F1 | P |
| E0 _H | ACC | | | | | | | | |
| F0 _H | B | | | | | | | | |

- : This Bit Location is reserved



Bit manipulation is available

Bit manipulation is not available

Table 3. SFR lists and their addresses

| Symbol | Name | Address |
|--------|----------------------------|-----------------|
| * ACC | Accumulator | E0 _H |
| * B | B Register | F0 _H |
| DPH | Data Pointer High Byte | 83 _H |
| DPL | Data Pointer Low Byte | 82 _H |
| * PSW | Program Status Word | D0 _H |
| SP | Stack Pointer | 81 _H |
| * IE | Interrupt Enable Control | A8 _H |
| * IP | Interrupt Priority Control | B8 _H |
| * P1 | Port 1 | 90 _H |
| * P3 | Port 3 | B0 _H |
| * TCON | Timer/Counter Control | 88 _H |
| TH0 | Timer/Counter 0 High Bytes | 8C _H |
| TL0 | Timer/Counter 0 Low Bytes | 8A _H |
| * TMOD | Timer/Counter Mode Control | 89 _H |

* = Bit addressable SFR

Timer/Counter 0

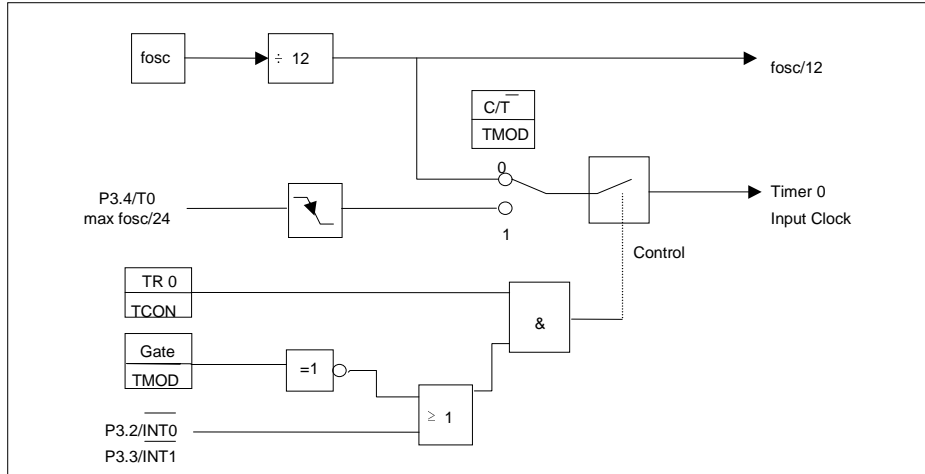
The GMS97C1051/L1051 has one 16-bit Timer/Counter register : Timer0 . As a Timer, the register is incremented every machine cycle. Thus, the register counts machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency. As a counter, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin P3.4/T0. Since 2 machine cycles are required to

recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. External inputs P3.2/INT0 and 3.3/INT1 can be programmed to function as a gate to facilitate pulse width measurements. Timer/Counter 0 can be used in four operating modes as listed in **Table 4.** **Figure 3** illustrates the input clock logic.

Table 4. Timer / Counter 0 Operating Modes

| Mode | Description | _TMOD | | | |
|------|--|-------|-----|----|----|
| | | Gate | C/T | M1 | M0 |
| 0 | 8-bit Timer/Counter with 5-bit prescaler | × | × | 0 | 0 |
| 1 | 16-bit timer/counter | × | × | 0 | 1 |
| 2 | 8-bit Auto-Reload Timer/Counter | × | × | 1 | 0 |
| 3 | (Timer 0) TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits, TH0 is an 8-bit Timer | × | × | 1 | 1 |

Figure 3. Time/Counter 0 Input Clock Logic



Interrupt System

The GMS97C1051/L1051 provides 3 interrupt sources (two external interrupts and timer interrupt) with two priority levels. **Figure 4** gives a general overview of the interrupt sources and illustrates the request and control flags. A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

If two requests of different priority levels are received simultaneously, the request of higher priority is serviced. If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence like **Table 6**.

Figure 4. Interrupt Request Sources

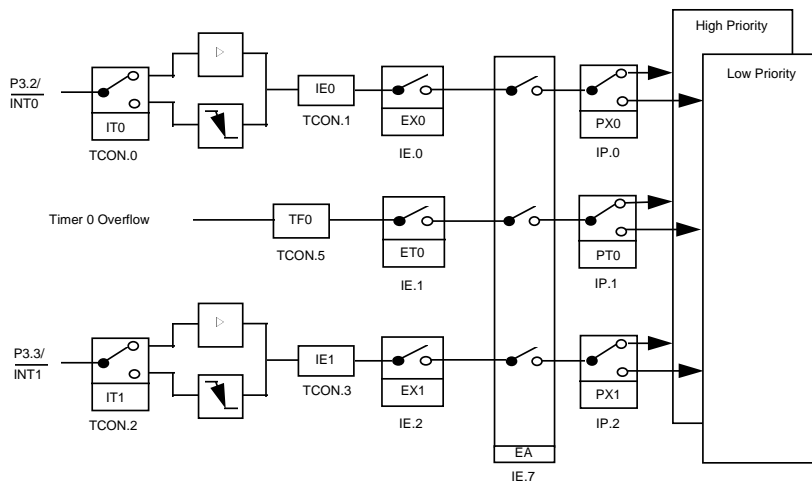


Table 5. Interrupt Sources and their corresponding Interrupt Vectors

| Interrupt | Source | Vector Address |
|----------------------|--------|----------------|
| External interrupt 0 | IE0 | 0003H |
| Timer0 | TF0 | 000BH |
| External Interrupt 1 | IE1 | 0013H |
| System Reset | RST | 0000H |

Table 6. Interrupt Priority-Within-Level

| Interrupt Source | | Priority |
|----------------------|-----|----------|
| External interrupt 0 | IE0 | Highest |
| Timer0 interrupt | TF0 | ↓ |
| External Interrupt 1 | IE1 | |

Restrictions on Certain Instructions

The GMS97C1051/L1051 is an economical and cost-effective member of HYUNDAI MicroElectronics growing family of microcontrollers. It contains 1Kbytes of EPROM program memory. It is fully compatible with the MCS-51 architecture, and can be programmed using the MCS-51 instruction set. However, there are a few considerations one must keep in mind when utilizing certain instructions to program this device.

1. Branching instructions:

LCALL, LJMP, ACALL, AJMP, SJMP, JMP @A+DPTR

These unconditional branching instructions will execute correctly as long as the programmer keeps in mind that the destination branching address must fall within the physical boundaries of the program memory size (locations 00H to 3FFH for the GMS97C1051/L1051). Violating the physical space limits may cause unknown program behavior.

CJNE [...], DJNZ [...], JB, JNB, JC, JNC, JBC, JZ, JNZ
With these conditional branching instructions the same

rule above applies. Again, violating the memory boundaries may cause erratic execution.

For applications involving interrupts the normal interrupt service routine address locations of the 80C51 family architecture have been preserved.

2. MOVX-related instructions, Data Memory:

The GMS97C1051/L1051 contains 64 bytes of internal data memory. Thus, in the GMS97C1051/L1051 the stack depth is limited to 64 bytes, the amount of available RAM. External DATA memory access is not supported in this device, nor is external PROGRAM memory execution. Therefore, no MOVX [...] instructions should be included in the program.

A typical 80C51 assembler will still assemble instructions, even if they are written in violation of the restrictions mentioned above. It is the responsibility of the controller user to know the physical features and limitations of the device being used and adjust the instructions used correspondingly.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset. P1.0 and P1.1 should be set to '0' if no external pullups are used, or set to '1' if external pullups are used.

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following one that invokes Idle should not be one that writes to a port pin or to external memory.

Power Down Mode

GMS97C1051/L1051 have two power saving modes, Idle and Power Down. The bits PD and IDLE of the register PCON select the Power Down mode and the Idle mode, respectively. If 1s are written to PD and IDLE at the same time, PD takes precedence. **Table 7** gives a general overview of the Power saving modes. In the Power Down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the Power Down mode is invoked, and that V_{CC} is restored to its normal operating level, before the Power Down mode is terminated. The reset signal that terminates the Power down mode also restarts the oscillator. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize. (similar to power-on reset).

Table 7. Power Saving Modes Overview

| Mode | Ex. instruction to enter | To terminate | Remarks |
|-----------------|--------------------------|--------------------------------------|---|
| Idle mode | ORL PCON, #01H | Enabled interrupt, Hardware Reset | - CPU is gated off - CPU status registers maintain their data. - Peripherals are active |
| Power-down Mode | ORL PCON, #02H | Hardware Reset | - Oscillator stops - Contents of on-chip RAM and SFRs are maintained - Reset redefines all the SFRs but does not change the on-chip RAM |

Programming The EPROM

The GMS97C1051/L1051 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the P3.2(\overline{PROG}).

The GMS97C1051/L1051 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an manufactured by HME.

Table 8 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the security bits. The circuit configuration and waveforms for quick-pulse programming are shown in **Figures 5** and **Figure 8**. **Figure 6** shows the circuit configuration for normal program memory verification.

EPROM Programming and Verification

Internal Address Counter :

The GMS97C1051/L1051 contains an internal EPROM address counter which is always set to 03FFH on the rising edge of RST after setting P3.0 to 'H' and is advanced by applying continuous level transition to pin P3.0.

Programming Algorithm :

To program the GMS97C1051/L1051, the following sequence is recommended.

1. Power-up Sequence
 - Apply power between V_{CC} and GND pins with crystal oscillation.
 - Set P3.0 to 'H'.
 - Set RST to GND.
 - With all other pins floating, wait for greater than 10ms.
2. Set pin RST to 'H' and pin P3.2 to 'H'.
3. Apply the appropriate combination of 'H' or 'L' logic levels to pins P3.3, P3.4, P3.5, P3.7 to select one of the programming operations shown in the EPROM Programming Modes. (**Table 8**).
To program and verify the array
4. The P3.0 level is pulled 'L' and apply data for code byte at location 0000H to P1.0 to P1.7
5. Raise RST to 12.75V to enable programming.
6. The P3.2(\overline{PROG}) is pulsed low 10 times as shown in **Figure 8**. Each programming pulse is low for 100us(± 10 us) and high for a minimum of 10us.
7. To verify the programmed data, lower RST from 12.75V to logic 'H' level and set pins P3.3 to P3.7

to the appropriate levels. Output data can be read at the port P1 pins. At this time P3.0 should not be changed.

8. To program a byte at the next address location, P3.0 level transition is needed to advance the internal address counter. Apply new data to the port P1 pins.
9. Repeat step 5 through 8, changing data and advancing the address counter for the entire 1K bytes array.

Program Verify :

If lock bits LB1 and LB2 have not been programmed, code data can be read back via port P1 pins.

1. Set the internal address counter to 03FFH by bringing RST from 'L' to 'H' and reset the internal address counter to 0000H by bringing P3.0 from 'H' to 'L'.
2. Apply the appropriate control signals for Read Code data to pins P3.3, P3.4, P3.5, P3.7 and read the output data at the port P1 pins.
3. The P3.0 level transition is taken to advance the internal address counter.
4. Read the next code data byte at the port P1 pins.
5. Repeat step 3 and 4 until the entire array is read.

Program Memory Lock Bits

The two-level Program Lock system consists of 2 Lock bits and a 32-byte Encryption Array which are used to protect the program memory against software piracy.

Encryption Array :

Within the EPROM array are 32 bytes of Encryption Array that are initially unprogrammed (all 1s). Every time that a byte is addressed during a verify, address lines are used to select a byte of the Encryption array. This byte is then exclusive-NORed (XNOR) with the code byte, creating an Encrypted Verify byte.

The algorithm, with the array in the unprogrammed state (all 1s), will return the code in its original, unmodified form. It is recommended that whenever the Encryption Array is used, at least one of the Lock Bits be programmed as well.

Lock Bit Protection Modes

| Program Lock Bits | | | Protection Type |
|-------------------|-----|---|---|
| LB1 | LB2 | | |
| 1 | U | U | No program lock features. |
| 2 | P | U | Further programming of the EPROM is disabled. |
| 3 | P | P | Same as mode 2, also verify is disabled. |

Reading the Signature Bytes :

The signature bytes are read by the same procedure as a normal verification of locations 000H and 001H, except that P3.5 and P3.7 need to be pulled to a logic low.

Manufacturer ID:

(00H) = E0H (Indicates manufactured by HEI)





Device ID:

(01H) = 16H (Indicates GMS97C1051/L1051)

U : unprogrammed, P : programmed

EPROM Programming Modes

Table 8. EPROM Programming Modes

| Mode | RST | P3.2/ $\overline{\text{PROG}}$ | P3.3 | P3.4 | P3.5 | P3.7 |
|----------------------|-----|---|------|------|------|------|
| Read Signature | 1 | 1 | 0 | 0 | 0 | 0 |
| Program Code Data | Vpp |  | 0 | 1 | 1 | 1 |
| Verify Code Data | 1 | 1 | 0 | 0 | 1 | 1 |
| Pgm encryption table | Vpp |  | 0 | 1 | 0 | 1 |
| Pgm encryption bit1 | Vpp |  | 1 | 1 | 1 | 1 |
| Pgm encryption bit | Vpp |  | 1 | 1 | 0 | 0 |

Notes: 1. '0' = Valid low, '1' = Valid high for that pin.

2. Vpp = 12.75 V \pm 0.25 V

3. Vcc = 5 V \pm 10 % during programming and verification.

4. P3.2/ $\overline{\text{PROG}}$ receives 10 programming pulses while Vpp is held at 12.75V. Each programming pulse is low for 100uS (\pm 10uS) and high for a minimum of 10uS.

Figure 5. Programming the EPROM Memory

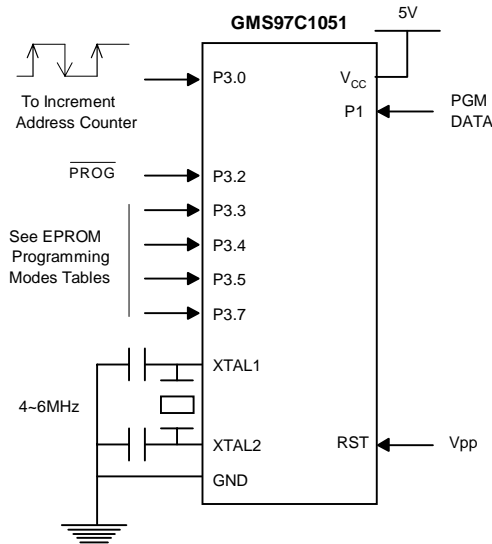
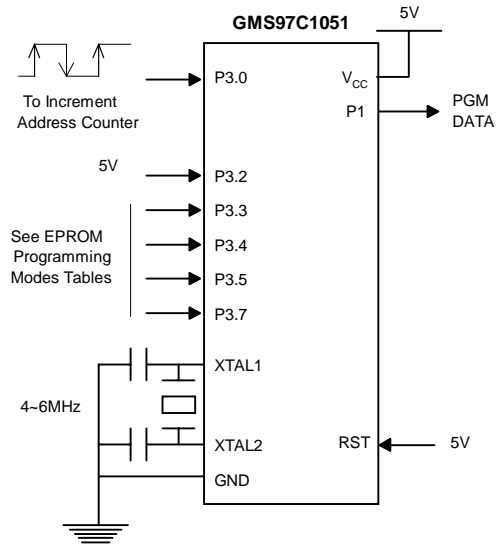


Figure 6. Verifying the EPROM Memory



EPROM Programming and Verification Characteristics

Table 9. EPROM Programming and Verification Characteristics

| Parameter | Symbol | Min | Max | Units |
|---|----------------|---------------|---------------|-------|
| Programming Supply Voltage | V_{PP} | 12.5 | 13.0 | V |
| Programming Supply Current | I_{PP} | | 50 | mA |
| Oscillator Frequency | $1 / t_{CLCL}$ | 4 | 6 | MHz |
| Address Setup to \overline{PROG} Low | t_{AVGL} | $48 t_{CLCL}$ | | |
| Data Setup to \overline{PROG} Low | t_{DVGL} | $48 t_{CLCL}$ | | |
| Data Hold after \overline{PROG} | t_{GHDX} | $48 t_{CLCL}$ | | |
| P3.4 (\overline{ENABLE}) High to V_{PP} | t_{EHS} | $48 t_{CLCL}$ | | |
| V_{PP} Setup to \overline{PROG} Low | t_{SHGL} | 10 | | us |
| V_{PP} Hold After \overline{PROG} | t_{GHSL} | 10 | | us |
| \overline{PROG} Width | t_{GLGH} | 90 | 110 | us |
| \overline{PROG} High to \overline{PROG} Low | t_{GHGL} | 10 | | us |
| P3.4 (\overline{ENABLE}) Low to Data Valid | t_{ELQV} | | $48 t_{CLCL}$ | |
| Data Float after P3.4 (\overline{ENABLE}) | t_{EHOZ} | 0 | $48 t_{CLCL}$ | |

$T_A = 21^\circ\text{C}$ to 27°C , $V_{CC} = 5.0 \pm 10\%$

EPROM Programming and Verification Waveforms

Figure 7. EPROM Programming and Verification

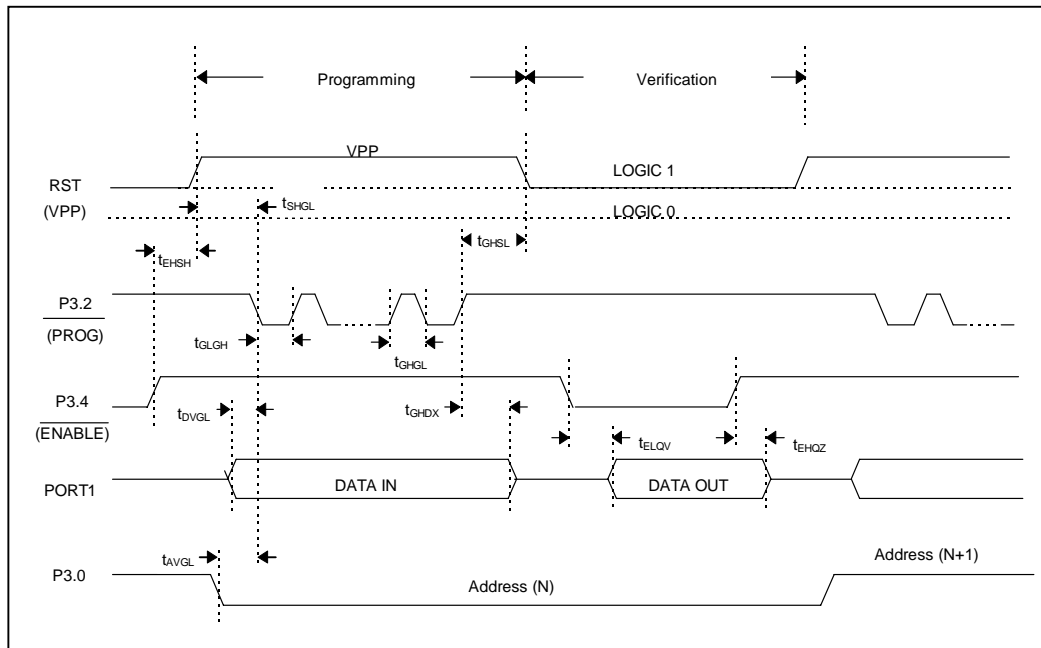
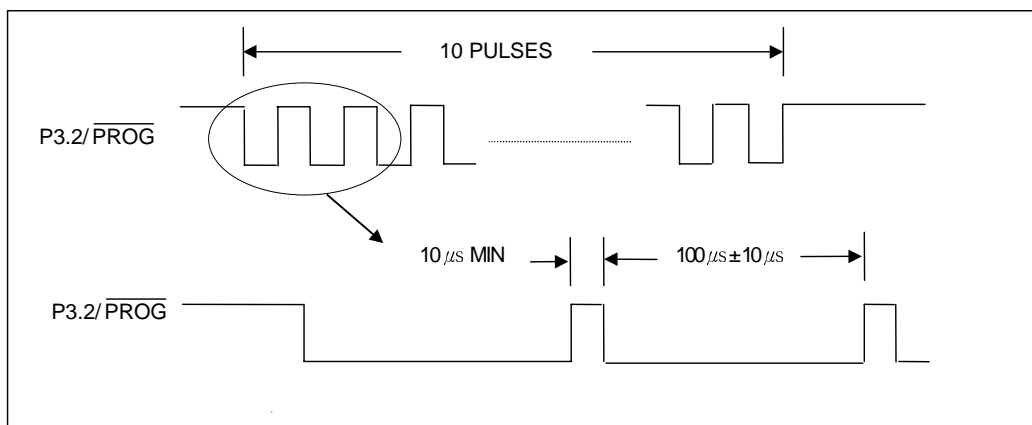


Figure 8. Programming Waveform



Absolute Maximum Ratings

| | |
|---|------------------------|
| Ambient temperature under bias (T_A)..... | - 40°C to + 85°C |
| Storage temperature (T_{ST}) | -65°C to + 150°C |
| Voltage on V_{CC} pin with respect to Ground(V_{SS})..... | -0.5V to +6.6V |
| Voltage on any pin with respect to Ground(V_{SS})... | -0.5V to $V_{CC}+0.5V$ |
| Input Current on any pin during overload condition..... | -10mA to +10mA |
| Absolute sum of all input current during overload condition..... | 100 mA |

NOTE : Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

D.C. Characteristics (5V Version)

$V_{CC} = 4.25V$ to $5.5V$, $V_{SS} = 0V$, $T_A = 0^{\circ}C$ to $70^{\circ}C$

for the

GMS97C2051/C1051

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|--|--------------|------------------------------------|-----------------|---------|---|
| | | Min | Max | | |
| Input Low Voltage | V_{IL} | -0.5 | $0.2V_{CC}-0.1$ | V | |
| Input High Voltage (Except XTAL1, RST) | V_{IH} | $0.5V_{CC}-0.1$ | $V_{CC}+0.5$ | V | |
| Input High Voltage (XTAL1, RST) | V_{IH1} | $0.7V_{CC}$ | $V_{CC}+0.5$ | V | |
| Output Low Voltage (ports 1,3) | V_{OL} | | 0.45 | V | $I_{OL}=10mA, V_{CC}=5V$ |
| Output High Voltage (ports 1,3) | V_{OH} | 2.4 $0.75V_{CC}$ $0.9V_{CC}$ | | V | $I_{OH} = -80\mu A, V_{CC}=5V \pm 10\%$ $I_{OH} = -30\mu A$ $I_{OH} = -12\mu A$ |
| Logical 0 Input Current (ports 1,3) | I_{IL} | | -50 | μA | $V_{IN}=0.45V$ |
| Logical 1-to-0 Transition Current (ports 1,3) | I_{TL} | | -750 | μA | $V_{IN}=2V$ |
| Input Leakage Current (Port P1.0, P1.1) | I_{LI} | | $\pm 1\mu A$ | μA | $0 < V_{IN} < V_{CC}$ |
| Comparator Input Offset Voltage | V_{OS} | | 200 | mV | $V_{CC}=5V$ |
| Comparator Input Common Mode Voltage | V_{CM} | 0 | V_{CC} | V | |
| Pin Capacitance | C_{IO} | | 10 | pF | Test Freq.=1MHz, $T_A=25^{\circ}C$ |
| Power supply current: Active mode, 12Mhz | I_{CC} | | 20 | mA | $V_{CC}=5.0V$ |
| Idle mode, 12Mhz | I_{CCidle} | | 12 | mA | $V_{CC}=5.0V, P1.0 \& P1.1=0$ or V_{CC} |
| Active mode, 24Mhz | I_{CC} | | 30 | mA | $V_{CC}=5.0V$ |
| Idle mode, 24Mhz | I_{CCidle} | | 15 | mA | $V_{CC}=5.0V, P1.0 \& P1.1=0$ or V_{CC} |
| Power Down mode | I_{PD} | | 100 | μA | $V_{CC}=5.0V, P1.0 \& P1.1=0$ or V_{CC} |

D.C. Characteristics (3V Version)

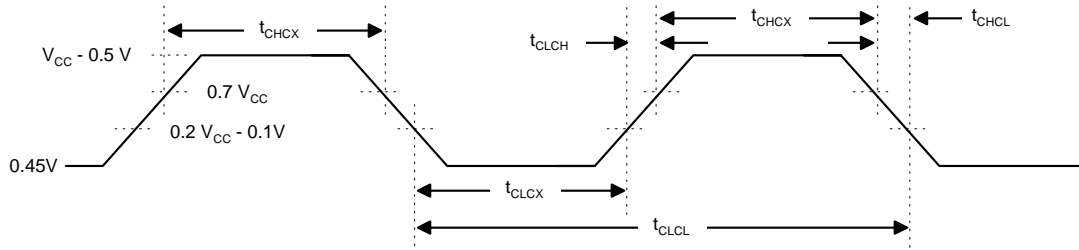
$V_{CC} = 2.7V$ to $3.6V$, $V_{SS} = 0V$, $T_A = 0^{\circ}C$ to $70^{\circ}C$

for the

GMS97L2051/L1051

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|--|--------------------------------------|-----------------------------|-----------------|---------------------|---|
| | | Min | Max | | |
| Input Low Voltage | V_{IL} | -0.5 | $0.2V_{CC}-0.1$ | V | |
| Input High Voltage (Except XTAL1, RST) | V_{IH} | $0.5V_{CC}-0.1$ | $V_{CC}+0.5$ | V | |
| Input High Voltage (XTAL1, RST) | V_{IH1} | $0.7V_{CC}$ | $V_{CC}+0.5$ | V | |
| Output Low Voltage (ports 1,3) | V_{OL} | | 0.45 | V | $I_{OL}=6mA, V_{CC}=2.7V$ |
| Output High Voltage (ports 1,3) | V_{OH} | $0.75V_{CC}$ $0.9V_{CC}$ | | V | $I_{OH} = -30\mu A$ $I_{OH} = -12\mu A$ |
| Logical 0 Input Current (ports 1,3) | I_{IL} | | -50 | μA | $V_{IN}=0.45V$ |
| Logical 1-to-0 Transition Current (ports 1,3) | I_{TL} | | -750 | μA | $V_{IN}=2V$ |
| Input Leakage Current (Port P1.0, P1.1) | I_{LI} | | $\pm 1\mu A$ | μA | $0 < V_{IN} < V_{CC}$ |
| Comparator Input Offset Voltage | V_{OS} | | 200 | mV | $V_{CC}=3V$ |
| Comparator Input Common Mode Voltage | V_{CM} | 0 | V_{CC} | V | |
| Pin Capacitance | C_{IO} | | 10 | pF | Test Freq.=1MHz, $T_A=25^{\circ}C$ |
| Power supply current: Active mode, 12Mhz Idle mode, 12Mhz Power Down mode | I_{CC} I_{CCidle} I_{PD} | | 10 5 50 | mA mA μA | $V_{CC}=3V$ $V_{CC}=3V, P1.0\&P1.1=0$ or V_{CC} $V_{CC}=3V, P1.0\&P1.1=0$ or V_{CC} |

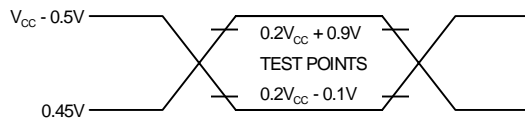
External Clock drive waveforms



External Clock Drive

| Symbol | Parameter | GMS97L2015/L1051 | | GMS97C2051/C1051 | | Units |
|--------------|----------------------|------------------|-----|------------------|-----|-------|
| | | Min | Max | Min | Max | |
| $1/t_{CLCL}$ | Oscillator Frequency | 0 | 12 | 0 | 24 | MHz |
| t_{CLCL} | Clock Period | 83.3 | | 41.6 | | ns |
| t_{CHCX} | High Time | 30 | | 15 | | ns |
| t_{CLCX} | Low Time | 30 | | 15 | | ns |
| t_{CLCH} | Rise Time | - | 20 | - | 20 | ns |
| t_{CHCL} | Fall Time | - | 20 | - | 20 | ns |

AC Testing Input/Output Waveforms⁽¹⁾



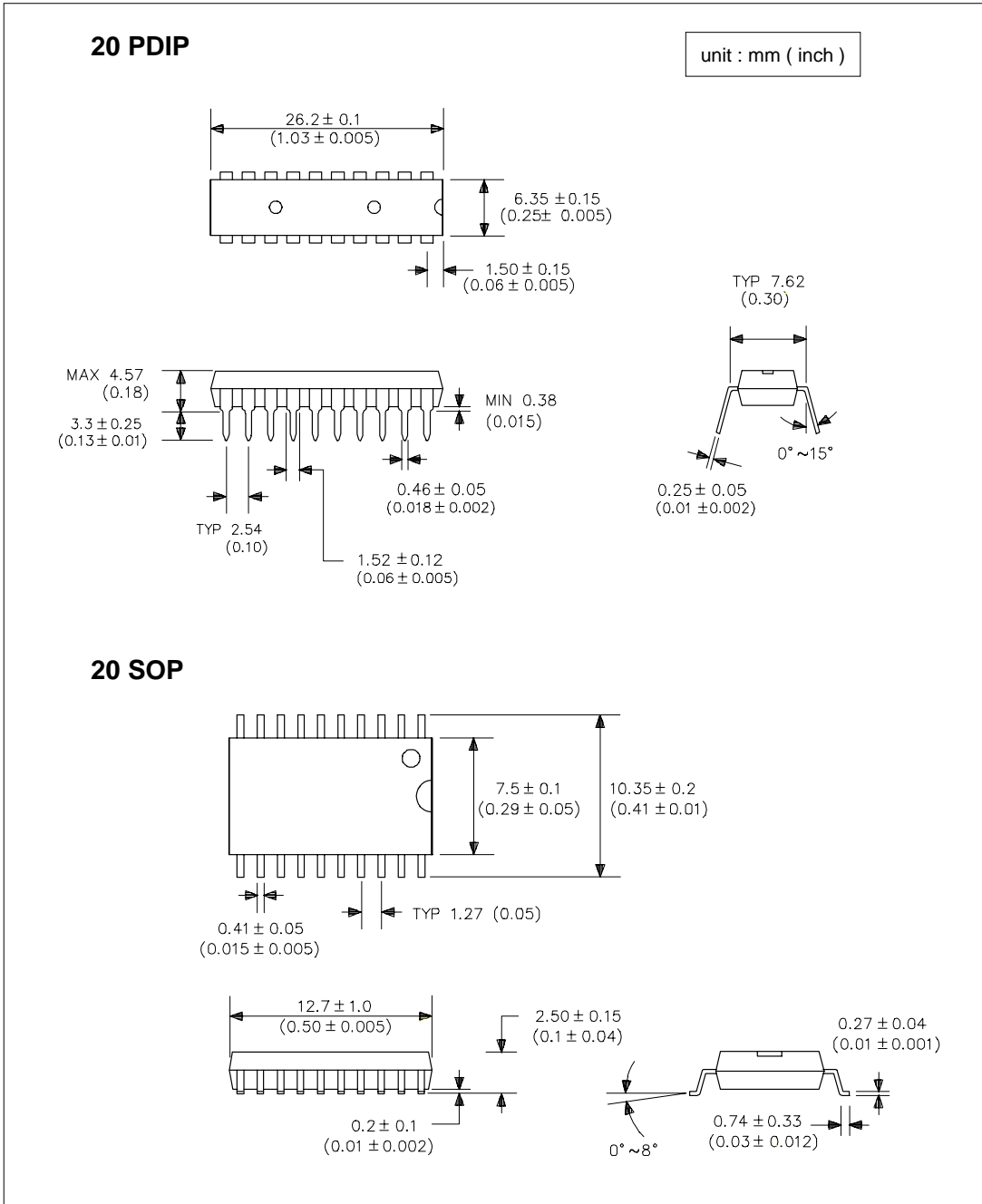
Note: 1. AC Inputs during testing are driven at $V_{CC} - 0.5V$ for a logic 1 and $0.45V$ for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms⁽¹⁾



Note: 1. For timing purposes, a port pin is no longer floating when a $100mV$ change from load voltage occurs. A port pin begins to float when a $100mV$ change from the loaded V_{OH}/V_{OL} level occurs.

Package Dimension



Ordering Information

| Speed (MHz) | Power Supply | Ordering Code | Package | Operation Range |
|--------------|---------------|----------------|---------|-----------------------------|
| 12 | 2.7V to 3.6V | GMS97L1051 | 20 PDIP | Commercial (0°C to 70°C) |
| | | GMS97L1051-D | 20 SOP | |
| | 4.25V to 5.5V | GMS97C1051 | 20 PDIP | |
| | | GMS97C1051-D | 20 SOP | |
| 24 | 4.25V to 5.5V | GMS97C1051-24 | 20 PDIP | |
| | | GMS97C1051-24D | 20 SOP | |

| Package Type | |
|----------------|---|
| 20 PDIP | 20 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 20 SOP | 20 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOP) |