Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 16K (2K x 8-BIT) WITH INTERRUPTS

IDT71321SA/LA
IDT71421SA/LA

T-46-23-12

FEATURES:

- High-speed access
  - —Military: 25/30/35/45/55/70ns (max.)
  - —Commercial: 20/25/30/35/45/55ns (max.)
- Low-power operation
  - —IDT71321/IDT71421SA
    - Active: 325mW (typ.)
    - Standby: 5mW (typ.)
  - —IDT71321/421LA
    - Active: 325mW (typ.)
    - Standby: 1mW (typ.)
- Two $\overline{INT}$ flags for port-to-port communications
- MASTER IDT71321 easily expands data bus width to 16-or-more-bits using SLAVE IDT71421
- On-chip port arbitration logic (IDT71321 only)
- $\overline{BUSY}$ output flag on IDT71321; $\overline{BUSY}$ input on IDT71421
- Fully asynchronous operation from either port
- Battery backup operation -2V data retention
- TTL-compatible, single 5V ±10% power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

The IDT71321/IDT71421 are high-speed 2K x 8 dual-port static RAMs with internal interrupt logic for interprocessor communications. The IDT71321 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT71421 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full speed, error-free operation without the need for additional discrete logic.

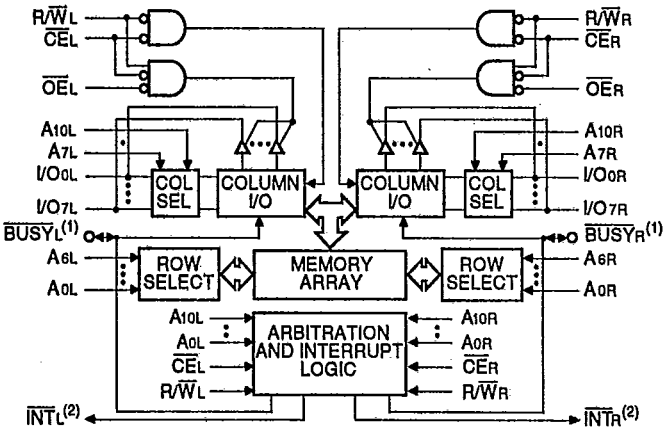
Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 20ns. Low-power (LA) versions offer battery backup data retention capability, with each dual-port typically consuming 200µW from a 2V battery.

The IDT71321/IDT71421 devices are packaged in 52-pin LCCs and PLCCs. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

6

FUNCTIONAL BLOCK DIAGRAM



2691 drw 01

NOTES:
1. IDT71321 (MASTER): $\overline{BUSY}$ is open output and requires pullup resistor. IDT71421 (SLAVE): $\overline{BUSY}$ is input.
2. Open drain output: requires pullup resistor.

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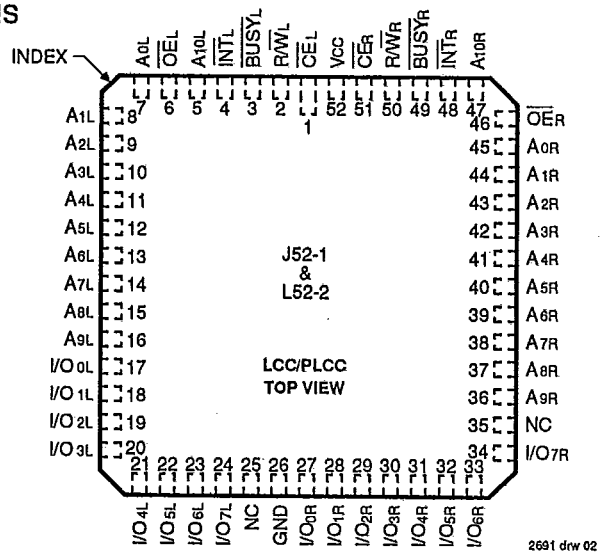
PIN CONFIGURATIONS

T-46-23-12



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2691 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed VCC + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2691 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0(2)	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

2691 tbl 03

NOTE:
1. VIL (min.) = -3.0V for pulse width less than 20ns.
2. VTERM must not exceed Vcc + 0.5V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT71321SA IDT71421SA Min.	IDT71321SA IDT71421SA Max.	IDT71321LA IDT71421LA Min.	IDT71321LA IDT71421LA Max.	Unit
|ILI|	Input Leakage Current(1)	Vcc = 5.5V, VIN = 0V to Vcc	—	10	—	5	µA
|ILO|	Output Leakage Current	$\overline{CE}$ = VIH, VOUT = 0V to Vcc	—	10	—	5	µA
VOL	Output Low Voltage (I/O0-I/O7)	IOL = 4mA	—	0.4	—	0.4	V
VOL	Open Drain Output Low Voltage ($\overline{BUSY}$/$\overline{INT}$)	IOL = 16mA	—	0.5	—	0.5	V
VOH	Output High Voltage	IOH = -4mA	2.4	—	2.4	—	V

1. At Vcc≤2.0V input leakages are undefined.

2691 tbl 04

T-46-23-12

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1, 6] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version		71321x20[2] 71421x20[2] Typ.	71321x20[2] 71421x20[2] Max.	71321x25/30 71421x25/30 Typ.	71321x25/30 71421x25/30 Max.	71321x35 71421x35 Typ.	71321x35 71421x35 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	Mil.	SA	—	—	125/125	300/295	125	290	mA
				LA	—	—	125/125	240/235	125	230	
			Com'l.	SA	125	265	125/125	260/255	75	195	
				LA	125	215	125/125	210/205	75	155	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}[4]	Mil.	SA	—	—	30/30	80/80	30	80	mA
				LA	—	—	30/30	60/60	30	60	
			Com'l.	SA	30	65	30/30	65/65	25	65	
				LA	30	45	30/30	45/45	25	45	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	—	—	80/80	195/190	80	185	mA
				LA	—	—	80/80	160/155	80	150	
			Com'l.	SA	80	180	80/80	175/170	40	130	
				LA	80	145	80/80	140/135	40	95	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, f = 0[5]	Mil.	SA	—	—	1.0/1.0	30/30	1.0	30	mA
				LA	—	—	0.2/0.2	10/10	0.2	10	
			Com'l.	SA	1.0	15	1.0/1.0	15/15	1.0	15	
				LA	0.2	5	0.2/0.2	5/5	0.2	4.0	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	—	—	70/70	185/180	70	175	mA
				LA	—	—	70/70	150/145	70	140	
			Com'l.	SA	70	175	70/70	170/165	40	115	
				LA	70	140	70/70	135/130	35	90	

2691 tbl 05

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1, 6] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version		71321x45 71421x45 Typ.	71321x45 71421x45 Max.	71321x55 71421x55 Typ.	71321x55 71421x55 Max.	71321x70[3] 71421x70[3] Typ.	71321x70[3] 71421x70[3] Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	Mil.	SA	75	230	65	230	65	225	mA
				LA	75	185	65	185	65	180	
			Com'l.	SA	75	190	65	180	—	—	
				LA	75	145	65	140	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}[4]	Mil.	SA	25	65	25	65	25	65	mA
				LA	25	55	25	55	25	55	
			Com'l.	SA	25	65	25	65	—	—	
				LA	25	45	25	45	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	40	135	40	135	40	135	mA
				LA	40	110	40	110	40	110	
			Com'l.	SA	40	120	40	115	—	—	
				LA	40	85	40	85	—	—	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, f = 0[5]	Mil.	SA	1.0	30	1.0	30	1.0	30	mA
				LA	0.2	10	0.2	10	0.2	10	
			Com'l.	SA	1.0	15	1.0	15	—	—	
				LA	0.2	4.0	0.2	4.0	—	—	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	40	125	40	120	40	110	mA
				LA	35	95	35	90	35	80	
			Com'l.	SA	40	115	40	100	—	—	
				LA	35	80	35	75	—	—	

2691 tbl 06

NOTES:
1. "x" in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency of read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. V_{CC} = 5V, T_A = +25°C for Typ.

T-46-23-12

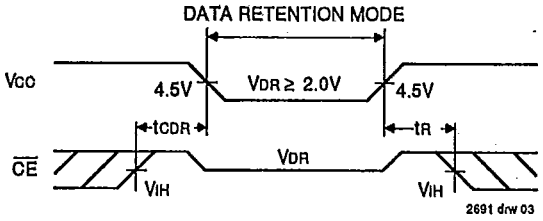
DATA RETENTION CHARACTERISTICS (LA Version Only)

Symbol	Parameter	Test Condition		IDT71321LA/IDT71421LA Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$		2.0	—	0	V
I_{CCDR}	Data Retention Current		MIL.	—	100	4000	µA
			COM'L.	—	100	1500	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

2691 tbl 07

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



2691 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, and 3

2691 tbl 08

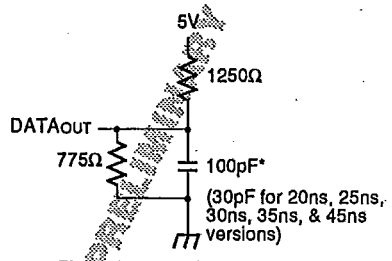


Figure 1. Output Load

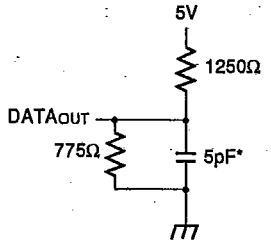


Figure 2. Output Load
(for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

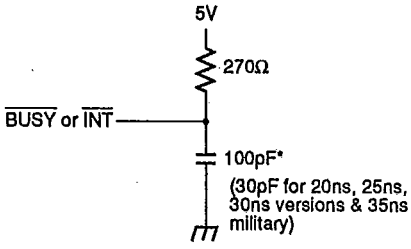


Figure 3. $\overline{BUSY}$ and $\overline{INT}$ Output Load

* Including scope and jig.

2691 drw 04

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[5]

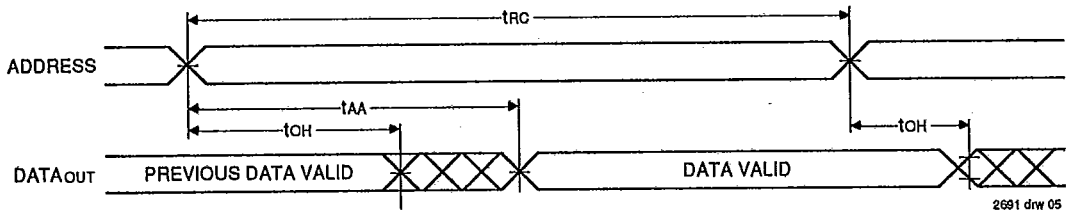
T-46-23-12

Symbol	Parameter	71321x20 (2) 71421x20 (2) Min.	Max.	71321x25/30 71421x25/30 Min.	Max.	71321x35 71421x35 Min.	Max.	71321x45 71421x45 Min.	Max.	71321x55 71421x55 Min.	Max.	71321x70(3) 71421x70(3) Min.	Max.	Unit
Read Cycle														
tRC	Read Cycle Time	20	—	25/30	—	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	20	—	25/30	—	35	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time	—	20	—	25/30	—	35	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	10	—	12/15	—	25	—	30	—	35	—	40	ns
tOH	Output Hold From Address Change	0	—	0/0	—	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time[1,4]	0	—	0/0	—	5	—	5	—	5	—	5	—	ns
tHZ	Output High Z Time[1,4]	—	8	—	10/12	—	15	—	20	—	30	—	35	ns
tPU	Chip Enable to Power Up Time[4]	0	—	0/0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[4]	—	50	—	50/50	—	50	—	50	—	50	—	50	ns

2691 tbl 09

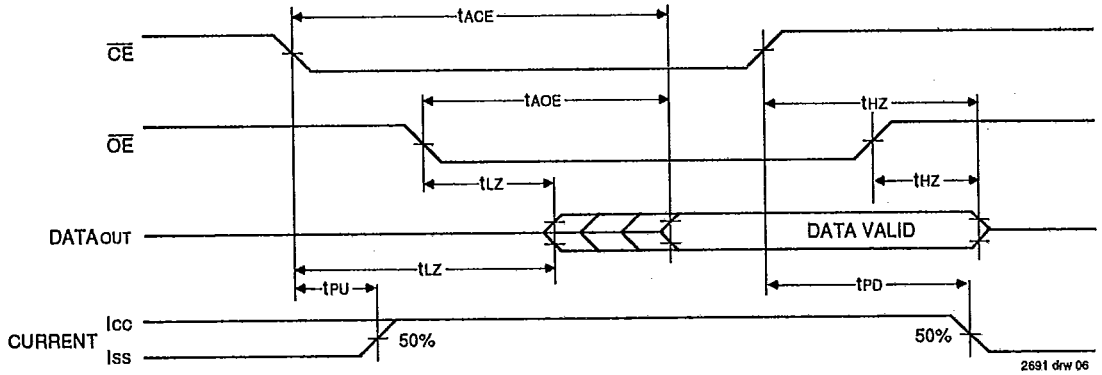
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2, and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. "X" in part numbers indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE [1,2,4]



2691 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE [1,3]



2691 drw 06

NOTES:
1. R/W is high for Read Cycles.
2. Device is continuously enabled, CE = VIL.
3. Addresses valid prior to or coincident with CE transition low.
4. OE = VIL.

T-46-23-12

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[7]

Symbol	Parameter	71321x20 [2] 71421x20 [2] Min.	Max.	71321x25/30 71421x25/30 Min.	Max.	71321x35 71421x35 Min.	Max.	Unit
Write Cycle								
tWC	Write Cycle Time[5]	20	—	25/30	—	35	—	ns
tEW	Chip Enable to End of Write	15	—	20/25	—	30	—	ns
tAW	Address Valid to End of Write	15	—	20/25	—	30	—	ns
tAS	Address Set-up Time	0	—	0/0	—	0	—	ns
tWP	Write Pulse Width[6]	15	—	20/25	—	30	—	ns
tWR	Write Recovery Time	0	—	0/0	—	0	—	ns
tDW	Data Valid to End of Write	10	—	12/15	—	20	—	ns
tHZ	Output High Z Time[1,4]	—	8	—	10/12	—	15	ns
tDH	Data Hold Time	0	—	0/0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1,4]	—	8	—	10/12	—	15	ns
tOW	Output Active From End of Write[1,4]	0	—	0/0	—	0	—	ns

2691 tbl 10

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[7] (CONTINUED)

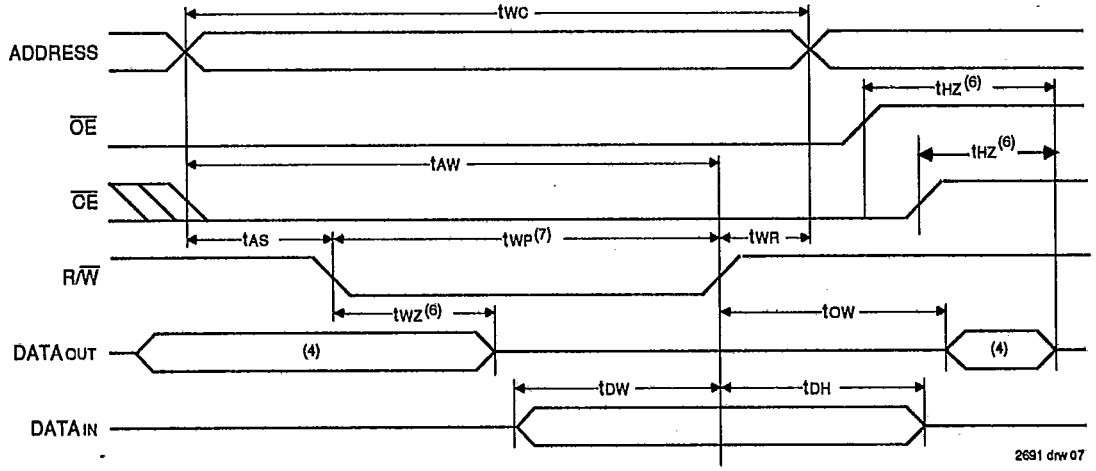
Symbol	Parameter	71321x45 71421x45 Min.	Max.	71321x55 71421x55 Min.	Max.	71321x70[3] 71421x70[3] Min.	Max.	Unit
Write Cycle								
tWC	Write Cycle Time[5]	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write	35	—	40	—	50	—	ns
tAW	Address Valid to End of Write	35	—	40	—	50	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width[6]	35	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	20	—	20	—	30	—	ns
tHZ	Output High Z Time[1,4]	—	20	—	30	—	35	ns
tDH	Data Hold Time	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1,4]	—	20	—	30	—	35	ns
tOW	Output Active From End of Write[1,4]	0	—	0	—	0	—	ns

2691 tbl 11

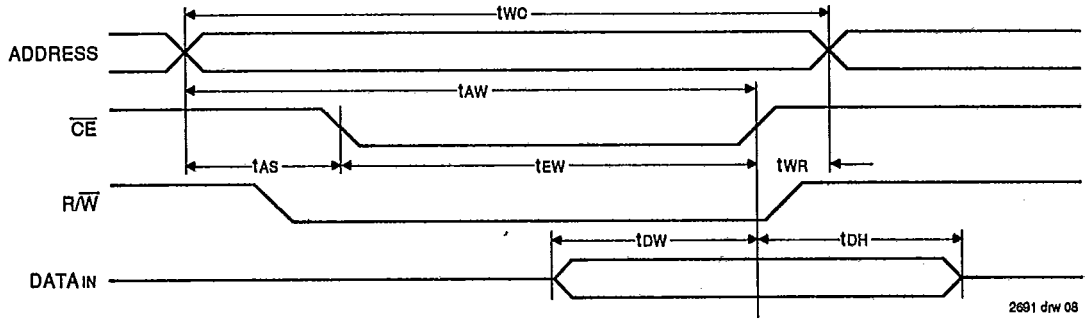
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2, and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, twc = tBAA + twP.
6. Specified for $\overline{OE}$ at high (Refer to "Timing Waveform of Write Cycle", Note 7).
7. "x" in part numbers indicates power rating (SA or LA).

T-46-23-12

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING (1,2,3,7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING (1,2,3,5)



NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

T-46-23-12

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[8]

Symbol	Parameter	71321x20 (1) 71421x20 (1) Min.	Max.	71321x25/30 71421x25/30 Min.	Max.	71321x35 71421x35 Min.	Max.	Unit
Busy Timing (For Master IDT71321 Only)								
tBAA	BUSY Access Time to Address	—	20	—	25/30	—	35	ns
tBDA	BUSY Disable Time to Address	—	20	—	20/25	—	30	ns
tBAC	BUSY Access Time to Chip Enable	—	20	—	20/25	—	30	ns
tBDC	BUSY Disable Time to Chip Enable	—	20	—	20/25	—	25	ns
tWDD	Write Pulse to Data Delay[3]	—	50	—	50/50	—	60	ns
tDDD	Write Data Valid to Read Data Delay[3]	—	35	—	35/35	—	35	ns
tAPS	Arbitration Priority Set-up Time[4]	5	—	5/5	—	5	—	ns
tBDD	BUSY Disable to Valid Data[5]	—	Note 5	—	Note 5	—	Note 5	ns
Busy Timing (For Slave IDT71421 Only)								
tWB	Write to BUSY Input[6]	0	—	0/0	—	0	—	ns
tWH	Write Hold After BUSY[7]	12	—	15/20	—	20	—	ns
tWDD	Write Pulse to Data Delay[9]	—	50	—	50/50	—	60	ns
tDDD	Write Data Valid to Read Data Delay[9]	—	35	—	35/35	—	35	ns

2691 tbl 12

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[8] (CONTINUED)

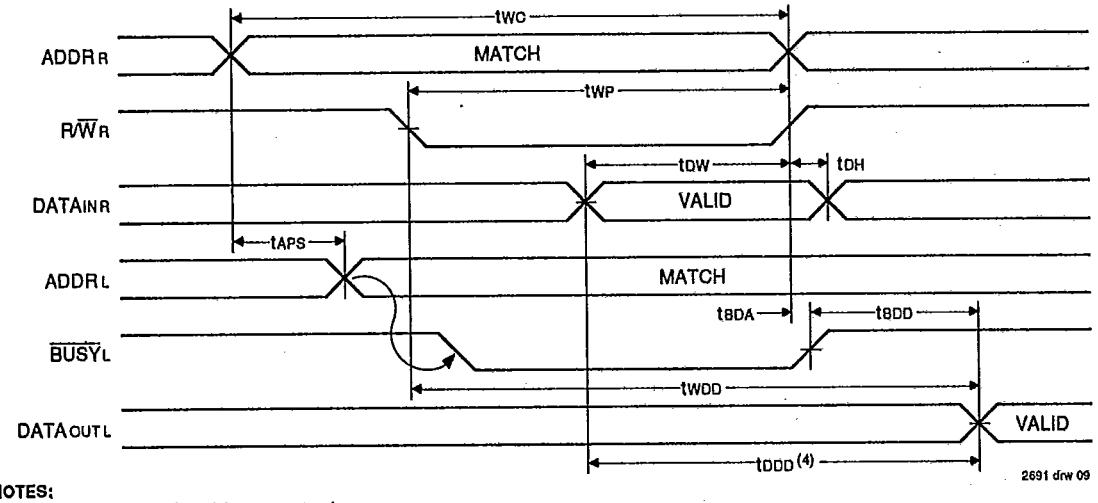
Symbol	Parameter	71321x45 71421x45 Min.	Max.	71321x55 71421x55 Min.	Max.	71321x70[2] 71421x70[2] Min.	Max.	Unit
Busy Timing (For Master IDT71321 Only)								
tBAA	BUSY Access Time to Address	—	35	—	45	—	45	ns
tBDA	BUSY Disable Time to Address	—	35	—	40	—	40	ns
tBAC	BUSY Access Time to Chip Enable	—	30	—	35	—	35	ns
tBDC	BUSY Disable Time to Chip Enable	—	25	—	30	—	30	ns
tWDD	Write Pulse to Data Delay[3]	—	70	—	80	—	90	ns
tDDD	Write Data Valid to Read Data Delay[3]	—	45	—	55	—	70	ns
tAPS	Arbitration Priority Set-up Time[4]	5	—	5	—	5	—	ns
tBDD	BUSY Disable to Valid Data[5]	—	Note 5	—	Note 5	—	Note 5	ns
Busy Timing (For Slave IDT71421 Only)								
tWB	Write to BUSY Input[6]	0	—	0	—	0	—	ns
tWH	Write Hold After BUSY[7]	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay[9]	—	70	—	80	—	90	ns
tDDD	Write Data Valid to Read Data Delay[9]	—	45	—	55	—	70	ns

2691 tbl 13

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Port-to-port delay through RAM cells from writing port to reading port. refer to "Timing Waveform of Read With BUSY (For Master IDT71321 only)".
4. To ensure that the earlier of the two ports wins.
5. tBDD is a calculated parameter and is the greater of 0, tWDD-tWP (actual) or tDDD - tDW (actual).
6. To ensure that the write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (SA or LA).
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With Port-to-Port Delay (For Slave IDT71421 Only)".

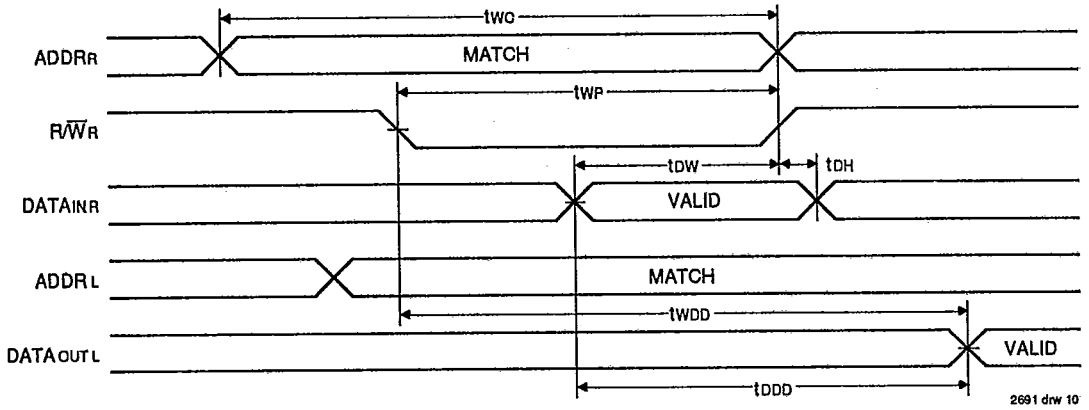
T-46-23-12

TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ (1,2,3) (FOR MASTER IDT71321)



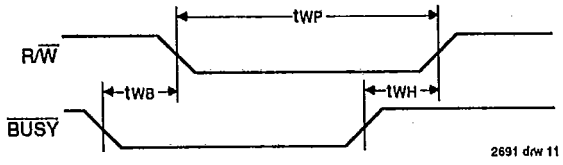
NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ at LO for the reading port.

TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (1,2,3) (FOR SLAVE IDT71421 ONLY)



NOTES:
1. Assume $\overline{BUSY}$ input at HI for the writing port, and $\overline{OE}$ at LO for the reading port.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.

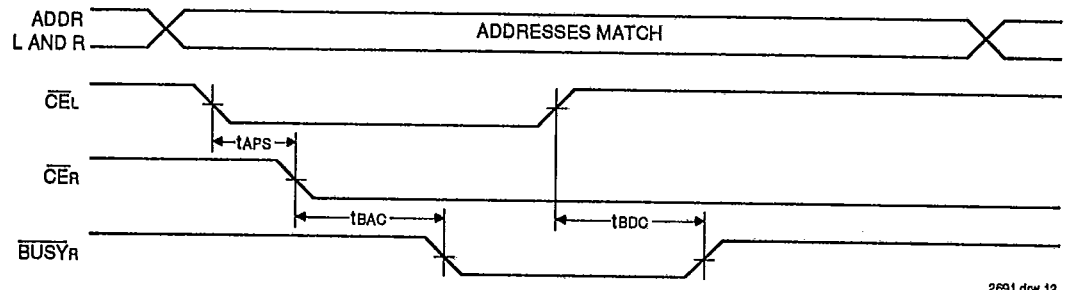
TIMING WAVEFORM OF WRITE WITH BUSY (FOR SLAVE IDT71421)



TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION (FOR MASTER IDT71321 ONLY)

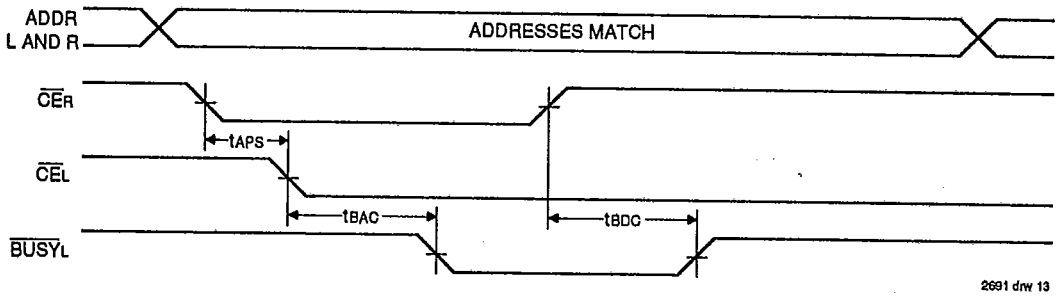
T-46-23-12

$\overline{CE}_L$ VALID FIRST:



2691 drw 12

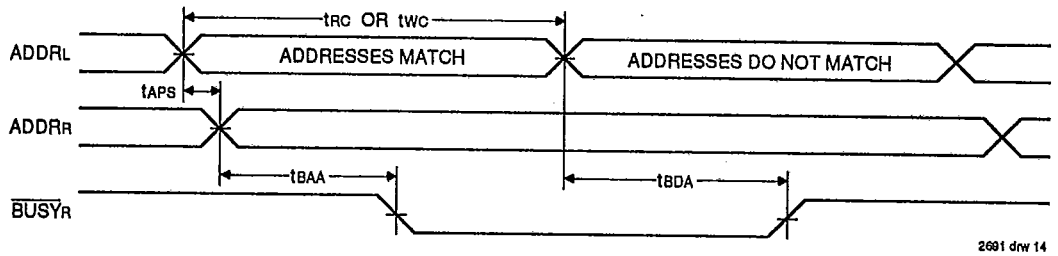
$\overline{CE}_R$ VALID FIRST:



2691 drw 13

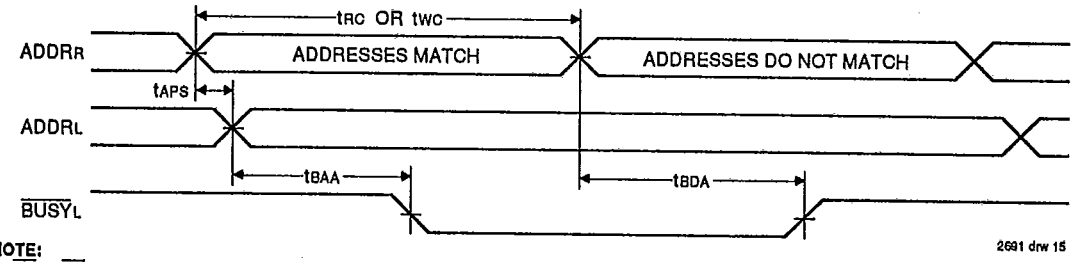
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION (FOR MASTER IDT71321 ONLY)(1)

LEFT ADDRESS VALID FIRST:



2691 drw 14

RIGHT ADDRESS VALID FIRST:



2691 drw 15

NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

T-46-23-12

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

Symbol	Parameter	71321SA/LA20(1) 71421SA/LA20(1) Min.	Max.	71321SA/LA25/30 71421SA/LA25/30 Min.	Max.	71321SA/LA35 71421SA/LA35 Min.	Max.	Unit
Interrupt Timing								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	20	—	25/30	—	35	ns
tINR	Interrupt Reset Time	—	20	—	25/30	—	35	ns

2691 tbl 14

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (CONTINUED)

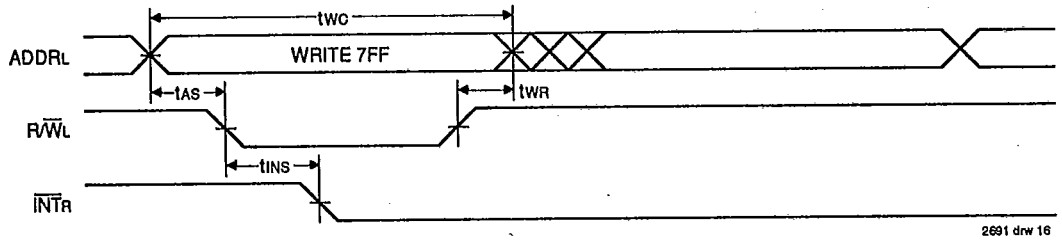
Symbol	Parameter	71321SA/LA45 71421SA/LA45 Min.	Max.	71321SA/LA55 71421SA/LA55 Min.	Max.	71321SA/LA70(2) 71421SA/LA70(2) Min.	Max.	Unit
Interrupt Timing								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	40	—	45	—	50	ns
tINR	Interrupt Reset Time	—	40	—	45	—	50	ns

2691 tbl 15

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.

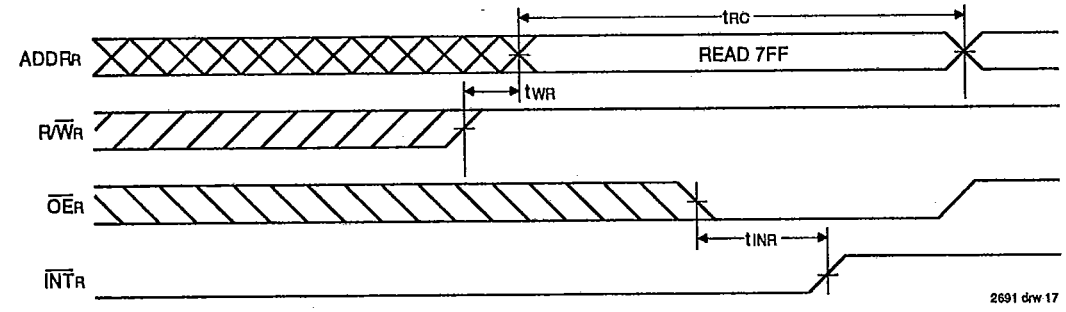
TIMING WAVEFORM OF INTERRUPT MODE (1, 2)

LEFT SIDE SETS $\overline{INT}_R$:



2691 drw 16

RIGHT SIDE CLEARS $\overline{INT}_R$:



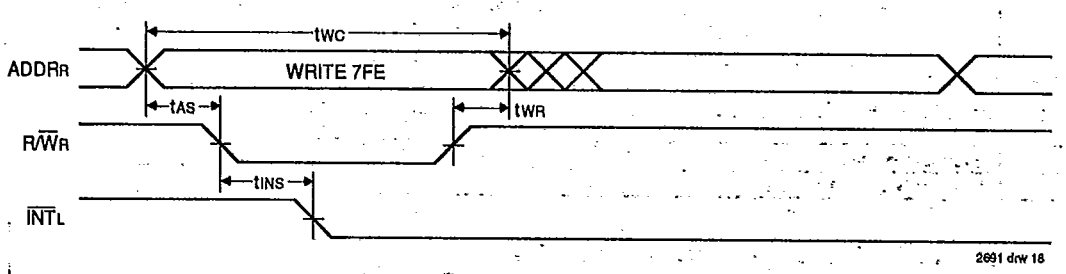
2691 drw 17

NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_L$ and $\overline{INT}_R$ are reset (HIGH) during power up.

TIMING WAVEFORM OF INTERRUPT MODE (1, 2)

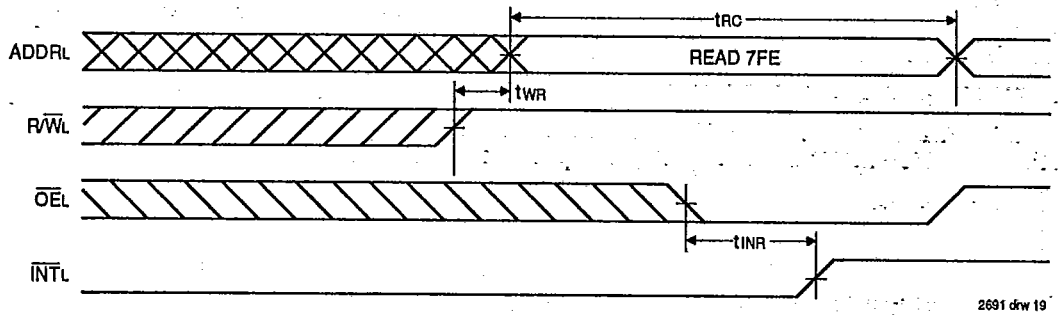
T-46-23-12

RIGHT SIDE SETS $\overline{INT}_L$:



2691 drw 18

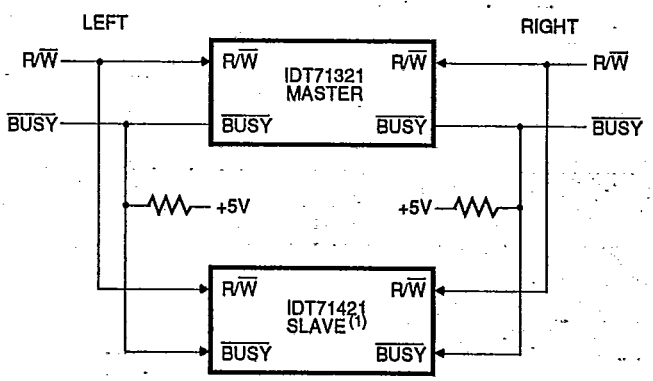
LEFT SIDE CLEARS $\overline{INT}_L$:



2691 drw 19

NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_R$ and $\overline{INT}_L$ are reset (HIGH) during power up.

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



2691 drw 20

NOTE:
1. No arbitration in IDT71421 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT71421 (SLAVE).

FUNCTIONAL DESCRIPTION

The IDT71321/IDT71421 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any locations in memory. These devices have an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table 1.

The interrupt flag ($\overline{INT}$) permits communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$)is set when the right port writes to memory location 7FE (HEX). The left port clears the interrupt by reading address location 7FE. Likewise, the right port interrupt flag (INT_R) is set when the left port writes to memory location 7FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 7FF. The message (8 bits) at 7FE or 7FF is user-defined. If the interrupt function is not used, address locations 7FE and 7FF are not used as mail boxes but as part of the random access memory. Refer to Table II for the interrupt operation.

ARBITRATION LOGIC FUNCTIONAL DESCRIPTION

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table III). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

T-46-23-12

DATA BUS WIDTH EXPANSION MASTER/SLAVE DESCRIPTION

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another acitivates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMS in width, the writing of the SLAVE RAMs must be delayed, until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

6

TRUTH TABLES

T-46-23-12

TABLE I – NON-CONTENTION READ/WRITE CONTROL(4)

Left Or Right Port(1)				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	Function
X	H	X	Z	Port Disabled and in Power Down Mode I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R$ = $\overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on Port Written into Memory(2)
H	L	L	DATAOUT	Data in Memory Output on Port(3)
H	L	H	Z	High Impedance Outputs

2691 tbl 16

NOTES:
1. A_{0L}-$A_{10L} \neq A_{0R}$-A_{10R}
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter (1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{IN} = 0V	11	pF

2691 tbl 17

NOTE:
1. This parameter is determined by device characterization but is not 100% tested.

TABLE II – INTERRUPT FLAG(1, 4)

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{10L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0L}-A_{10R}	$\overline{INT}_R$	Function
L	L	X	7FF	X	X	X	X	X	L(2)	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	7FF	H(3)	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L(3)	L	L	X	7FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	7FE	H(2)	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

2691 tbl 18

NOTES:
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then NC.
3. If $\overline{BUSY}_R$ = L, then NC.
4. H = HIGH, L = LOW, X = DON'T CARE, NC = NO CHANGE.

TABLE III – ARBITRATION(1, 2)

Left Port		Right Port		Flags		
$\overline{CE}_L$	A_{0L}-A_{10L}	$\overline{CE}_R$	A_{0R}-A_{10R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Function
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R}$-A_{10R}	L	$\neq A_{0L}$-A_{10L}	H	H	No Contention
Address Arbitration With $\overline{CE}$ Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ Arbitration With Address Match Before $\overline{CE}$						
LL5R	= A_{0R}-A_{10R}	LL5R	= A_{0L}-A_{10L}	H	L	L-Port Wins
RL5L	= A_{0R}-A_{10R}	RL5L	= A_{0L}-A_{10L}	L	H	R-Port Wins
LW5R	= A_{0R}-A_{10R}	LW5R	= A_{0L}-A_{10L}	H	L	Arbitration Resolved
LW5R	= A_{0R}-A_{10R}	LW5R	= A_{0L}-A_{10L}	L	H	Arbitration Resolved

2691 tbl 19

NOTES:
1. $\overline{INT}$ Flags Don't Care.
2. X = DON'T CARE, L = LOW, H = HIGH
   LV5R = Left Address Valid ≥ 5ns before right address.
   RV5L = Right Address Valid ≥ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$.
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other.