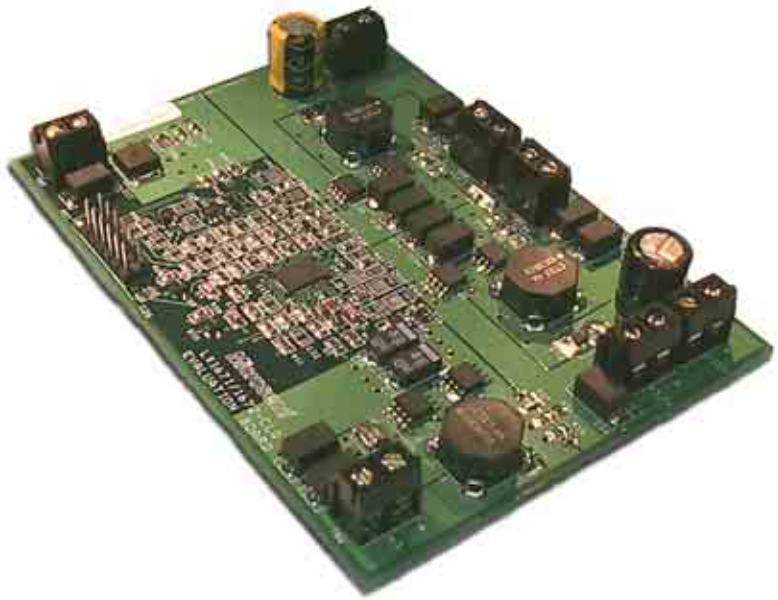
LX1671/LX1672 CLQ (MLPQ PACKAGE) MULTIPLE OUTPUT LOADSHARE™ PWM EVALUATION BOARD

USERS GUIDE



Microsemi
INTEGRATED PRODUCTS

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OVERVIEW

The LX1671 evaluation board is designed to allow the user to get a detailed understanding of the operation of the LX1671 or LX1672 and to allow evaluation of several configurations that demonstrate the full capabilities of the controller. All three Pulse Width Modulator (PWM) phases and the Linear Regulator (LDO) can be completely evaluated. The LX1672 is a two phase version of the LX1671

Due to the flexibility of the LX1671 evaluation board a number of components must be selected for the specific mode of operation desired and to establish several variable parameters. The evaluation board is delivered with all required factory-installed components in a fully functional configuration.

The LX1671 evaluation board can be delivered in a number of standard configurations. User changes to the standard board can be made for different applications and custom versions may be supplied in some situations. When the MLPQ package is used the LX1671 and the LX1672 have the same pinout so the circuit board can be used for either part.

This document is intended to be used in conjunction with the LX1671 data sheet and LX1671 Product Design Guide (or LX1672 if applicable).

LX1671 PWM TOPOLOGY

The LX1671 is a PWM controller offering a high level of integration. Three separate synchronous, voltage mode PWM controllers are integrated into a single package. Phases 1 and 2 can be used in a Bi-Phase mode with LoadSHARE™ or used as two separate single-phase controllers. Phase 3 is always used in single phase. The single-phase buck regulators are limited to approximately 15 Amps maximum output by the available gate drive; the ability to operate in Bi-Phase allows output currents of 30 Amps by paralleling the output capabilities of two controller phases. There is also a controller for a linear regulator that utilizes an external pass transistor with a maximum output of approximately 5A.

LX1671 FEATURES

- Three synchronous PWM controllers
- One LDO controller
- Two PWM controllers can be operated in Bi-Phase to double the current output capability.·
- In Bi-Phase the two PWMs operate 180 degrees out of phase to reduce input and output ripple current.
- Each PWM controller can operate from a different input voltage when in single or Bi-Phase.
- When in Bi-Phase the currents supplied by each phase can be unbalanced with the LoadSHARE™ topology.
- 300 KHz PWM Switching frequency.
- Hiccup current limiting in all PWM outputs.
- Reference allows low output voltages down to 0.8 volts.·
- No current sense resistors; $R_{DS(ON)}$ is used for current limit and hiccup mode.
- Soft start on each PWM and Under Voltage Lockout on VCC and upper FET drivers·
- Output voltage power-up sequencing by selecting soft-start capacitor value.
- Reference input on Phase 2 for forced current sharing or DDR memory data bus termination.

EVALUATION BOARD FEATURES·

- The heat sinking on the LX1671/72 evaluation board allows up to 8A out for each PWM phase. Note: The controller is capable of 15A out on all PWM phases but component selection and thermal limits on the evaluation board will prevent operating at full current.
- Linear Regulator with pass transistor, limited to five watts power dissipation.
- Provisions are made for different input voltages of 3.3, 5 , and 12 volts to be used as input power for each of the three phases. Bootstrap diodes and capacitors can be installed depending on the input voltage selected.
- Three terminal blocks are provided to allow connection of input 3.3, 5, and 12 volt power.
- Four terminal blocks are provided for connecting loads to the outputs.
- A connector with jumpers allows enabling each PWM and the linear regulator independently.

LOADSHARE (BI-PHASE) OPERATION

For LoadSHARE operation it is necessary to use phases 1 and 2 because of the different configuration of the phase 2 error amplifier input. The phase 2 error amplifier does not internally connect to the reference like the other two phases but is brought out to the (RF2) pin to allow a filtered feedback from phase 1 to be brought into the error amplifier. Phase 1 determines the output voltage and forces phase 2 to follow. When using

LoadSHARE the input power drawn by phase 1 and 2 can be different to proportion the available power. Phase 3 and the LDO operate independently and their output voltages can be set as desired. Jumpers are installed on J1 to disable each regulator independently.

CONFIGURATION

The LX1671 evaluation board is available in several standard configurations or it can be customized for specific applications.

Note: For the purpose of this document one of the standard configurations (LX1671 EVAL -010) has been chosen to describe the evaluation board features and operation, all wording relates to this specific version. The standard board is designed for the MLPQ package. The LX1672 in the MLPQ package has the same pinout so that the same circuit board can be used with either part.

This configuration has three output voltages with phases 1 and 2 operating in LoadSHARE; phase 3 and the LDO each have their own outputs.

The LoadSHARE configuration used is the ESR method where the current sharing ratio is determined by the ESR of the output inductors. Since both inductors are the same part number the current sharing ratio is 50% for each phase.

The Schematic (Fig 7) and Bill of Material (Fig 8) are for the -010 version which is configured as shown in Table 1 below.

Each evaluation board will have a Schematic and Bill of Material documenting that specific configuration.

Vout Phase 1 & 2	1.5 Volts		
Vout Phase 3	2.5 Volts		
Vout LDO	2.5 Volts		
Vin Phase 1	5 Volts	Phase 1 (VC1)	+12 Volts
Vin Phase 2	3.3 Volts	Phase 2 (VC2)	+12 Volts
Vin Phase 3	12 Volts	Phase 3 (VC3)	Bootstrap
Vin LDO	3.3 Volts		
Phase 3	Single Phase		
Phase 1 & 2	LoadSHARE (Bi-Phase)		
VCCL	5 Volts		

Table 1 LX1671–010 Eval Board Configuration

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INITIAL SETUP

Before applying any input power to the circuit board several choices must be made and the proper components must be chosen to allow operation with the desired characteristics. Note: The factory configuration is fully functional and can be changed if desired. Prior to changing the factory configuration, the following criteria should be considered:

- Single Phase or LoadSHARE operation for Phase 1 and 2.
- Input voltages for each of the three PWM regulators.
- Will bootstrap be required, based on input voltages.
- Output voltages for all four outputs.
- Output current limit for PWM outputs.
- Power up sequencing for output voltages.

Once the above are known the proper components and jumpers must be installed for the following:

- Feedback and low pass filters for phase 1 and 2 PWM regulators if LoadSHARE operation is selected.
- Output voltage for Phase 2 if single phase operation is used.
- Output voltage for Phase 1 and 3 if different from preset values.
- Output voltage for the LDO if different from preset value
- Bootstrap configuration if required.
- Current Limit for the PWM (if other than the preset value).
- Soft start capacitors if different start up sequence is required.

When LoadSHARE operation is used low pass filtering is required on the two feedback paths from the outputs of phase 1 and 2 to the phase 2 error amplifier inputs. Typical values are shown on the evaluation board schematic, Figure (7)

CONFIGURATION OPTIONS·

Bootstrap

A bootstrap circuit will be required if the high side FET driver supply voltage (VCX) is not at least 5 volts greater than the PWM input voltage (high side FET drain voltage).

A typical configuration is to use +12 for the high side gate driver, VCX, with either 3.3 or 5 as the PWM input, this gives sufficient gate drive to enhance the upper FET. An alternative is to use the bootstrap configuration to add 5 volts to the PWM input voltage which will generally make a slight improvement in efficiency by keeping the VCX voltage as low as possible and does not require a +12 volt input. If 12 volts is selected as the PWM input then bootstrapping will be required. Each of the three PWM phases has provisions for a diode, capacitor, and several 0 ohm jumpers that allow bootstrapping each phase independently. See schematic Figure (7). Be sure that the zero ohm jumpers are configured to connect either +12 or the bootstrap voltage to the VCX pins and add the diode and capacitor for that phase. The bootstrap diodes and capacitors are CR1-C26,CR2-C2, and CR3,-C25.

Rectifier/Filter

Since the LDO gets its power from VC1 using a bootstrap configuration for phase 1 results in the error amplifier having a square wave as its supply voltage. This square wave can be rectified and filtered by adding a second diode and capacitor to obtain a filtered output. VCCL can also be powered by a bootstrap rectifier/filter configuration, options allow deriving VCCL from either phase 2 or phase 3. Additional diodes and capacitors are used to implement a rectifier/filter with a clean DC output as follows, CR4-C33 for VC1; CR5-C9 for VCCL derived from phase 3; and CR10-C9 for VCCL derived from phase 2. By optimizing drive voltages it is possible to achieve small improvements in efficiency.

Input Voltage Jumpers

There are three resistors shown in series with each high side FET for the PWMs. These are actually zero ohm jumpers that connect the desired input voltage 3.3, 5, or 12 volts to the high side FET drain. Only one of the three can be installed per phase with the others left open. Similarly the LDO has three choices that allow 3.3 volts, 5 volts, or the output of phase 3 to be used for the input.

R6 and R56

The resistors shown as R6 and R56 on the schematic are actually jumper wires due to the high currents that can flow in these paths. These are only installed for specific configurations.

Parallel Diodes

There are 3 Schottky diodes shown in parallel with the lower FETs on the PWM output stage. These diodes CR7-8- 9 may not be installed but can be used to help prevent negative spikes on the lower FET drain and will give a slight improvement in efficiency.

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LoadSHARE Methods
There are four basic methods used for LoadSHARE that are described in the LX1671 Product Design Guide. Numerous components are related to the implementation of these various methods.

LoadSHARE Filters
The low pass filters used for LoadSHARE operation are made up of R18-C22 for the FB2 input and R23-C6 for the RF2 input. Typical values are 61.9K and 4700pf.

Proportional LoadSHARE
U2 and U3 are only used if proportional LoadSHARE is desired. Several other components around U2 and U3 are also used only with proportional LoadSHARE control.

LDO Soft Start
CR6-C27-R27 can be used to ramp the LDO output up slowly if desired. The primary reason for this is to prevent a possible UVLO condition if 5 volts is used for the LDO input. If 5 volts is used for the LDO input and a sudden current demand is placed on it by the LDO load it can result in a transient on the 5 volts that will trigger the UVLO.

Frequency Compensation
Three resistors R8-13-22 set the gain of the PWM error amplifiers, these are typically 200K ohm and three capacitors C23-31-32 can be placed in parallel with the feedback resistors to lower the error amplifier bandwidth.

Bulk Capacitors
There are a number of output bulk capacitors. Phase one output C10-11; phase 2 output C12-13; phase 3 output C19-26. These are chosen to provide the required output filtering at the output voltage.

SINGLE PHASE / BI-PHASE

- LoadSHARE operation of phases 1 and 2 requires several component selections that are factory installed (if ordered for Bi-Phase operation). If single-phase operation of phase 1 and 2 is desired than modifications must be made as follows.·
- Remove R6 (jumper wire) - Connects phase 1 and 2 outputs together
- Remove R23 and C6 - Feedback filter to RF2·
- Remove C5 and replace with a jumper - Phase 2 feedback integrator capacitor
- Change R22 to 200K - Phase 2 error amplifier gain·
- Install a jumper for R26 - Connects the reference to phase 2 error amplifier positive input RF2·
- Remove R18 and C22 - Filtered feedback to FB2·
- Change R21 to 4.02K
- Phase 2 voltage feedback
- Select R17 and R20 to give the desired output voltage for phase 2

$$V_{OUT} = 0.8\left(\frac{R17 + R20}{R20}\right)$$

This equation is simplified and does not account for drop across the input resistors due to error amplifier input current. It is suggested that input resistors be kept between 1K ohm and 10K ohm to minimize error and noise coupling from surrounding circuits.

REQUIRED TEST EQUIPMENT

- Multiple channel Oscilloscope with ten to one probes having short ground leads
- Digital Multimeter
- Power source (3.3 volts) if required for PWM input (factory configuration requires +3.3)
- Power source (5 volts) with sufficient current for loads (factory configuration requires +5)
- Power Source (12 volts) if required for PWM input or VCX (factory configuration requires +12)

Resistive loads for all outputs at the required power levels for each output

OPTIONAL TEST EQUIPMENT

- Oscilloscope current probe with amplifier
- Electronic loads

EVALUATION BOARD OPERATION

Once all components have been installed power can be applied to the input terminal blocks and initial operation checked with no load. It is recommended that the power supplies used on the input have adjustable current limits that can be set to a low value for initial turn on of a new board. Apply all input voltages with current limits set below 1A and enable each output independently to verify that all outputs are functional and have the correct output voltage. Input power sequencing is not critical. Once every output has been verified for proper operation at no-load, a resistive load can be connected to each output (up to the desired output level). It is recommended that each output be loaded individually the first time to insure normal operation

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and that each FET be checked for safe operating temperature after a few moments of operation at full load. When all outputs have been checked at full output current with resistive loads there are a number of tests that can be performed to evaluate performance. For details of operation see the LX1671 Product Design Guide.

EFFICIENCY

Since efficiency is always of interest it should be measured. Variables such as input voltage and output current effect efficiency so any measurements should be made at or close to actual values. Efficiency (h) can be expressed as :

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100$$

Note: There will be voltage drops across the input terminal blocks and zero ohm jumpers that will effect efficiency measurements. The input voltage is best measured directly across the half bridge to obtain accurate results. The output voltage can be measured at the output capacitor.

LOAD REGULATION

Measure the output voltage at a fixed load and vary the load current over the range of interest. Observe the change in output voltage as a function of load current.

LINE REGULATION

Measure the output voltage and vary the input voltage over the range of interest. Observe the change in output voltage as a function of input voltage. Note: The under voltage lockout internal to the LX1671 requires greater than 4.5 volts VCC to operate and the VCC max is 6 volts. If the required input voltage range includes voltages less than 4.5 or more than 6 volts then the high side FET drain must be connected to a separate power supply to isolate it from VCC.

OVER CURRENT PROTECTION

Each output has a current protection limit that can be set to the desired maximum current by a resistor R_{SET}. Short circuit current limits can be verified either by gradually increasing the load current or by applying a shorting wire across the output. The drain of the lower FET should be monitored with an oscilloscope to insure that the over current limit is functioning properly, during the hiccup period the lower FET will be held on. With a short circuit condition the LX1671 will go into a hiccup mode where the soft start mode is repeatedly cycled to maintain safe FET currents and temperatures. The initial R_{SET} value is 1K ohm resulting in a 25A current limit, this will result in safe average FET temperatures and currents.

UVLO

The VCC and VCX pins are monitored by a under-voltage lockout circuit that will disable the PWM if either voltage is below the preset limit. The input voltages to these pin can be lowered to verify operation. All phases will shutdown if any monitored voltage goes below the threshold. The LDO is not effected by the UVLO.

DYNAMIC LOADS

In many applications it is required that the output voltage remain within specified limits for a specified step change in load current. The primary component that influences this specification is the output capacitor. A step change in output current will result in an instantaneous drop in output voltage that is the product of the output capacitor ESR and the magnitude of the current step. A current step can be applied using either a dynamic load or an external FET switch with an appropriate drain resistor to give the desired current change. A function generator can be used to supply the FET gate drive. The rise time of the current step can be controlled by adding resistance in series with the FET gate to slow down the switching time.

OSCILLOSCOPE WAVEFORMS

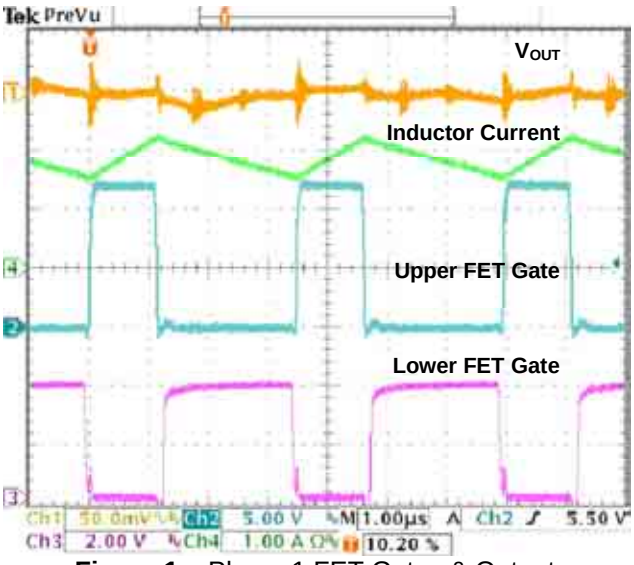

Figure 1 – Phase 1 FET Gates & Output

Upper and lower gate waveforms along with inductor current and output voltage. Note that the duty cycle is 30% corresponding to a 5 volt input with a 1.5 volt output.

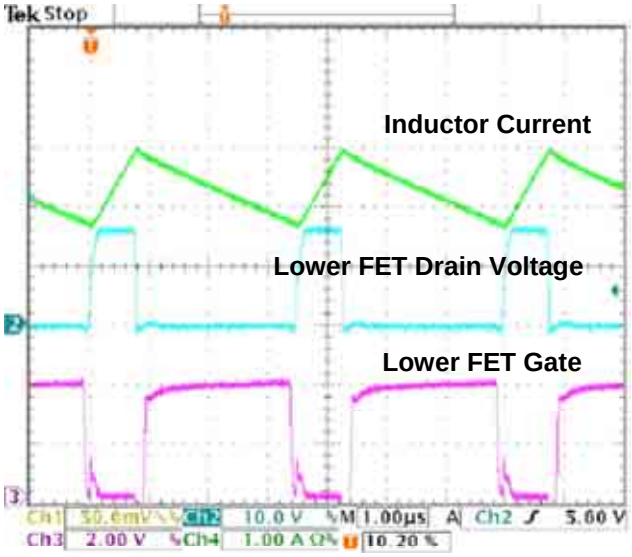

Figure 2 – Phase 2 FET Gates & Output

Lower FET gate drive against its drain voltage and inductor current. Note that the inductor current ramps up when the lower FET is off (upper FET on) and then ramps down when the lower FET is on. The difference in width between the low gate drive and high drain voltage is the non-overlap period where both FETs are off.

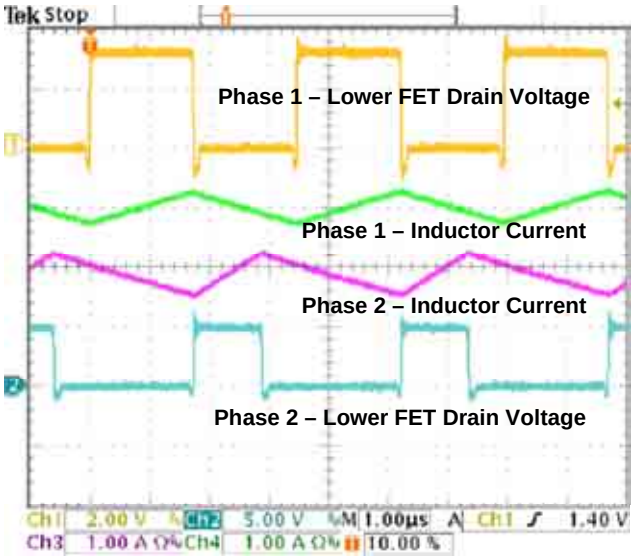

Figure 3 – Phase 1 versus Phase 2 Bi-Phase

Waveforms of the phase node voltage and inductor currents of phase 1 and 2 operating in Bi-Phase. The drain voltage waveforms show the 180 degree out-of-phase operation of the two PWM controllers. The difference in duty cycle is due to phase 1 having a 5 volt input and phase 2 having a 3.3 volt input. If both input voltages were the same the inductor currents would also be 180 degrees out of phase. Note the non-overlap period where both FETs are off and the drain voltage is slightly below ground. This is caused by the FET body diode conducting due to inductor current flow from ground up to the phase node. When the FET actually turns on the drop is reduced due to the low RDS(on) in parallel with the body diode

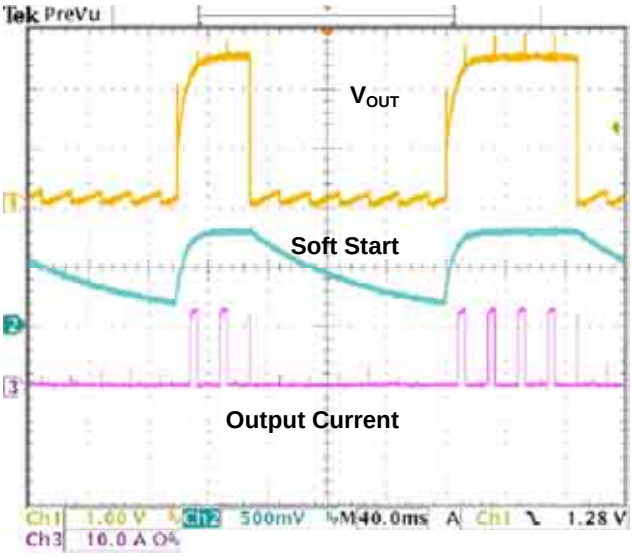

Figure 4 – Soft Start and Hiccup Mode

An external switch is periodically connecting a load resistor across the output terminals. The load resistor is low enough to result in current pulses that exceed the current limit threshold determined by the RSET resistor. During the soft start interval the output voltage ramps up to the correct value while the current limit circuit limits the peak value of the current pulses. At the end of the soft start interval the next load pulse triggers the hiccup sequence causing the output voltage to go to zero until the end of the hiccup interval when the soft start ramp begins again. This sequence will repeat indefinitely keeping average FET temperatures within acceptable limits.

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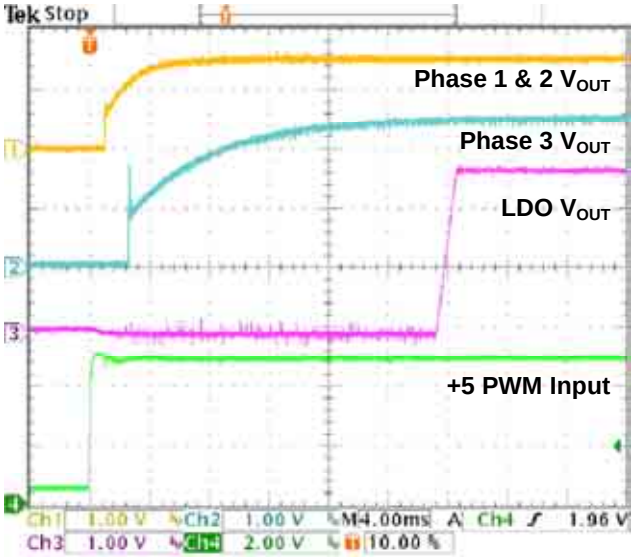

Figure 5 – Start-Up Sequence

Start-up sequence of phase 1 and 2 in Bi-Phase versus phase 3 and the LDO when the +5 input is switched on.

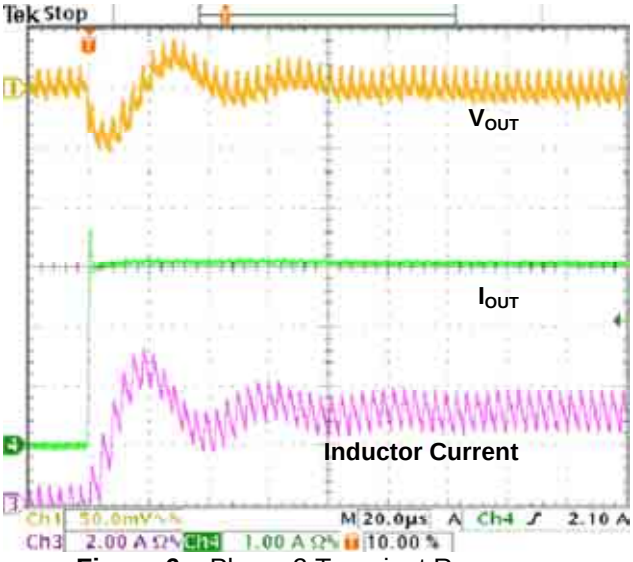

Figure 6 – Phase 2 Transient Response

Output voltage and inductor current of phase 3 when a 3 amp current step is applied to the output.

SCHEMATIC

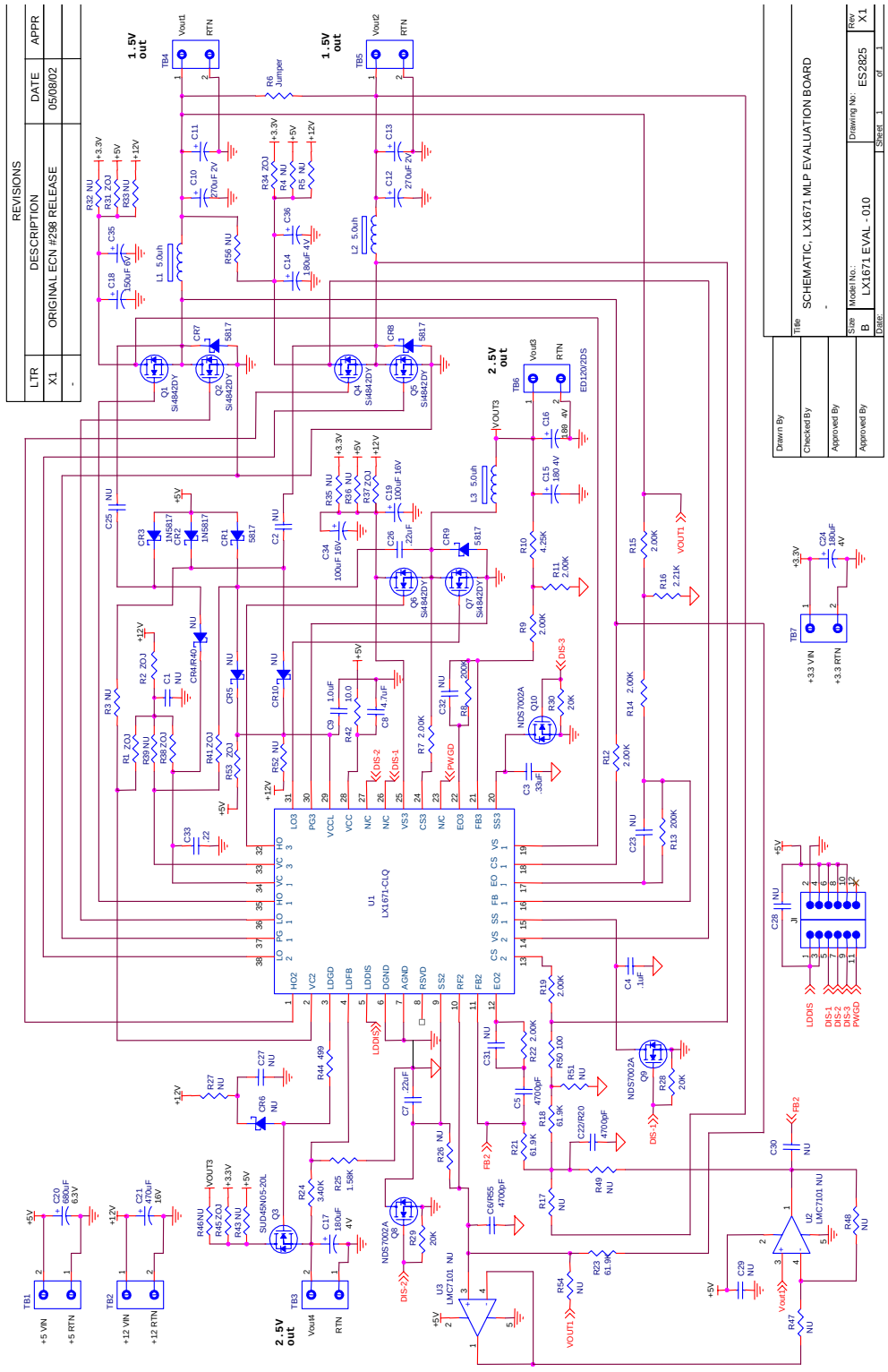

Figure 7 – LX1671 EVAL –010 Schematic

BILL OF MATERIALS LX1671 EVAL -010

MISCELLANEOUS COMPONENTS

Line Item	Part Description	Manufacturer & Part #	Case	Reference Designators	Qty
1	Int. Ckt, Multi-Phase PWM	MICROSEMI LX1671CLQ	MLPQ	U1	1
2	FAB, PWB, Eval Board X1	MICROSEMI SGE2825X1			1
3	Diode, Schottky, 1A 20V	MICROSEMI UPS5817	PWRMITE	CR1,CR7, CR8,CR9	4
4	Inductor, Power, 5µH, 6.5A	COOPER CTX5-4A	SMD	L1-L3	3
5	Trans, N-Channel, 30V, 6mΩ, 19A, 35nC Max	VISHAY SI4842DY	SO-8	Q1, Q2, Q4-Q7	6
6	Trans, N-Channel, 30V, 18mΩ, 50A	VISHAY SUD45N05-20L	TO-252	Q3	1
7	Trans, N-Channel, 60V, 2Ω	FAIRCHILD NDS7002A	SOT-23	Q8, Q9, Q10	3
8	Terminal Block, 2Pin	SGE2442-2		TB1-B7	7
9	Header, 12Pin, 2x6 Dual Row			J1	1

CAPACITORS

Line Item	Part Description	Manufacturer & Part #	Case	Reference Designators	Qty
1	4.7µF, 16V, Ceramic	Taiyo Yuden EMK316BJ475ML	1206	C8	1
2	0.1µF, 25V, ±10%	ROHM MCH182CN104KK	0805	C4, C26, C33	3
3	0.22µF, 25V, ±10%	ROHM MCH182CN224KK	0805	C2,C7,C7,C25,C26	4
4	0.33µF, 25V, ±10%	ROHM MCH182CN334KK	0805	C3	1
5	4700pF, 25V, ±10%	ROHM MCH182CN472KK	0805	C5, C6, C22	3
6	270µF, 2V, Poly Elect	CDE ESRE271M02B	D7.3x4.3	C10-C13	4
7	180µF, 4V, Poly Elect	CDE ESRE181M04B	D7.3x4.3	C14-C17, C24,C36	6
8	150µF, 6V, Poly Elect	CDE ESRE151M06B	D7.3x4.3	C18,C35	2
9	100µF, 16V, Poly Elect	NEC NRD107M16	D7.3x4.3	C19,C34	2
10	680µF, 6.3V, ±20% Poly	FUJITSU FP-063RE681M-R	10x10.5	C20	1
11	470µF, 16V, ±20%, AL-EL	PANASONIC EEU-FC1C471	10x10.5	C21	1
12	1µF, 16V, Ceramic	Taiyo Yuden EMK316BJ105ML	1206	C9	1

RESISTORS

Line Item	Part Description	Manufacturer & Part #	Case	Reference Designators	Qty
1	0Ω Jumper	ROHM SGE2372-5	0805	R3 R31, R34, R37, R41,R43, R45, R50, R53	9
2	0Ω Jumper	ROHM Buss Wire	#18GA	R6	1
4	2K, 1%, 1/8W	ROHM MCR10F2001	0805	R7, R9, R11, R12, R14, R15, R19, R22	8
5	200K, 1%, 1/8W	ROHM MCR10F2003	0805	R8, R13	2
6	4.25K, 1%, 1/8W	ROHM MCR10F4251	0805	R10	1
7	2.21K, 1%, 1/8W	ROHM MCR10F2211	0805	R16	1
8	61.9K, 1%, 1/8W	ROHM MCR10F6192	0805	R18, R21, R23	3
9	3.402K, 1%, 1/8W	ROHM MCR10F3401	0805	R24	1
10	1.58K, 1%, 1/8W	ROHM MCR10F1581	0805	R25	1
11	20K, 1%, 1/8W	ROHM MCR10F2002	0805	R28-R30	3

Figure 8

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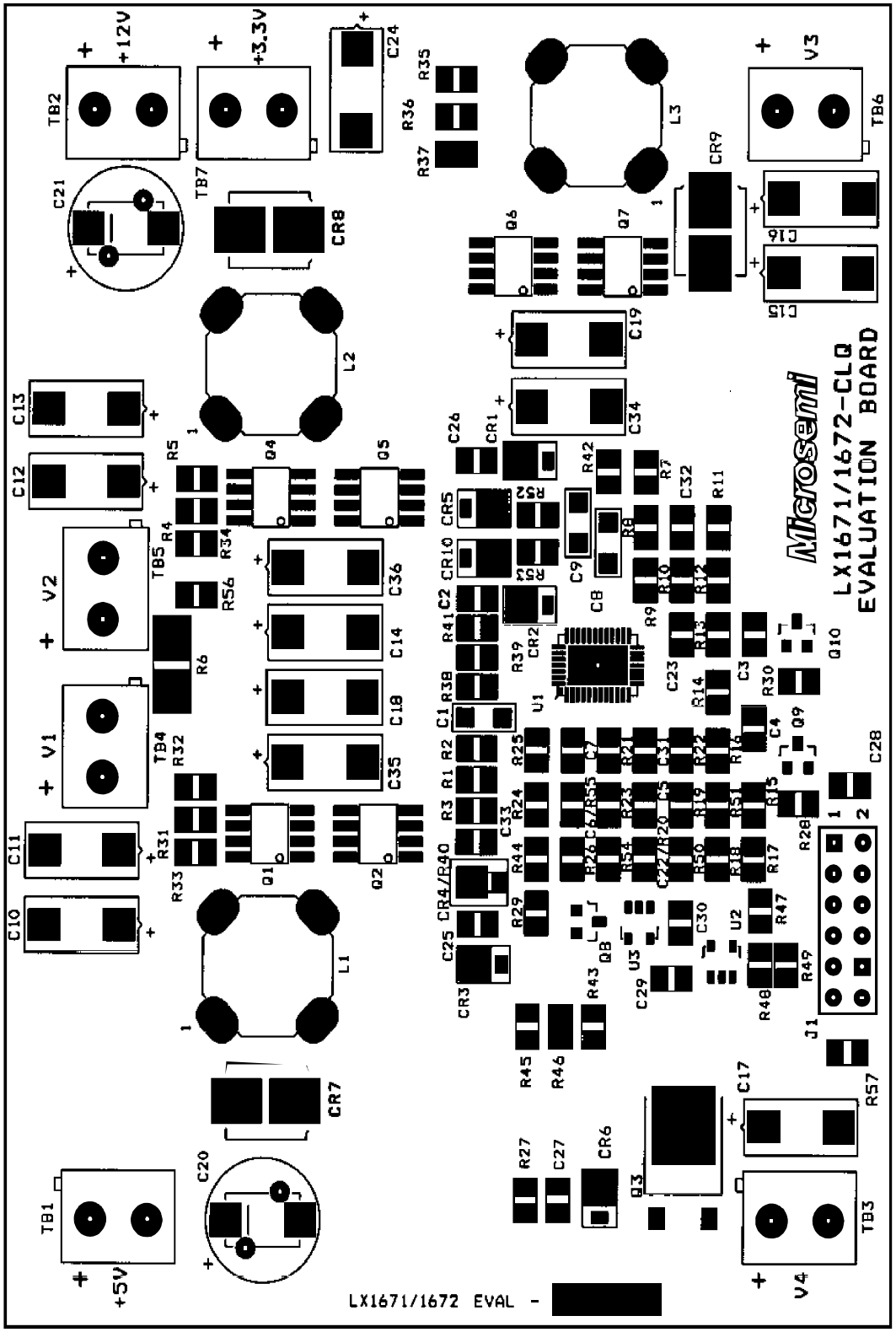
PCB SILK SCREEN



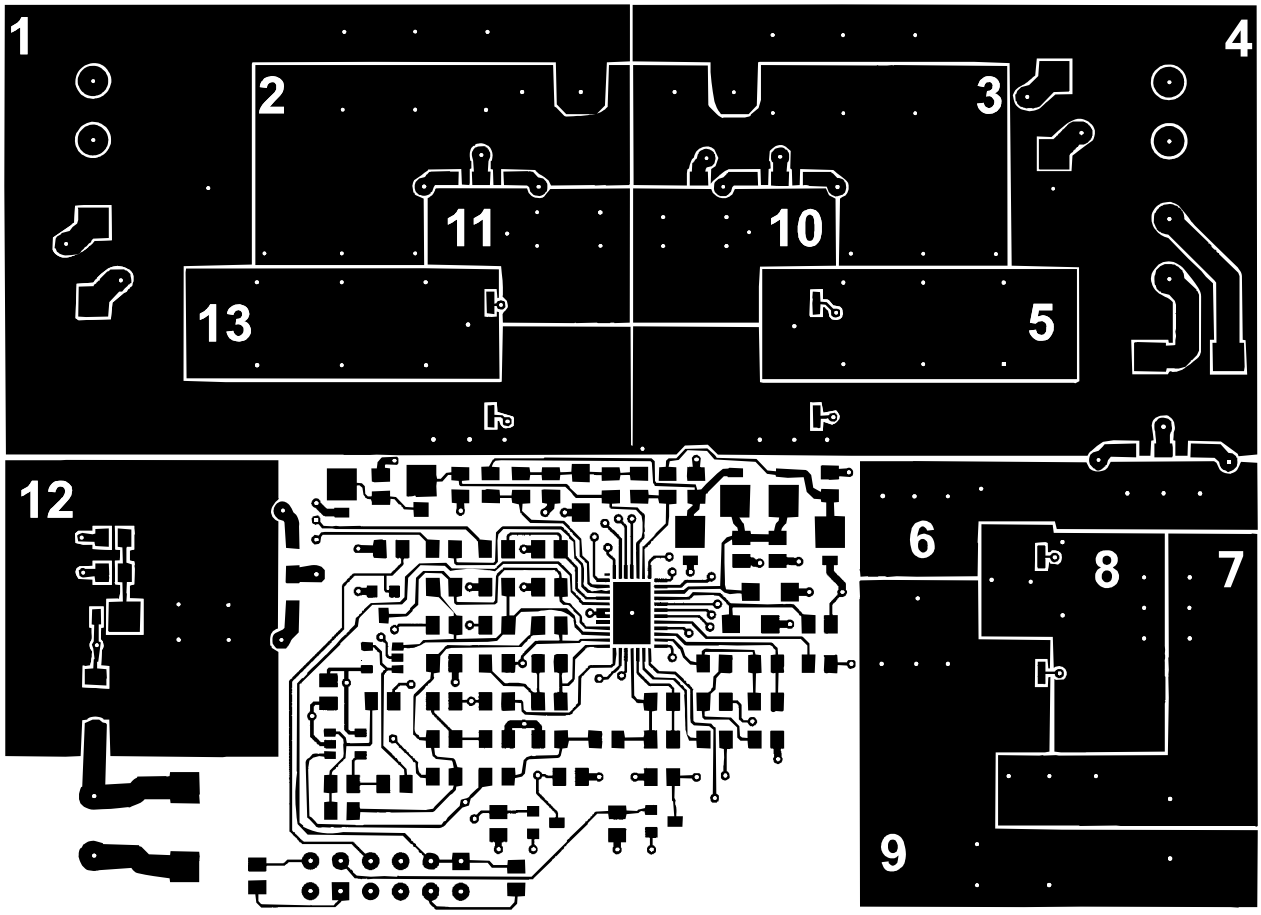


Figure10 Component Side Layer 1

1. Power Ground
2. Phase 1 VOUT
3. Phase 2 VOUT
4. Power Ground
5. Phase 2 Phase Node
6. Phase 3 Input
7. Phase 3 VOUT
8. Phase 3 Phase Node
9. Power Ground
10. Phase 2 Input
11. Phase 1 Input
12. LDO Input
13. Phase 1 Phase Node

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PCB LAYOUT / LAYERS

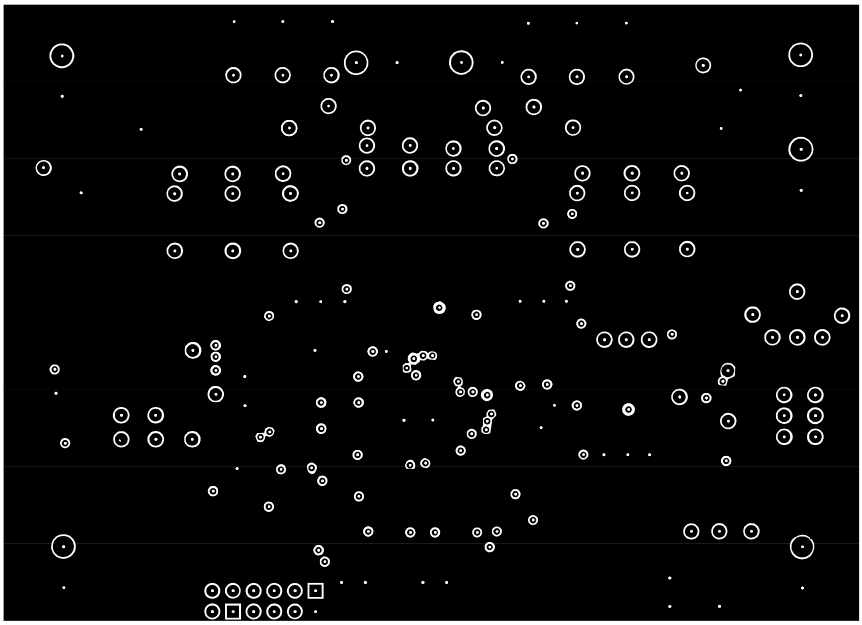
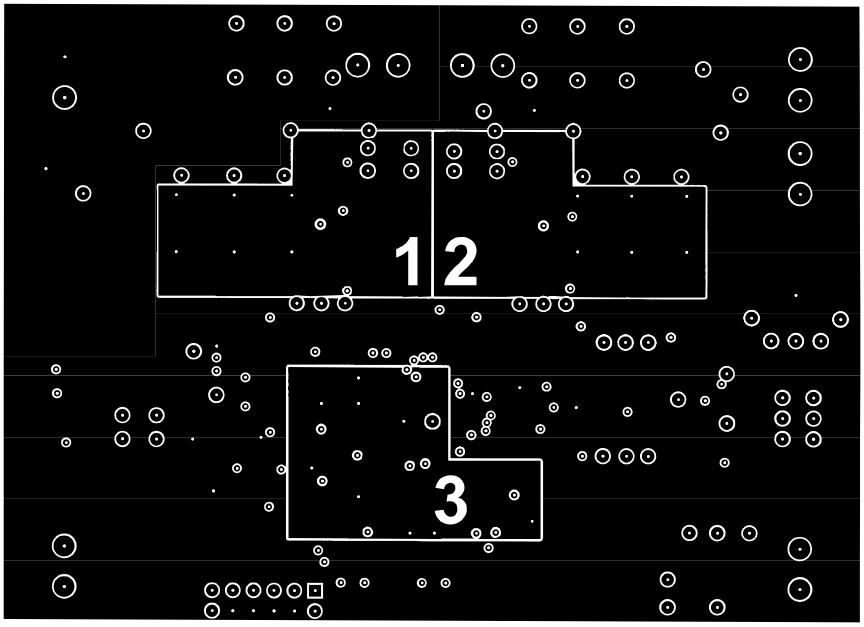


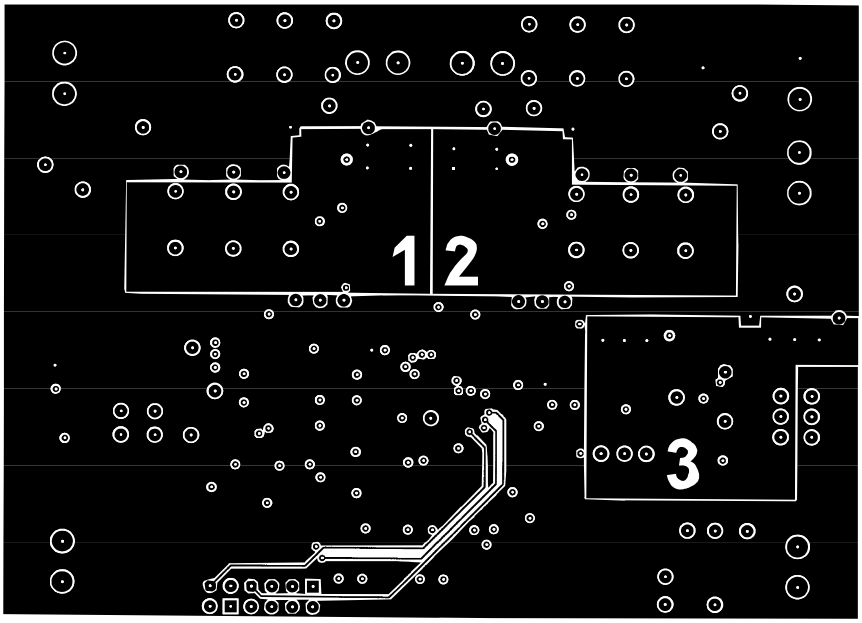
Figure 11 – Ground Plane Layer 2



1. Phase 1 Phase Node
2. Phase 2 Phase Node
3. Analog Ground

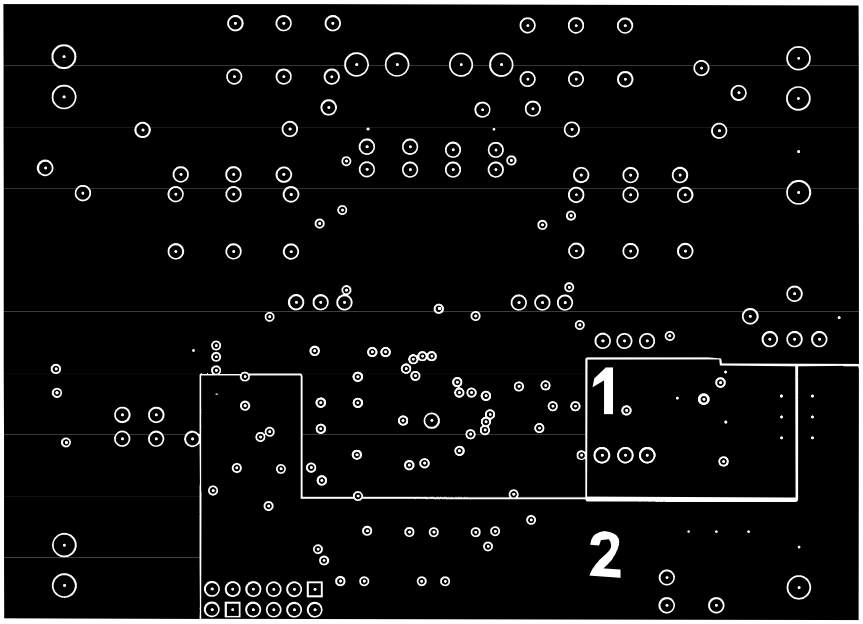
Figure 12 - +5V Plane Layer 3

PCB LAYOUT / LAYERS



1. Phase 1 Input
2. Phase 2 Input
3. Phase 3 Input

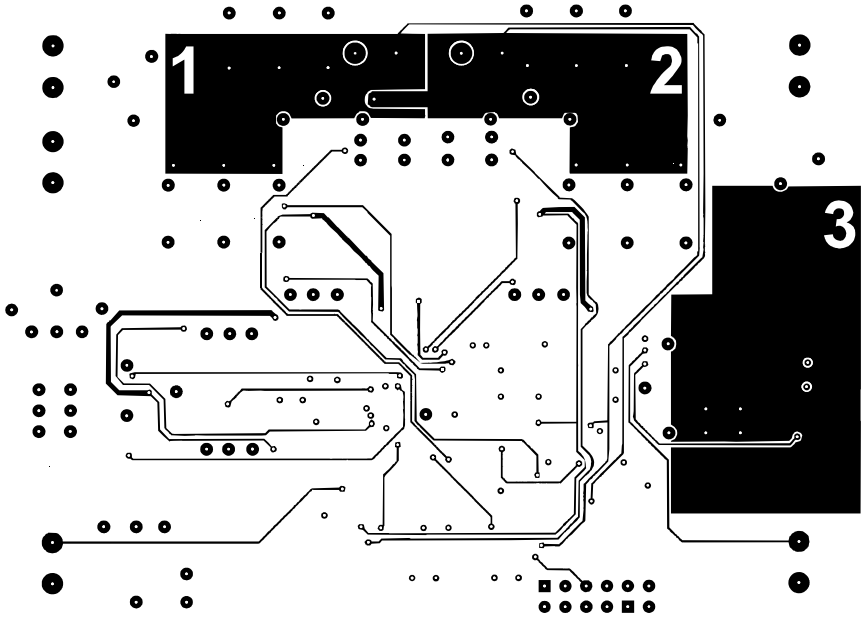
Figure 13 - +12V Plane Layer 4



1. Phase 3 Phase Node
2. Phase 3 VOUT

Figure 14 - +3.3V Plane Layer 5

PCB LAYOUT / LAYERS



1. Phase 2 VOUT
2. Phase 1 VOUT
3. LDO Input

Figure 15 – Layer 6 (Solder Side View)