

TPS22051 DUAL-SLOT PC CARD POWER-INTERFACE SWITCH WITH SUSPEND MODE FOR PARALLEL PCMCIA CONTROLLER

SLVS128 – OCTOBER 1995

- Fully Integrated V_{CC} and V_{PP} Switching for Dual-Slot PC Card™ Interface
- Suspend Mode (3.3 V only)
- Compatible With Controllers From Cirrus, Intel, and Texas Instruments
- Meets PCMCIA Standards
- Internal Charge Pump (No External Capacitors Required) – 12-V Supply Can Be Disabled Except for Programming
- Short Circuit and Thermal Protection
- SSOP (30) Package Less than 2 mm High
- Compatible With 3.3-V, 5-V and 12-V PC Cards
- Power Saving $I_{DD} = 83 \mu A$ Typ, $I_Q = 1 \mu A$
- Low $r_{DS(on)}$ (150-m Ω 5-V Switch; 200-m Ω 3.3-V Switch)
- Break-Before-Make Switching

DF or DB PACKAGE
(TOP VIEW)

5V	1	30	5V
5V	2	29	B_VPP_PGM
A_VPP_PGM	3	28	B_VPP_VCC
A_VPP_VCC	4	27	B_VCC5
A_VCC5	5	26	B_VCC3
A_VCC3	6	25	NC
12V	7	24	12V
AVPP	8	23	BVPP
AVCC	9	22	BVCC
AVCC	10	21	BVCC
AVCC	11	20	BVCC
GND	12	19	NC
NC	13	18	OC
SHDN	14	17	3.3V
3.3V	15	16	3.3V

NC - No Internal Connection

description

The TPS2205 PC Card (PCMCIA) power interface switch provides an integrated power-management solution for two PC Cards. All of the discrete power MOSFETs, a logic section, current limiting and reporting, and thermal protection for PC Card control are combined on a single integrated circuit (IC), using the Texas Instruments LinBiCMOS™ process. The circuit allows the distribution of 3.3-V, 5-V and/or 12-V card power and is compatible with most PCMCIA controllers. The suspend mode allows the TPS2205 to operate off of 3.3-V input pins during modem or pager operations. The current-limiting feature eliminates the need for fuses, which reduces component count and improves reliability; current-limit reporting can help the user isolate a system fault to a bad card.

The TPS2205 maximizes battery life by generating its own switch-drive voltage using an internal charge pump. Therefore, the 12-V supply can be powered down and only brought out of standby when flash memory needs to be written to or erased. End equipment for the TPS2205 includes notebook computers, desktop computers, personal digital assistants (PDAs), digital cameras, handterminals, and bar-code scanners.

The TPS2205I is only available in the DB package, left-end taped and reeled (indicated by the LE suffix on the device type; when ordering, specify TPS2205IDBLE).

LinBiCMOS is a trademark of Texas Instruments Incorporated.
PC Card is a trademark of PCMCIA (Personal Computer Memory Card International Association).

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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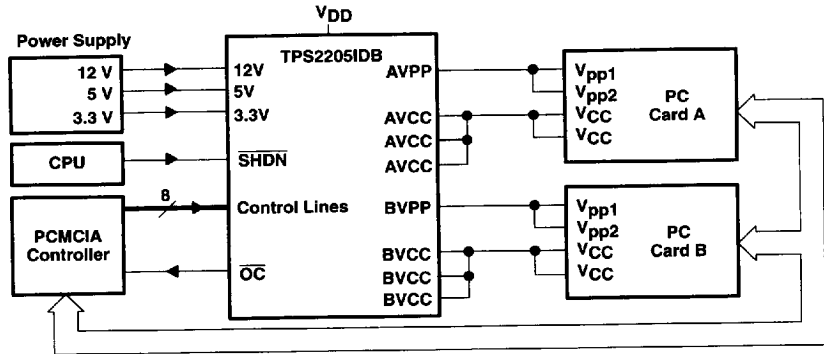
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typical PC Card power distribution application



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD}	-0.3 V to 7 V
Input voltage range for card power: $V_{I(5V)}$	-0.3 V to 7 V
$V_{I(3.3V)}$	-0.3 V to $V_{I(5V)}$
$V_{I(12V)}$	-0.3 V to 14 V
Logic input voltage	-0.3 V to 7 V
Continuous total power dissipation	See Dissipation Rating Table
Output current (each card): $I_{O(xVCC)}$	internally limited
$I_{O(xVPP)}$	internally limited
Operating virtual junction temperature range, T_J	-40°C to 150°C
Operating free-air temperature range, T_A	-40°C to 85°C
Storage temperature range, T_{stg}	-55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DF	1158 mW	9.26 mW/°C	741 mW	602 mW
DB	1024 mW	8.2 mW/°C	655 mW	532 mW

‡ These devices are mounted on an FR4 board with no special thermal considerations.

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Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
A_VCC3	6	I	Logic input that controls voltage on AVCC (see control-logic table)
A_VCC5	5	I	Logic input that controls voltage on AVCC (see control-logic table)
A_VPP_PGM	3	I	Logic input that controls voltage on AVPP (see control-logic table)
A_VPP_VCC	4	I	Logic input that controls voltage on AVPP (see control-logic table)
AVCC	9, 10, 11	O	Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance
AVPP	8	O	Switched output that delivers 0 V, 3.3 V, 5 V, 12 V, or high impedance
B_VCC3	26	I	Logic input that controls voltage on BVCC (see control-logic table)
B_VCC5	27	I	Logic input that controls voltage on BVCC (see control-logic table)
B_VPP_PGM	29	I	Logic input that controls voltage on BVPP (see control-logic table)
B_VPP_VCC	28	I	Logic input that controls voltage on BVPP (see control-logic table)
BVCC	20, 21, 22	O	Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance
BVPP	23	O	Switched output that delivers 0 V, 3.3 V, 5 V, 12 V, or high impedance
SHDN	14	I	Logic input that shuts down the TPS2205 and set all power outputs to high-impedance state
OC	18	O	Logic-level overcurrent reporting output that goes low when an overcurrent condition exists
VDD	25		5-V power to chip
GND	12		Ground
3.3V	15, 16, 17	I	3.3-V V _{CC} in for card power
5V	1, 2, 30	I	5-V V _{CC} in for card power
12V	7, 24	I	12-V VPP in for card power
NC	13,19		

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V _{DD}		TBD	TBD	V
Input voltage range, V _I	V _I (5 V)	0	5.25	V
	V _I (3.3 V)	0	V _I (5 V) [†]	V
	V _I (12 V)	0	13.5	V
Output current	I _O (xVCC) at 25°C		1	A
	I _O (xVPP) at 25°C		150	mA
Operating virtual junction temperature, T _J		–40	125	°C

[†] V_I(3 V) should not be taken above V_I(5 V).

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electrical characteristics, $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$ (unless otherwise noted)
dc characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switch resistances	5 V to xVCC			150		m Ω
	3.3 V to xVCC			200		m Ω
	3.3 V to xVCC	Suspend mode		500		m Ω
	5 V to xVPP				6	Ω
	3.3 V to xVPP				6	
	12 V to xVPP				1	
$V_O(xVPP)$ Clamp low voltage		I_{pp} at 10 mA			0.8	V
$V_O(xVCC)$ Clamp low voltage		I_{CC} at 10 mA			0.8	V
Leakage current	I_{pp} High-impedance state	$T_A = 25^\circ\text{C}$		1	10	μA
		$T_A = 85^\circ\text{C}$			50	
	I_{CC} High-impedance state	$T_A = 25^\circ\text{C}$		1	10	
		$T_A = 85^\circ\text{C}$			50	
Input current	I_{DD} Supply current	$V_O(AVCC) = V_O(BVCC) = 5\text{ V}$, $V_O(AVPP) = V_O(BVPP) = 12\text{ V}$		83	150	μA
	I_{DD} Supply current in shutdown	$V_O(BVCC) = V_O(AVCC) = V_O(AVPP) = V_O(BVPP) = \text{high Z}$			1	μA
Power-ready threshold, PWR_GOOD			10.72	11.05	11.4	V
Power-ready hysteresis, PWR_GOOD		12-V mode		50		mV
Short-circuit output-current limit	$I_O(xVCC)$	$T_J = 85^\circ\text{C}$, Output shorted to GND		1		A
	$I_O(xVPP)$		120	200	400	mA

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electrical characteristics, $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$ (unless otherwise noted) (continued)

logic section

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Logic input current			1	μA
Logic input high level		2		V
Logic input low level			0.8	V
Logic output high level	$I_O = 1\text{ mA}$	$V_{DD} - 0.4$		V
Logic output low level			0.4	V

switching characteristics†

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r, t_f Output rise and fall times	$V_O(xVCC)$ rise time		1.2		ms
	$V_O(xVCC)$ fall time		10		ms
	$V_O(xVPP)$ rise time		5		ms
	$V_O(xVPP)$ fall time		14		ms
t_{pd} Propagation delay (see Figure 1‡)	$V_I(x_VPP_PGM)$ to $V_O(xVPP)$	t_{on}	5.8		ms
		t_{off}	18		ms
	$V_I(x_VCC3)$ to $xVCC$	t_{on}	5.8		ms
		t_{off}	28		ms
	$V_I(x_VCC5)$ to $xVCC$	t_{on}	4		ms
		t_{off}	30		ms

† Refer to Parameter Measurement Information

‡ Rise and fall times are with $C_L = 100\text{ }\mu\text{F}$.

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APPLICATION INFORMATION

TPS2205 control logic

AVPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
SHDN	A_VPP_PGM	A_VPP_VCC	S7	S8	S9	VAVPP
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	VCC†
1	1	0	OPEN	OPEN	CLOSED	VPP(12 V)
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	X	X	OPEN	OPEN	OPEN	Hi-Z

BVPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
SHDN	B_VPP_PGM	B_VPP_VCC	S10	S11	S12	VBVPP
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	VCC‡
1	1	0	OPEN	OPEN	CLOSED	VPP(12 V)
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	X	X	OPEN	OPEN	OPEN	Hi-Z

AVCC

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
SHDN	A_VCC3	A_VCC5	S1	S2	S3	VAVCC
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	3 V
1	1	0	OPEN	OPEN	CLOSED	5 V
1	1	1	CLOSED	OPEN	OPEN	0 V
0	X	X	OPEN	OPEN	OPEN	Hi-Z

BVCC

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
SHDN	B_VCC3	B_VCC5	S4	S5	S6	VBVCC
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	3 V
1	1	0	OPEN	OPEN	CLOSED	5 V
1	1	1	CLOSED	OPEN	OPEN	0 V
0	X	X	OPEN	OPEN	OPEN	Hi-Z

† Output depends on AVCC

‡ Output depends on BVCC

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