

FEATURES

- Full Dielectric Isolation for High Reliability
- 45 dB typical Output Off Isolation at 10 Mhz
- Typical on resistance, R_{ON} , is 28 ohms
- Excellent Noise Immunity & Extremely Low Isol
- On-chip Shift Register, and Latch Logic Circuitry
- Fully Flexible High Voltage Supply Combinations
- DC to 10Mhz Analog Signal Frequency
- Excellent Latch-up Immunity
- Eight 300V Bi-directional Analog Switches

ABSOLUTE MAXIMUM RATINGS*

V_{DO} Logic Power Supply Voltage	0.5V to 18V
V_{PP} - V_{NN} Supply Voltage	300V
V_{PP} Positive High Voltage Supply	-0.5V to $V_{NN} + 265V$
V_{NN} Negative High Voltage Supply	-235V
Logic Input Voltage	0.5V to $V_{DD} + 0.3V$
Peak Analog Pulsar Current/Channel	3.0A
Storage Temperature	-65°C to + 150°C
Analog Pulsar Range	$V_{AP} - V_{NN} = 0V$ to 240V
Power Dissipation	Plastic Package 0.8W Ceramic Package 2.0W

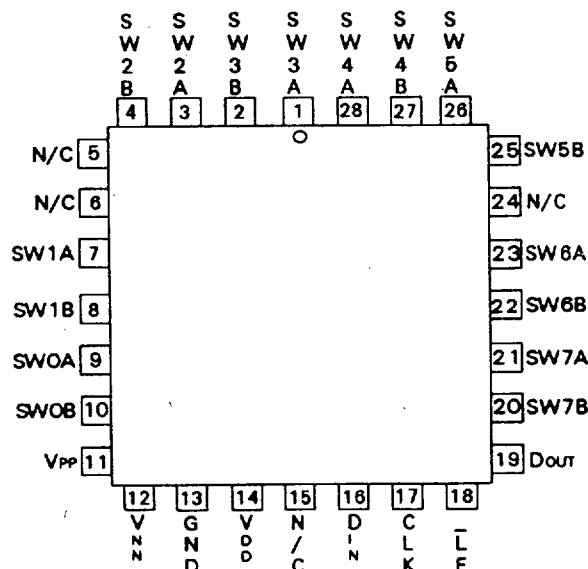
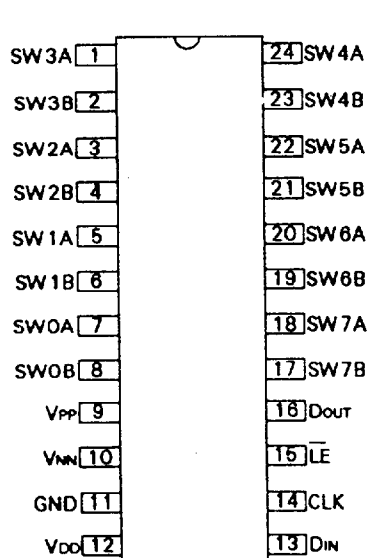
*Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional Operation under these conditions is not implied. Continuous operation of the device at the absolute level may affect device reliability.

GENERAL DESCRIPTION

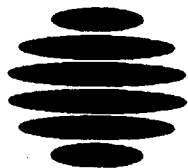
The USH5010 is an 8-channel high voltage analog switch which utilizes Universal's Proprietary full oxide isolation process for switching high voltage analog signals. This device can be used in ultrasound imaging systems and other high voltage applications which requires flexible high voltage switching controlled by internal CMOS logic signals.

The USH5010 combines high voltage bidirectional DMOS switches with low power CMOS logic to provide efficient control of high voltage analog signals. Input data is shifted into an 8-bit latch. To minimize any clock feedthrough noise, Latch Enable Bar should be left high until all bits are clocked in.

The USH5010, for example, is suitable for various combinations of high voltage supplies, e.g., + 80V/- 220V, or + 150V/-150V, or +290V/-10V applications



Vpp-Vnn	28-Lead Ceramic Lcc	24-lead Ceramic Side-Brazed	24-lead plastic DIP	28-lead PLCC	Operating Temperatures
300V	USH5010-AIL 28	USH5010-AIC24	USH5010-AIP 24	USH 5010-AIK28	0°C TO 70°C



ELECTRICAL CHARACTERISTICS

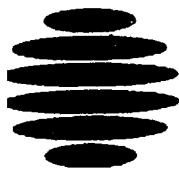
(over recommended operating conditions, $V_{PP} = +110V$, $V_{NN} = -100V$ and $V_{DD} = 15V$ unless otherwise noted)*

DC CHARACTERISTICS

PARAMETERS	SYM	0°C		25°C			70°C		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
Small Signal Ron	R _{ONS}		30		24	30		45	ohms	I _{sw} = 5mA
Large Signal Ron	R _{ONS}		20		20	22		23	ohms	I _{sw} = 200mA
Delta Ron	Δ R _{ONS}		20		10	20		20	%	I _{sw} = 5mA
Large Signal Ron	R _{ONL}		90		28	40		100	ohms	V _{AP} = V _{PP} -10V I _{sw} =5mA
Switch Off Leakage/SW	I _{SOI}		1		0.5	1		1	uA	V _{AP} = V _{PP} -10V/V _{NN} +10V
DC Offset Switch Off	I _{DCOFF}		1		1	1		1	mV	R _L = 100K
DC Offset Switch On	I _{DCON}		1		1	1		1	mV	R _L = 100K
Pos. HV Supply Current	I _{PPQOFF}		10		50				uA	ALL SWITCHES OFF
Neg. HV Supply Current	I _{NNQOFF}		-10		-50				uA	ALL SWITCHES OFF
Pos. HV Supply Current	I _{PPQON}		10		50				uA	ALL SWITCHES ON I _{sw} =5mA
Neg. HV Supply Current	I _{NNQON}		-10		-50				uA	ALL SWITCHES ON I _{sw} =5mA
Analog Pulse Pk Current	I _{PAP}		2		1.5	2		2	A	V _{AP} Duty Cycle < 0.1%
Output Switch Frequency	f _{SW}		50		50			50	Khz	Duty Cycle = 50%
I _{PP} Ave. Supply Current	I _{PPAV}		5		6.5				mA	f _{sw} = 50Khz
I _{NN} Ave. Supply Current	I _{NNAV}		5		6.5				mA	f _{sw} = 50Khz
V _{DD} Ave. Current	I _{DDAV}		6		6			6	mA	f _{CLK} = 3Mhz
V _{DD} Quiescent Current	I _{DDQ}		10		1.8	5		10	uA	
Data Out Source Current	I _{SOR}	1.8		1.8			1.8		mA	V _{OUT} = V _{DD} -0.7V
Data Out Sink Current	I _{SINK}		-1.8			-1.8		-1.8	mA	V _{OUT} = 0.7V

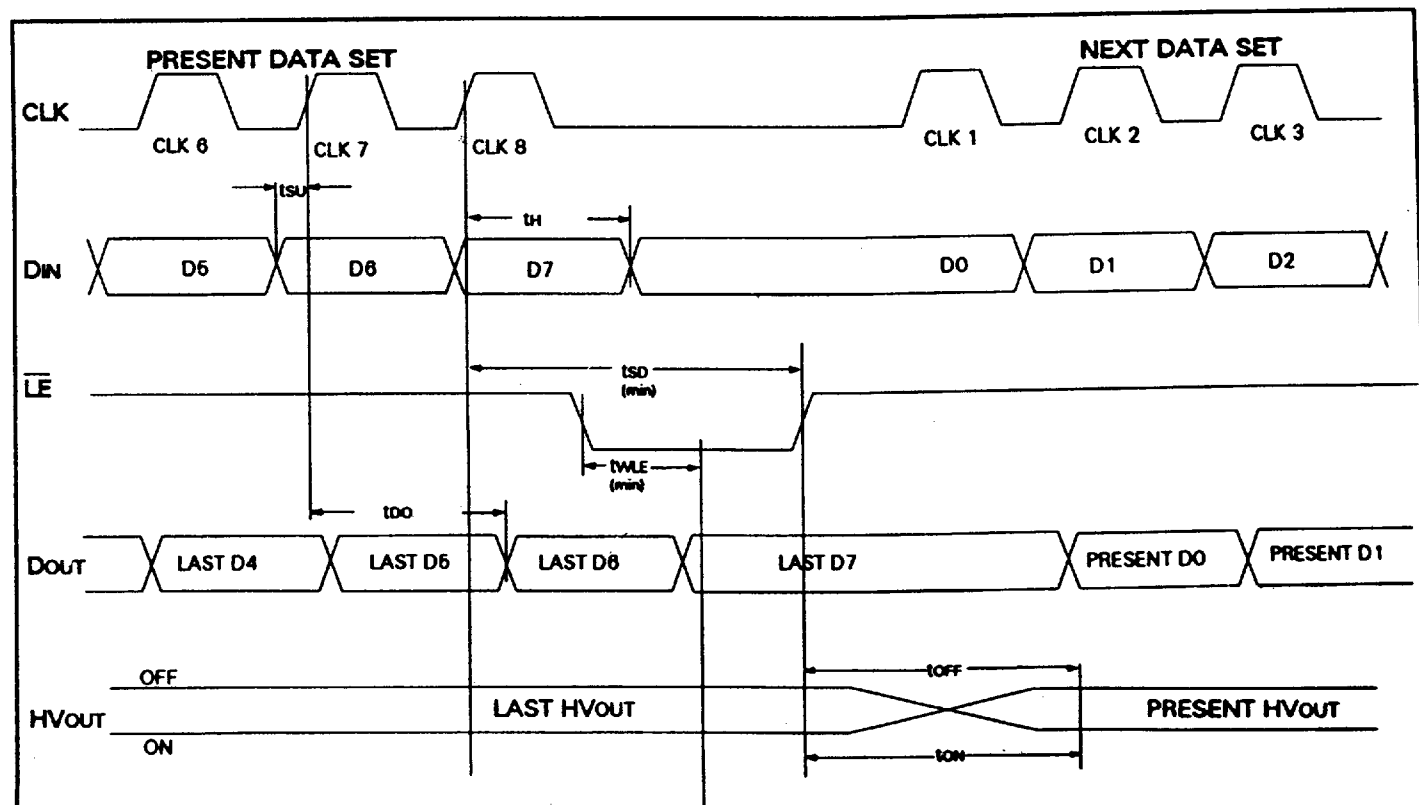
AC CHARACTERISTICS

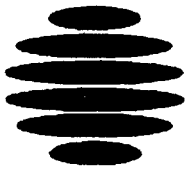
PARAMETERS	SYM	0°C		25°C			70°C		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
Set Up Time Before LE Rises	t _{SD}	150		150			150		ns	
LE Pulse Width	t _{WLE}	50		50			50		ns	
Clock to Dout Delay Time	t _{DO}		300			300		300	ns	
Din to Clock Set Up Time	t _{SU}	30		30			30		ns	
Din to Clock Hold Time	t _H	30		30			30		ns	
Logic Input Rise & Fall Time	t _R /t _F	10	200	10	10	200	10	200	ns	
Max. Logic Clock Frequency	f _{CLK}		5			5		5	Mhz	
CLK to HVOUT Turn On Time	t _{ON}		5		2	5		5	us	R _L = 10K ohm
CLK to HVOUT Turn Off Time	t _{OFF}		5		3	5		5	us	R _L = 10K ohm
Channel - Channel Cross-talk	K _{CR}	-60		-60	-65		-60		dB	f _{MN} = 5Mhz/50 ohm load
Single Channel Off-Isolation	K _O	-45		-45	-50		-45		dB	f _{MN} = 5Mhz/50 ohm load
Max. Positive Noise Glitch	V _{GP}		500			500		500	mV	680 ohms//220 pf load
Max. Negative Noise Glitch	V _{GN}		-1.2			-1.2		-1.2	V	680 ohms//220 pf load
Analog Pulser Rise & Fall Time	V _{APDVT}				12				V/ns	I _{VAP} = 180V in 15ns
Analog Pulser Max. Bandwidth	f _{VAP}		10			10		10	Mhz	
Logic Input Cap.	C _A				3				pf	0V, 1Mhz
Switch Off Cap. to GND	C _{SG(OFF)}		10		8	10		10	pf	0V, 1Mhz
Switch On Cap. to GND	C _{SG(ON)}		30		18	30		30	pf	0V, 1Mhz



RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Device			Other Conditions
		USH50 10-AI			
V _{PP}	Logic Power Supply Voltage	10V to 15.5V ^{**}			
V _{PP} Mode A	Positive High Voltage Supply	40V			
V _{NN} Mode A	Negative High Voltage Supply	-230V			
V _{AP} Mode A	Analog Pulser Voltage Range	-220V < V _{AP} < 30V			
V _{PP} Mode B	Positive High Voltage Supply	135V			
V _{NN} Mode B	Negative High Voltage Supply	-135V			
V _{AP} Mode B	Analog Pulser Voltage Range	-125V < V _{AP} < 125V			
V _{PP} Mode C	Positive High Voltage Supply	260V			
V _{NN} Mode C	Negative High Voltage Supply	-10V			
V _{AP} Mode C	Analog Pulser Voltage Range	0V < V _{AP} < 250V			
V _{PP} Mode D	Positive High Voltage Supply	40V			
V _{NN} Mode D	Negative High Voltage Supply	-10V			
V _{AP} Mode D	Analog Pulser Voltage Range	0V < V _{AP} < 30V			
V _{IH}	Logic Input High Level	V _{DD} -2V < V _{IH} < V _{DD}			
V _{IL}	Logic Input Low Level	0V < V _{IL} < 2V			
Power Sequence	GND, ANY SEQUENCE	SAME	SAME	SAME	V _{NN} < -10V





TRUTH TABLE

D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	OFF							
H								L	ON							
	L							L		OFF						
	H							L		ON						
		L						L			OFF					
		H						L			ON					
			L					L				OFF				
			H					L				ON				
				L				L					OFF			
				H				L					ON			
					L			L						OFF		
					H			L						ON		
						L		L							OFF	
						H		L							ON	
							L	L								OFF
							H	L								ON
X	X	X	X	X	X	X	X	H	HOLDS PREVIOUS STATE							

- Notes :
1. The eight switches operate independently.
 2. Serial data is clocked in on the L $\rightarrow$ H transition CLK.
 3. The switches go to a state retaining their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift register data flows through the latch.
 4. Dout is high when switch 7 is on.
 5. Shift register clocking has no effect on the switch states if $\overline{LE}$ is high.

Description Of Operation

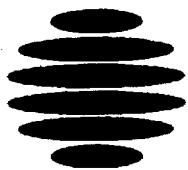
The USH5010 is a High Voltage Integrated Circuit (HIVIC) which contains eight high voltage bidirectional switches and the CMOS logic necessary to interface them to a CMOS environment. This HIVIC is designed to switch various analog signals into capacitive loads, and it is designed to conduct current pulses of 2 Amps with 0.1% duty cycle.

The data in the shift register is transferred to the latches by the latch enable LE. When LE is low the shift register data flows through the latch and controls the state of the switch.

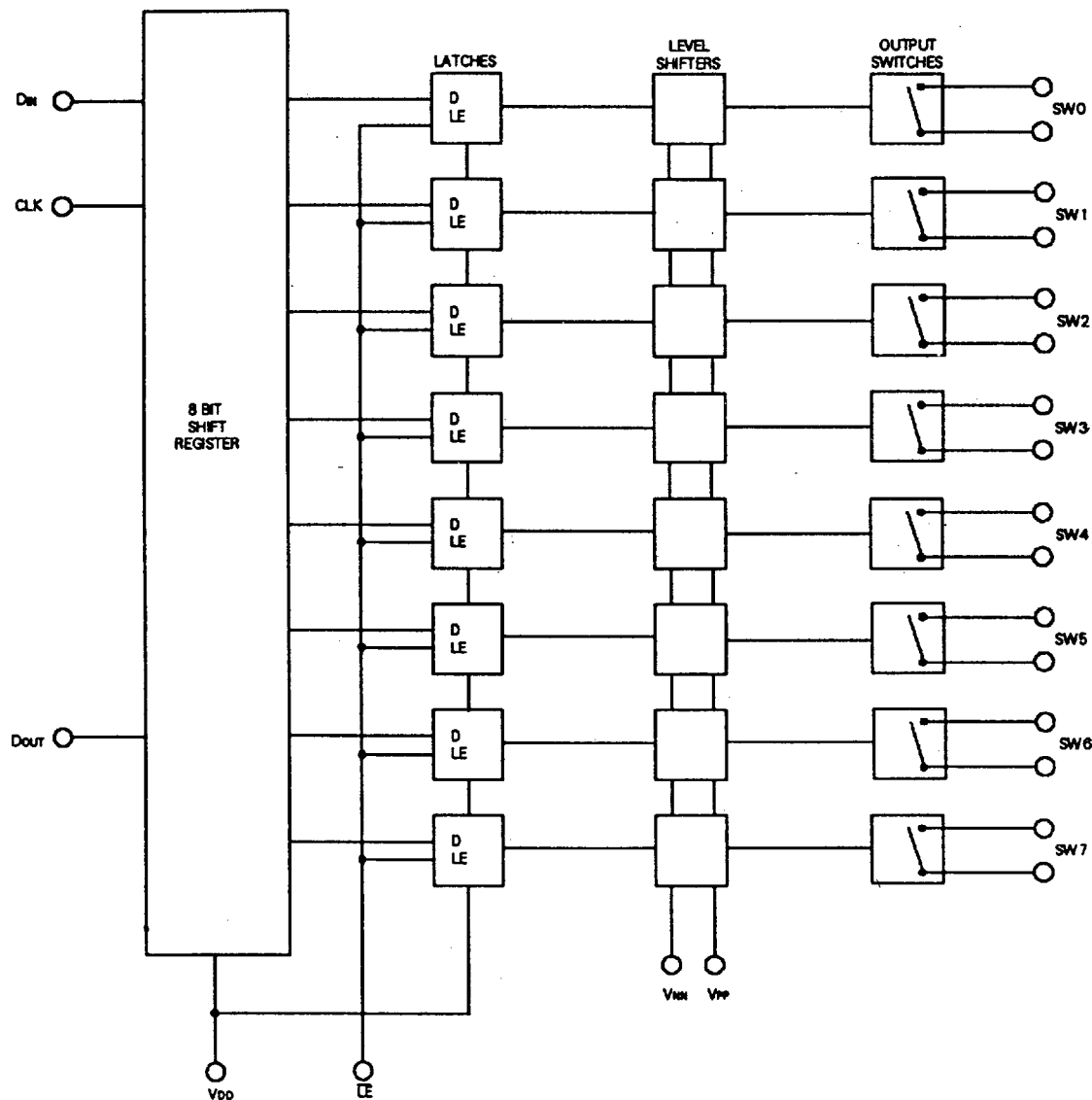
The switches (SW0 - SW7) are controlled by the serial data on (DIN), the shift register clock input (CLK), and the data transfer enable (LE). (See the Timing Diagram and the Truth Table) Serial data on line DIN is clocked into the eight staged static shift registers.

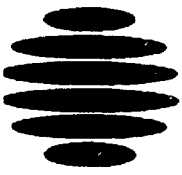
Pin Definitions

DIN	Serial Data Input to Shift Register
CLK	Serial Shift Clock
$\overline{LE}$	Parallel Transfer Enable from Shift Registers to Latches
DOUT	Serial Data Out of Eighth Stage of Shift Register.
SW0-7	Eight Pairs of High Voltage Lines For Analog Signal Switching.
VPP	Positive High Voltage Supply for the Level Shift Circuit.
VNN	Negative High Voltage Supply for the Level Shift Circuits.
Vcc	Logic Supply Pin.



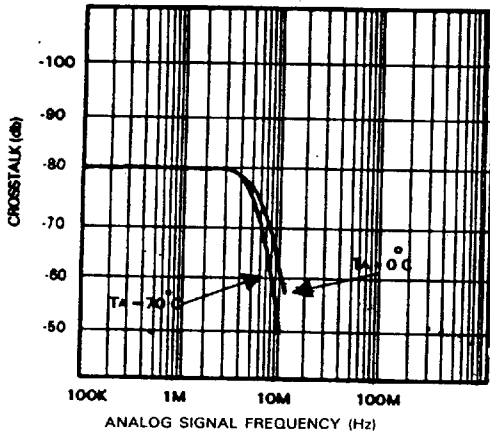
Logic Diagram



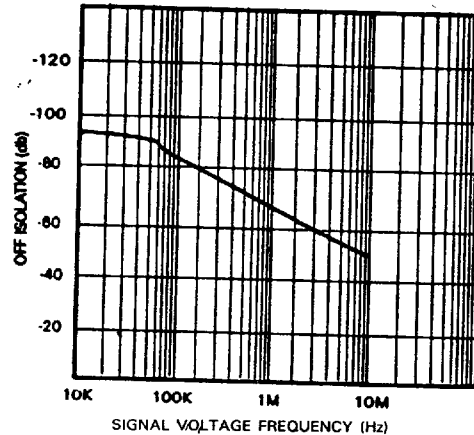


TYPICAL PERFORMANCE CURVES

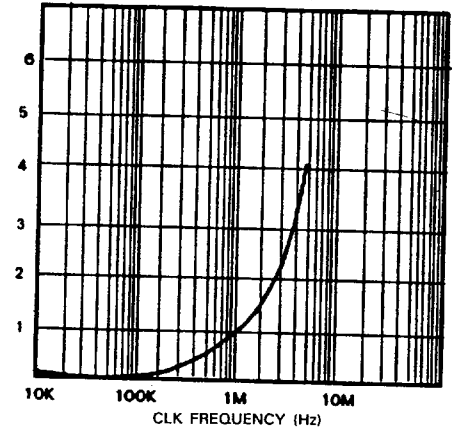
CROSSTALK VS ANALOG SIGNAL FREQUENCY
 $V_{DD} = 15V V_{PP}/V_{NN} + /-80V$



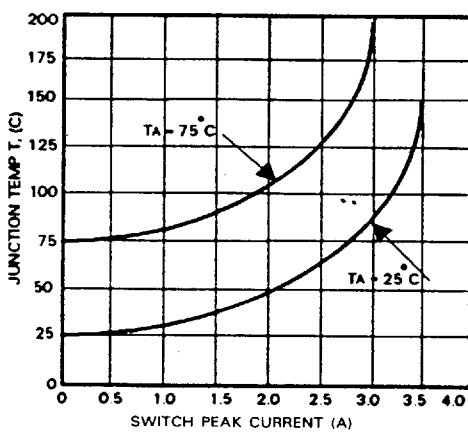
OFF ISOLATION VS SIGNAL VOLTAGE FREQUENCY
 $V_{DD} = 15V V_{PP}/V_{NN} + /-80V$



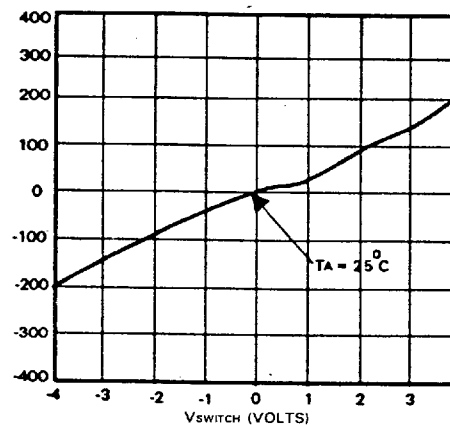
I_{DD} VS CLK FREQUENCY
 $V_{DD} = 15V V_{PP}/V_{NN} + /-80V$



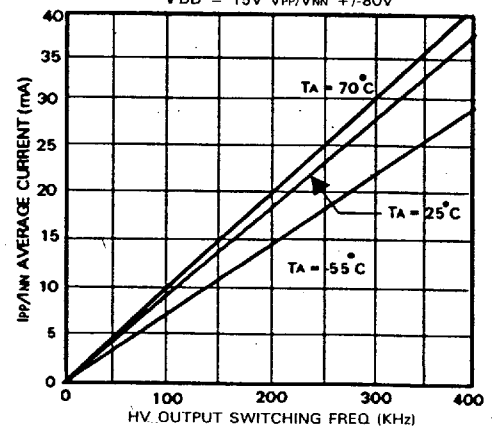
JUNCTION TEMP T_J VS SWITCH PEAK CURRENT
 $V_{SIG FREQ} = 10 KHz$ & DUTY CYCLE = 0.1%
 $V_{DD} = 15V V_{PP}/V_{NN} + /-80V$

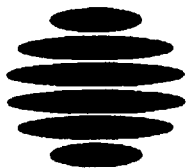


SWITCH CURRENT VS SWITCH VOLTAGE DROP
 $V_{DD} = 15V V_{PP}/V_{NN} + /-80V$

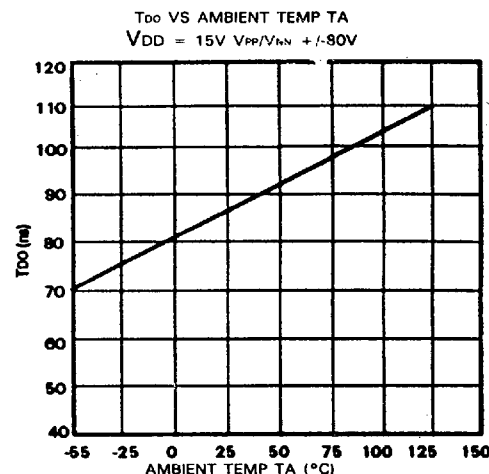
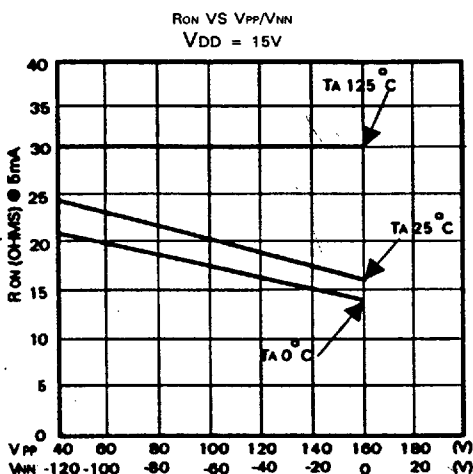
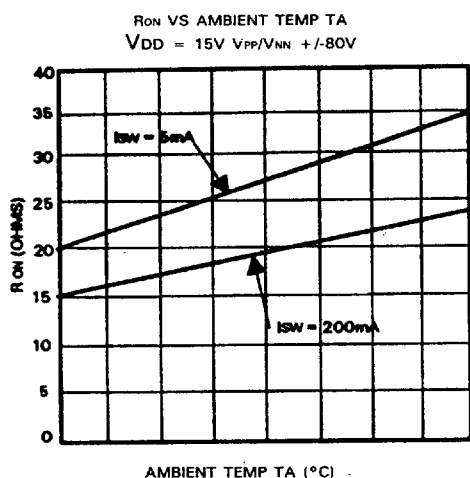


I_{PP}/I_{NN} VS OUTPUT SWITCHING FREQUENCY
 $V_{DD} = 15V V_{PP}/V_{NN} + /-80V$

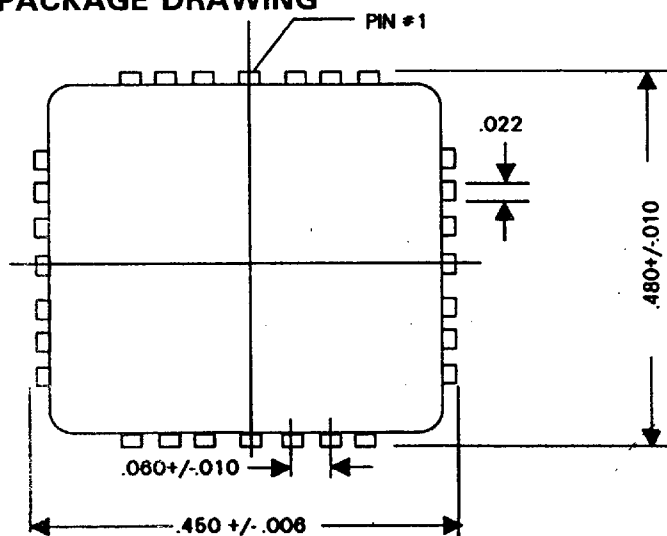




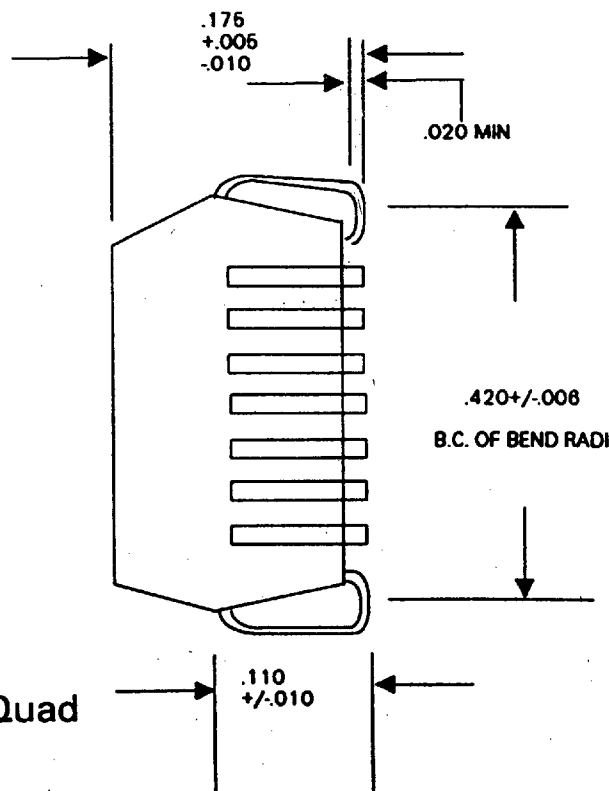
TYPICAL PERFORMANCE CURVES

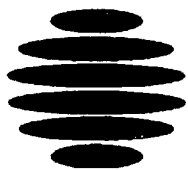


PACKAGE DRAWING

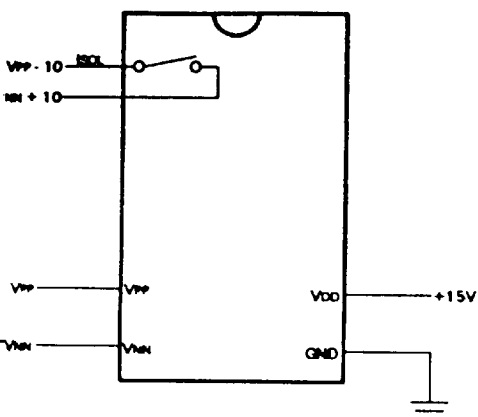


28-lead Plastic Quad
"J" Bend

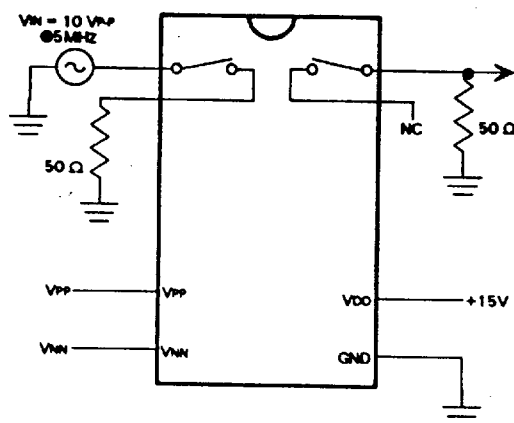




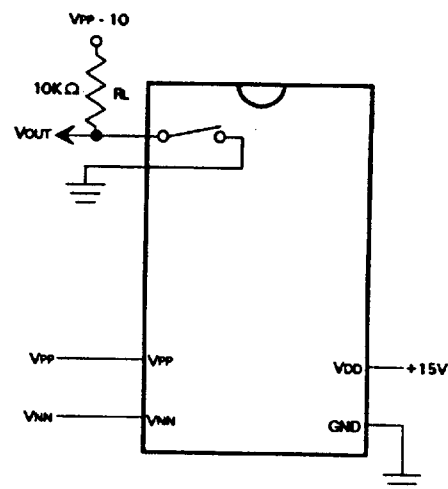
TEST CIRCUITS



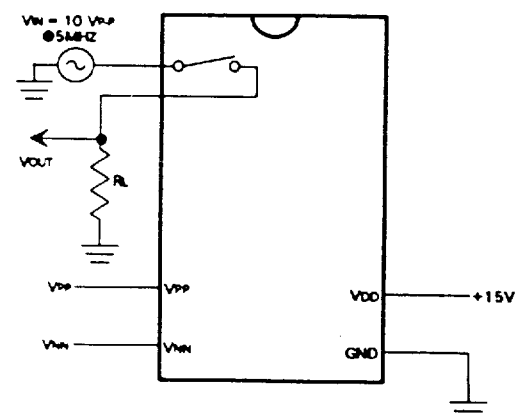
SWITCH OFF LEAKAGE



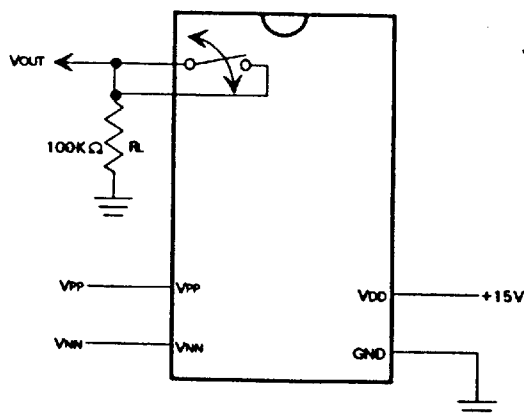
CROSSTALK



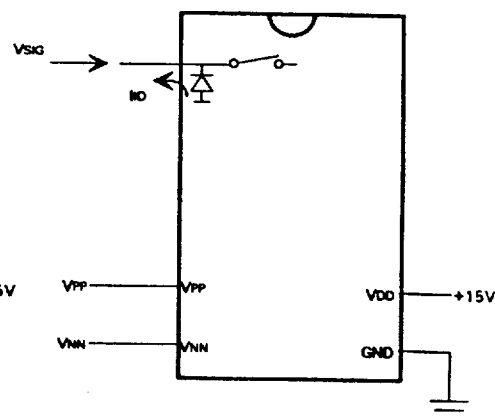
TON/TOFF TEST CIRCUIT



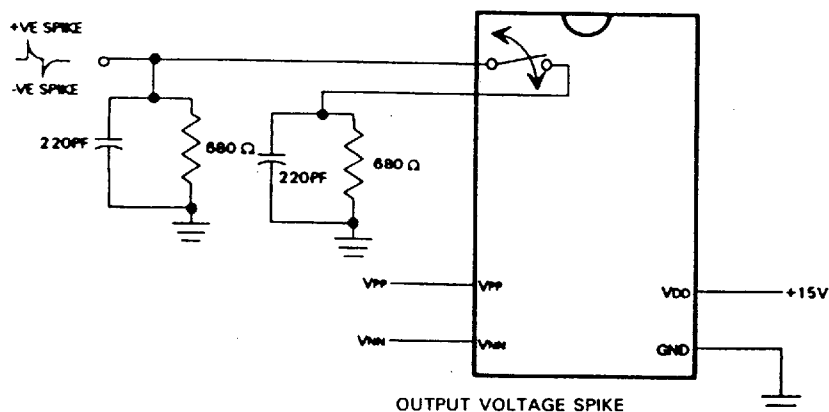
OFF ISOLATION



DC OFFSET ON/OFF



ISOLATION DIODE CURRENT



OUTPUT VOLTAGE SPIKE