Octal transceiver with direction pin (3-State)

54ABT245

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: +48mA/-24mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883C Method 3015.6

DESCRIPTION

The 54ABT245 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 54ABT245 device is an octal transceiver featuring noninverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
20-Pin Ceramic DIP	54ABT245/BRA	GDIP1-T20
20-Pin Ceramic LLCC	54ABT245/B2A	CQCC2-N20

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

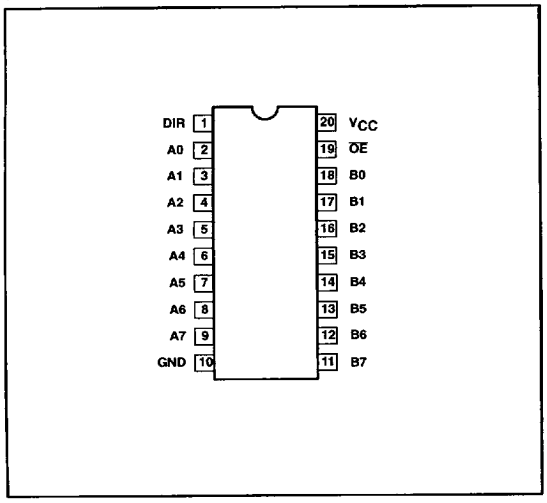
FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	A_n	B_n
L	L	A=B	Inputs
L	H	Inputs	B=A
H	X	Z	Z

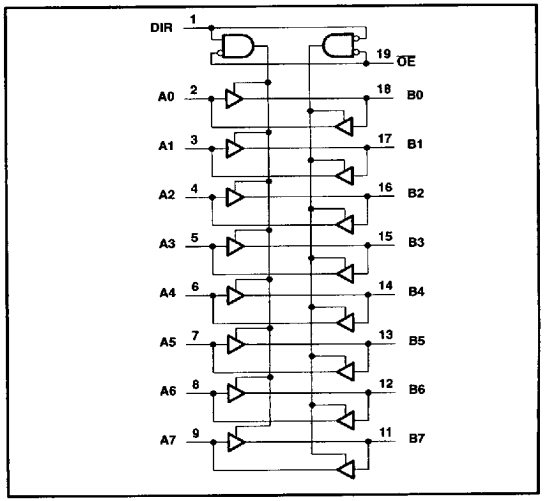
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	DIR	Direction control input
2, 3, 4, 5, 6, 7, 8, 9	A0 - A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B0 - B7	Data inputs/outputs (B side)
19	$\overline{OE}$	Output enable
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

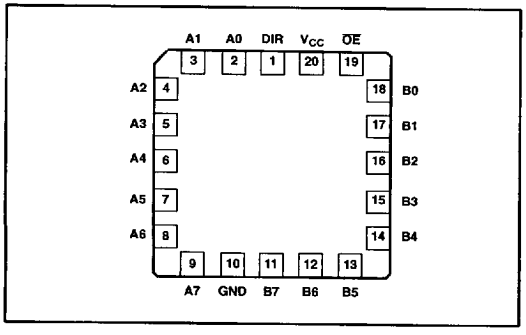
PIN CONFIGURATION



LOGIC SYMBOL



LLCC LEAD CONFIGURATION



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER		CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage			-0.5 to +7.0	V
V_I	DC input voltage[3]	DIR, $\overline{OE}$		-1.2 to +7.0	V
		An, Bn		-1.2 to +5.5	V
I_{OK}	DC output diode current		$V_O < 0$	-50	mA
V_O	DC output voltage[2]		Output in Off or High state	-0.5 to +5.5	V
I_O	DC output current		Output in Low state	96	mA
T_{stg}	Storage temperature range			-65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
I_{IK}	Input clamp current		-18	mA
I_{OH1}	High level output current		-3	mA
I_{OH2}	High level output current		-24	mA
I_{OL}	Low level output current		48	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-55	+125	°C
V_{IL}	Input Low level voltage		0.8	V
V_{IH}	Input High level voltage	2.0		V

DC ELECTRICAL CHARACTERISTICS

(Unless otherwise noted: V_{CC} = MAX, V_I = V_{IL} or V_{IH}, T_{amb} = –55 to +125°C.)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				MIN	TYP	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH1} = -3mA	2.5			V
			I_{OH2} = -24mA	2.0			V
		V_{CC} = 5.0V	I_{OH} = -3mA	3.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_I = V_{IL} or V_{IH}, I_{OL} = MAX			0.42	0.55	V
I_I	Input leakage current	Control Pins	V_I = GND or 5.5V		±0.01	±1.0	µA
		Data Pins[6]	V_I = GND or 5.5V		±5	±100	µA
I_{IH} + I_{OZH}	3-State output High current	V_{CC} = MAX, V_O = 2.7V, V_I = V_{IL} or 3.0V			5.0	10	µA
I_{IL} + I_{OZL}	3-State output Low current	V_{CC} = MAX, V_O = 0.5V, V_I = V_{IL} or 3.0V			-5.0	-10	µA
I_{OFF}	Power off leakage current	V_{CC} = 0V, V_I or V_O ≤ 4.5V		-100	1.0	100	µA
I_{CEX}	Output high leakage current	V_{CC} = 5.5V, V_O = 5.5V				50	µA
I_O	Output current[3]	V_{CC} = MAX, V_O = 2.5V		-50	-100	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = MAX, Outputs High, V_I = GND or V_{CC}			50	250	µA
I_{CCL}		V_{CC} = MAX, Outputs Low, V_I = GND or V_{CC}			24	30	mA
I_{CCZ}		V_{CC} = MAX, Outputs 3-State, V_I = GND or V_{CC}			50	250	µA
ΔI_{CC}	Additional supply current per input pin[4]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND, V_{CC} = MAX			0.5	1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND, V_{CC} = MAX[5]			0.5	50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND, V_{CC} = MAX			0.5	1.5	mA

AC CHARACTERISTICS

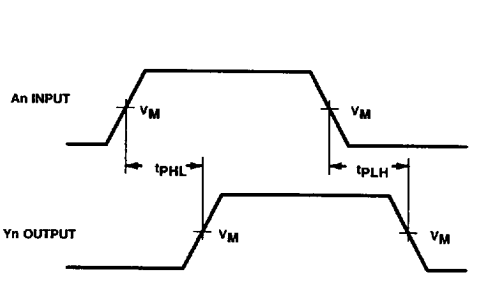
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = -55°C to +125°C, V_{CC} = +5.0V ±0.5V, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	1.0 1.0	2.2 2.9	4.1 4.2	1.0 1.0	4.8 4.8	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.3 2.3	2.9 4.0	4.8 5.8	1.0 2.0	5.9 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2.7 2.3	4.7 4.0	6.2 5.8	2.2 2.0	7.4 6.5	ns

NOTES:

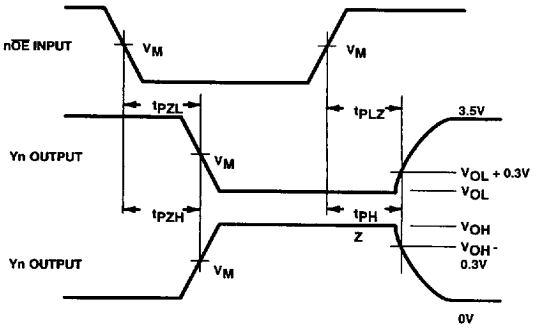
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
4. This is the increase in supply current for each input at 3.4V.
5. Typical value does not include leakage due to external capacitance or fixturing.
6. Input leakage on transceiver data pins also includes I_{OZH} or I_{OZL} current from the output circuitry.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

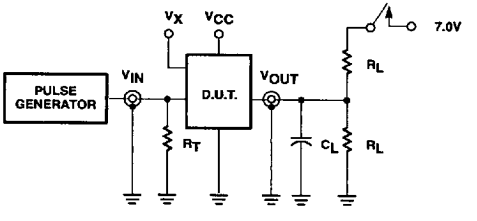


Waveform 1. Waveforms Showing the Input to Output Propagation Delays

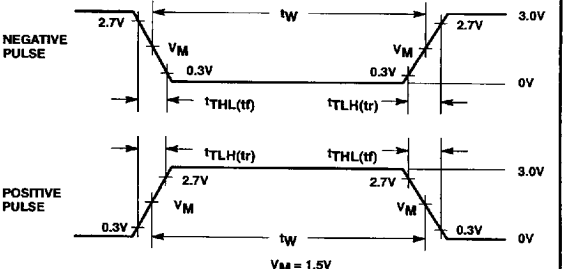


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54ABT	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.