REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
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SHEET	15	16	17	18	19	20	21	22	23	24	25	26							

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
93-03-18

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, 32-BIT RISC MICROPROCESSOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	**5962-92284**

SHEET 1 OF 26

DESC FORM 193
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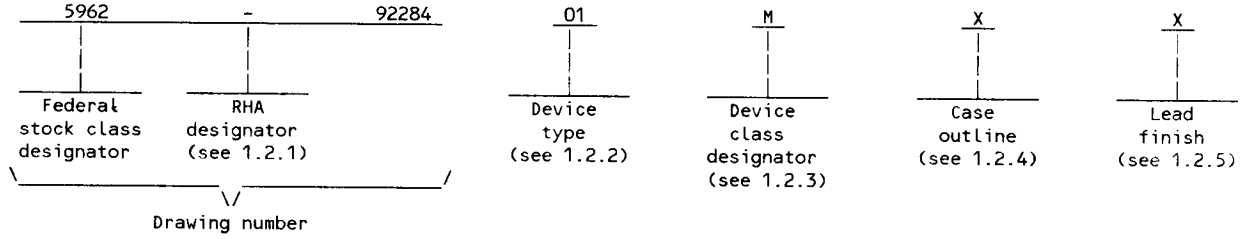
5962-E067-93

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Speed
01	29000	32 Bit streamlined instruction processor	20 MHz
02	29000	32 Bit streamlined instruction processor	16 MHz

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Z	CMGA9-P169	169	Pin grid array

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage range	+4.5 V dc to +5.5 V dc
Input voltage range	-0.5 to V_{CC} +0.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) (2/)	3.3 W
Lead temperature (soldering, 10 seconds)	300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case Z	See MIL-STD-1835
Junction temperature (T_J)	131.6°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Minimum high-level input voltage (V_{IH})	2.0 V dc
Maximum low-level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Maximum low-level SYSCLK input voltage ($V_{ILSYSCLK}$)	+0.8 V dc
Minimum high-level SYSCLK input voltage ($V_{IHSYSCLK}$)	V_{CC} - 0.8 V dc

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 3/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Must withstand the added P_D due to short circuit test (I_{OS})
3/ Values will be added when they become available.

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Low level input voltage 1/ 2/	V_{IL}	V_{CC} = 4.5 V	1, 2, 3	All 3/	-0.5 4/	0.8	V
High level input voltage 1/ 2/	V_{IH}	V_{CC} = 5.5 V			2.0	V_{CC}+0.5 4/	V
Low level INCLK input voltage	$V_{ILINCLK}$	V_{CC} = 4.5 V			-0.5 2/ 4/	0.8	V
High level INCLK input voltage	$V_{IHINCLK}$	V_{CC} = 5.5 V			2.0	V_{CC}+0.5 2/ 4/	V
Low level SYSCLK input voltage	$V_{ILSYSCLK}$	V_{CC} = 4.5 V			-0.5 4/ 5/	0.8	V
High level SYSCLK input voltage	$V_{IHSYSCLK}$	V_{CC} = 5.5 V			V_{CC}-0.8	V_{CC}+0.5 4/ 5/	V
Low level output voltage 6/	V_{OL}	I_{OL} = 3.2 mA V_{CC} = 4.5 V				0.45 2/	V
High level output voltage 6/	V_{OH}	I_{OH} = -400 µA V_{CC} = 4.5 V			2.4 2/		V
Low level SYSCLK output voltage	V_{OLC}	I_{OLC} = 20 mA V_{CC} = 4.5 V				0.6 2/	V
High level SYSCLK output voltage	V_{OHC}	I_{OHC} = 20 mA V_{CC} = 4.5 V			V_{CC}-0.6 2/		V
Input leakage current	I_{IL} 7/	V_{CC} = 5.5 V $0.45\ V \le V_{IN} \le V_{CC}$-0.45 V	1, 2, 3	All	-10	10	uA
Output leakage current	I_{OL} 7/	V_{CC} = 5.5 V $0.45\ V \le V_{IN} \le V_{CC}$-0.45 V			-10	10	uA
Operating power supply current 8/	I_{CCOP}	V_{CC} = 5.5 V				25	mA/MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
SYSCLK GND short circuit current	I_{OSGND}	V_{CC} = 5.0 V	1, 2, 3	All	100 4/		mA
SYSCLK V_{CC} short circuit current	I_{OSVCC}	V_{CC} = 5.0 V			100 4/		mA
Input capacitance	C_{IN}	f = 1 MHz See 4.4.1c	4 9/			15	pf
INCLK Input capacitance	C_{INCLK}					20	pf
SYSCLK capacitance	C_{SYSCLK}					90	pf
Output capacitance	C_{OUT}					20	pf
I/O Pin capacitance	$C_{I/O}$					20	pf
Functional test		See 4.4.1b	7, 8				

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroup	Device type	Limits Min	Limits Max	Unit
System clock (SYSCLK) period (T)	1	$SYSCLK_1$	10/ 11/ 12/	9,10, 11	01	50	125	ns
					02	60	125	ns
SYSCLK at 1.5 V to $\overline{SYSCLK}$ at 1.5 V when used as an output	1A	$SYSCLK_2$			01	0.5T-1	0.5T+1	ns
					02	0.5T-2	0.5T+2	ns
SYSCLK high time when used as an input	2	$SYSCLK_3$			01	22		ns
					02	27		ns
SYSCLK low time when used as an input	3	$SYSCLK_4$			01	19		ns
					02	22		ns
SYSCLK rise time 13/	4	$SYSCLK_5$			All		5 4/	ns
SYSCLK fall time 13/	5	$SYSCLK_6$			All		5 4/	ns
Synchronous SYSCLK 14/ output valid delay	6	$SYSCLK_7$	10/ 11/ 12/	9,10,11	All	0	16 15/	ns
Synchronous SYSCLK output valid delay for D_{31}-D_0	6A	$SYSCLK_9$	10/ 11/ 12/	9,10,11	All	0	20 15/	ns
Three-state synchronous SYSCLK output invalid delay 4/ 16/ 17/	7	$SYSCLK_{11}$	10/ 11/ 12/	9,10, 11	All	0	30	ns
Synchronous $\overline{SYSCLK}$ output valid delay 18/	8	$SYSCLK_{12}$	10/ 11/ 12/	9,10,11	All	0	16 15/	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroup	Device type	Limits		Unit
						Min	Max	
Three-state synchronous SYSCLK output invalid delay 4/ 17/	8A	$SYSCLK_{14}$	10/ 11/ 12/	9,10, 11	All	0	30	ns
Synchronous input setup time 19/	9	t_{S1}	10/ 11/ 12/	9,10, 11	All	15		ns
Synchronous input setup time for D_{31}-D_0, I_{31}-I_0	9A	t_{S2}	10/ 11/ 12/		All	8		ns
Synchronous input setup time for DRDY	9B	t_{S3}	10/ 11/ 12/		All	16		ns
Synchronous input hold time 20/	10	t_{H1}	10/ 11/ 12/	9,10, 11	All	2		ns
Asynchronous input minimum pulse width 21/	11	t_{PW1}		9,10, 11	All	T+10 4/		ns
INCLK Period	12	$INCLK_1$		9,10, 11	01	25	62.5	ns
					02	30	62.5	
INCLK to SYSCLK delay	12A	$INCLK_2$			01	2	12	ns
					02	2	15	
INCLK to $\overline{SYSCLK}$ delay	12B	$INCLK_3$			01	2	12	ns
					02	2	15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroup	Device type	Limits Min	Limits Max	Unit
INCLK LOW time	13	$INCLK_4$	10/ 11/ 12/	9,10, 11	01	10		ns
					02	12		
INCLK HIGH time	14	$INCLK_5$			01	10		ns
					02	12		
INCLK Rise Time 4/	15	$INCLK_6$		9,10, 11	All		5	ns
INCLK Fall Time 4/	16	$INCLK_7$		9,10, 11	All		5	ns
INCLK to deassertion of $\overline{RESET}$ (for phase synchronization of SYSCLK) 4/	17	$INCLK_8$	10/ 11/ 12/	9,10, 11	All	0	5	ns
$\overline{WARN}$ synchronous deassertion hold minimum pulse width	18	t_{PW2}		9,10, 11	All	4T		ns
$\overline{BINV}$ Synchronous output valid delay from SYSCLK	19	$BINV_1$	10/ 11/ 12/	9,10,11	01	0	8 15/	ns
					02	0	9 15/	ns
Three-state synchronous SYSCLK output invalid delay for D_{31}-D_0 4/ 17/	20	$SYSCLK_{15}$	10/ 11/ 12/	9,10, 11	All	0	25	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ All inputs except SYSCLK and INCLK.

2/ Verified at T12 max.

3/ All inputs/outputs are TTL compatible for V_{IH}, V_{IL}, V_{OH} and V_{OL} unless otherwise noted.

4/ This parameter limit is not 100% tested but guaranteed by characterization.

5/ Verified at T1 max.

6/ All outputs except SYSCLK.

7/ Outputs floating; holding $\overline{TEST}$ active with externally supplied SYSCLK at 100 KHz.

8/ Outputs floating; holding $\overline{RESET}$ active with externally supplied SYSCLK.

9/ Refer to 4.4.1c.

10/ All output timing specifications are for $C_L \leq 80$ pF of loading.

11/ All inputs are driven at 0 V for V_{IL} and 3.0 V for V_{IH}, V_{CC} = 4.5 V.

12/ See figure 3 for switching test and timing waveforms circuit.

13/ SYSCLK rise and fall times measured between 0.8 V and (V_{CC}-1.0 V).

14/ Synchronous outputs relative to SYSCLK rising edge are: A_{31}-A_0, $\overline{BGRT}$, R/$\overline{W}$ SUP/$\overline{US}$, $\overline{LOCK}$, $MPGM_1$-$MPGM_0$, $\overline{IREQ}$, IREQT, $\overline{PIA}$, $\overline{DREQ}$, $DREQT_1$-$DREQT_0$, $\overline{PDA}$, OPT_2-OPT_0, $STAT_2$-$STAT_0$ and MSERR.

15/ The max limit is not tested at -55°C and 25°C, but guaranteed by +125°C testing.

16/ Three-state synchronous outputs relative to SYSCLK rising edge are: A_{31}-A_0, R/$\overline{W}$, SUP/$\overline{US}$, $\overline{LOCK}$, $MPGM_1$-$MPGM_0$, $\overline{IREQ}$, IREQT, $\overline{PIA}$, $\overline{DREQ}$, $DREQT_1$-$DREQT_0$, $\overline{PDA}$, OPT_2-OPT_0.

17/ Three-state output inactive test load. Three-state synchronous output invalid delay is measured as the time to a ±500 mV change from prior output level.

18/ Synchronous outputs relative to SYSCLK falling edge: $\overline{IBREQ}$, $\overline{DBREQ}$.

19/ Synchronous inputs are: $\overline{BREQ}$, $\overline{PEN}$, $\overline{IRDY}$, $\overline{IERR}$, $\overline{IBACK}$, $\overline{IDERR}$, $\overline{DBACK}$, $\overline{CDA}$.

20/ Synchronous inputs are: $\overline{BREQ}$, $\overline{PEN}$, $\overline{IRDY}$, $\overline{IERR}$, $\overline{IBACK}$, $\overline{DERR}$, $\overline{DBACK}$, $\overline{CDA}$, I_{31}-I_0, $\overline{DRDY}$, and D_{31}-D_0.

21/ Asynchronous inputs are: $\overline{WARN}$, $\overline{INTR3-0}$, $\overline{TRAP3-0}$, CNTL1-0 and $\overline{TEST}$.

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
A-1	GND	C-10	GND	J-16	A_{16}	R-12	$STAT_2$
A-2	I_1	C-11	GND	J-17	A_{14}	R-13	GND
A-3	I_0	C-12	D_{22}	K-1	I_{28}	R-14	OPT_1
A-4	D_2	C-13	D_{26}	K-2	I_{25}	R-15	A_2
A-5	D_4	C-14	V_{CC}	K-3	GND	R-16	A_6
A-6	D_6	C-15	D_{30}	K-15	V_{CC}	R-17	A_7
A-7	D_9	C-16	D_{31}	K-16	A_{12}	T-1	INCLK
A-8	D_{11}	C-17	A_{29}	K-17	A_{13}	T-2	$\overline{BREQ}$
A-9	D_{12}	D-1	I_{11}	L-1	I_{27}	T-3	$\overline{DERR}$
A-10	D_{14}	D-2	I_{10}	L-2	I_{28}	T-4	$\overline{IRDY}$
A-11	D_{16}	D-3	I_7	L-3	V_{CC}	T-5	$\overline{WARN}$
A-12	D_{18}	D-4	PIN169	L-15	V_{CC}	T-6	$\overline{INTR_2}$
A-13	D_{20}	D-15	A_{31}	L-16	A_{10}	T-7	$\overline{INTR_0}$
A-14	D_{21}	D-16	A_{28}	L-17	A_{11}	T-8	$\overline{BINV}$
A-15	D_{25}	D-17	A_{26}	M-1	I_{29}	T-9	$\overline{BGRT}$
A-16	D_{27}	E-1	I_{13}	M-2	I_{30}	T-10	$\overline{DREQ}$
A-16	GND	E-2	I_{12}	M-3	GND	T-11	$\overline{LOCK}$
B-1	I_6	E-3	V_{CC}	M-15	GND	T-12	MSERR
B-2	I_5	E-15	GND	M-16	A_0	T-13	$STAT_0$
B-3	I_3	E-16	A_{27}	M-17	A_1	T-14	SUP/$\overline{US}$
B-4	D_0	E-17	A_{23}	N-1	I_{31}	T-15	OPT_1
B-5	D_1	F-1	I_{16}	N-2	$\overline{TEST}$	T-16	A_3
B-6	D_5	F-2	I_{15}	N-3	SYSCLK	T-17	A_4
B-7	D_8	F-3	I_{14}	N-15	GND	U-1	GND
B-8	D_{10}	F-15	A_{25}	N-16	$MPGM_1$	U-2	$\overline{PEN}$
B-9	D_{13}	F-16	A_{24}	N-17	$MPGM_0$	U-3	$\overline{IERR}$
B-10	D_{15}	F-17	A_{21}	P-1	$CNTL_1$	U-4	$\overline{IBACK}$
B-11	D_{17}	G-1	I_{19}	P-2	$CNTL_0$	U-5	$\overline{INTR_3}$
B-12	D_{19}	G-2	I_{18}	P-3	PWRCLK	U-6	$\overline{INTR_1}$
B-13	D_{23}	G-3	I_{17}	P-15	A_5	U-7	$\overline{TRAP_0}$
B-14	D_{24}	G-15	A_{22}	P-16	A_8	U-8	$\overline{IBREQ}$
B-15	D_{28}	G-16	A_{20}	P-17	A_9	U-9	$\overline{IREQ}$
B-16	D_{29}	G-17	A_{19}	R-1	$\overline{RESET}$	U-10	$\overline{PIA}$
B-17	A_{30}	H-1	I_{20}	R-2	$\overline{CDA}$	U-11	R/$\overline{W}$
C-1	I_9	H-2	I_{22}	R-3	$\overline{DRDY}$	U-12	$\overline{DREQT_1}$
C-2	I_8	H-3	I_{21}	R-4	$\overline{DBACK}$	U-13	$\overline{DREQT_0}$
C-3	I_4	H-15	GND	R-5	GND	U-14	$STAT_1$
C-4	I_2	H-16	A_{18}	R-6	V_{CC}	U-15	IREQT
C-5	GND	H-17	A_{17}	R-7	$\overline{TRAP_1}$	U-16	OPT_2
C-6	D_3	J-1	I_{23}	R-8	GND	U-17	GND
C-7	D_7	J-2	I_{24}	R-9	$\overline{DBREQ}$		
C-8	V_{CC}	J-3	GND	R-10	$\overline{PDA}$		
C-9	V_{CC}	J-15	A_{15}	R-11	V_{CC}		

FIGURE 1. Terminal connections.

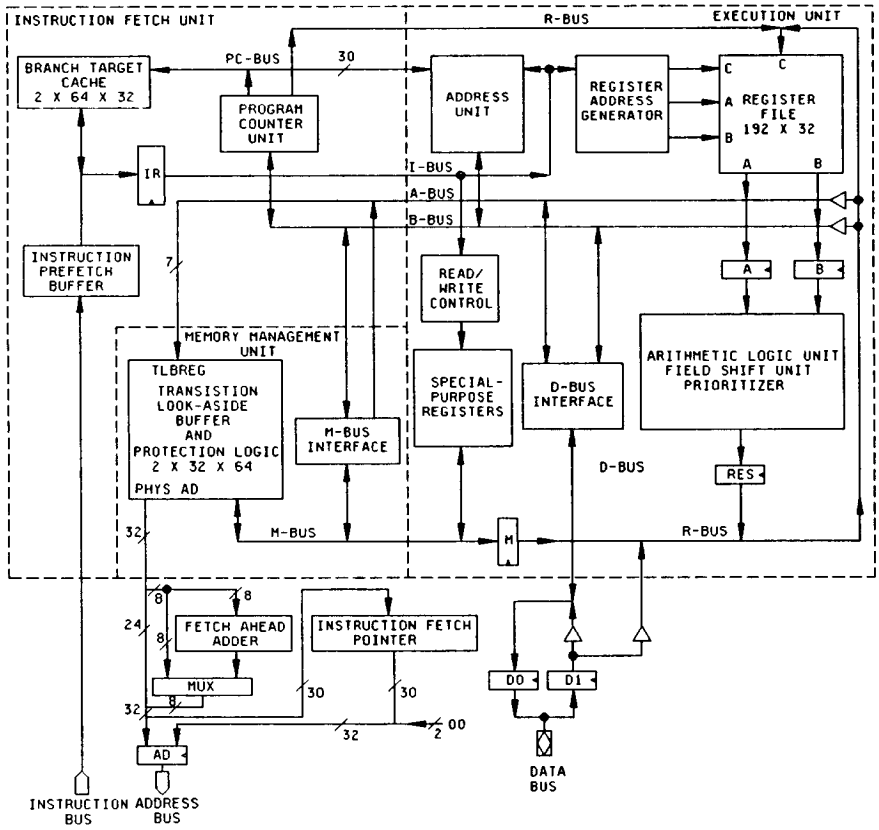


FIGURE 2. Block diagram.

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		REVISION LEVEL	SHEET 13

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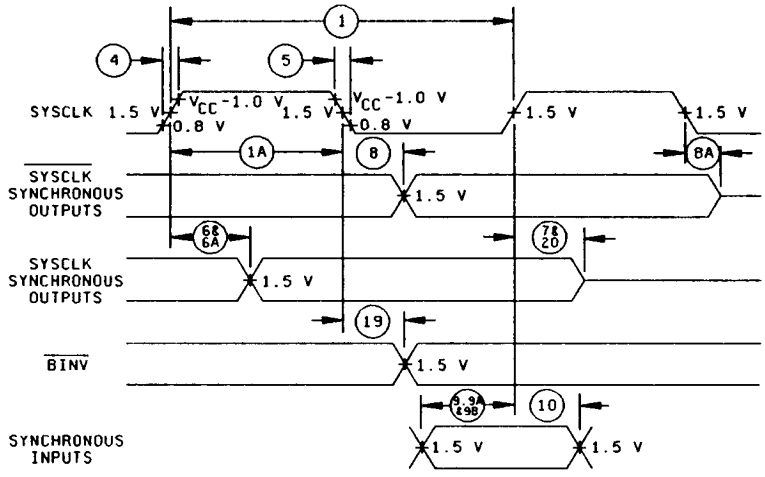
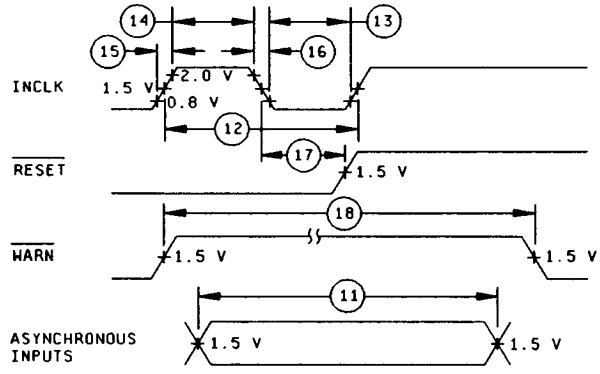
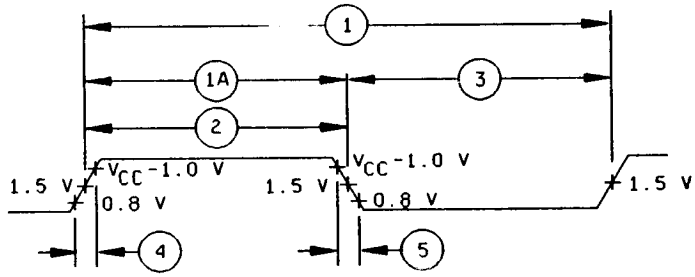


RELATIVE TO SYNCLK

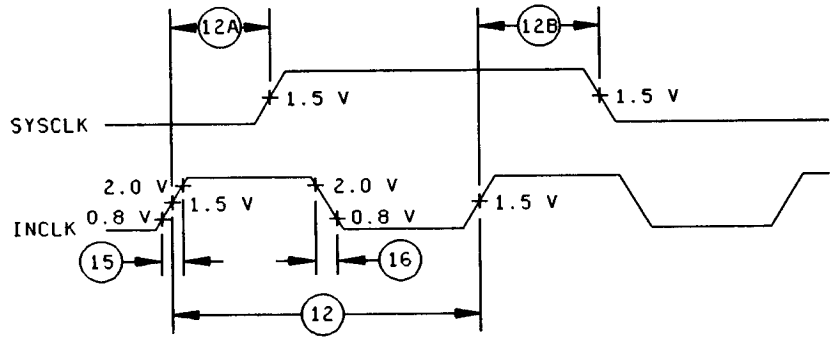


INCLK AND ASYNCHRONOUS INPUTS

FIGURE 3. Switching test and timing waveforms circuits.



SYSCLK DEFINITION



INCLK TO SYSCLK DELAY

FIGURE 3. Switching test and timing waveforms circuits - Continued.

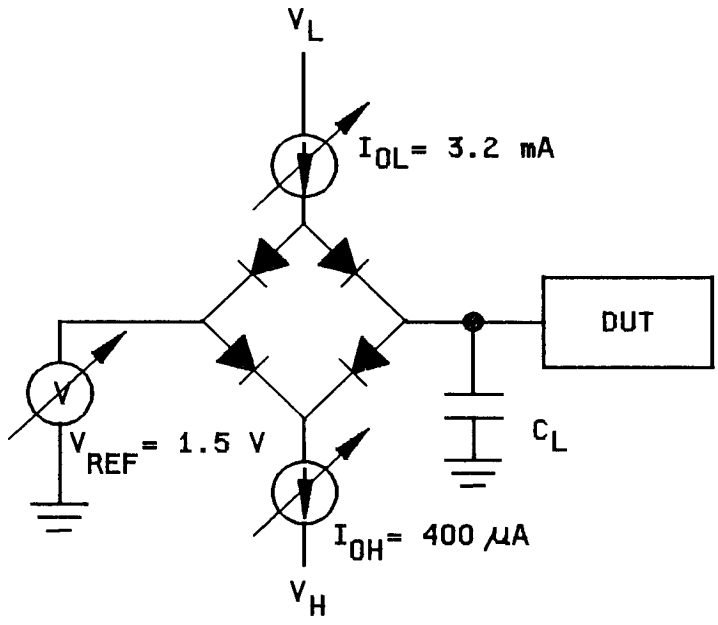


FIGURE 3. Switching test and timing waveforms circuits - Continued.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN}, C_{INCLK}, C_{SYSCLK}, C_{OUT}, $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is five devices with no failures, and all input and output terminals tested.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)			Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)					
Final electrical parameters (see 4.2)	1,2,3,7,8, 9,10,11 1/	1,2,3,7,8, 9,10,11 1/	1,2,3,7,8 9,10,11 2/	1,2,3,7,8, 9,10,11 1/	1,2,3,7,8, 9,10,11 2/
Group A test requirements (see 4.4)	1,2,3,4,7 8,9,10,11	1,2,3,4,7, 8,9,10,11	1,2,3,4,7 8,9,10,11	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11
Group B end-point electrical parameters (see 4.4)			1,2,3,7,8		
Group C end-point electrical parameters (see 4.4)	1,2,3,7,8	1,2,3,7,8		1,2,3,7,8	1,2,3,7,8
Group D end-point electrical parameters (see 4.4)	1,2,3,7,8	1,2,3,7,8	1,2,3,7,8	1,2,3,7,8	1,2,3,7,8
Group E end-point electrical parameters (see 4.4)					

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table II herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510 and MIL-STD-1331 and Table III.

TABLE III. Pin description.

Symbol	Name and function
A_{31}-A_0	Address Bus (three-state output, synchronous) The Address Bus transfers the byte address for all accesses except burst-mode accesses. For burst-mode accesses, it transfers the address for the first access in the sequence.
$\overline{BGRT}$	Bus Grant (output, synchronous) This output signals to an external master that the processor is relinquishing control of the channel in response to BREQ .
$\overline{BINV}$	Bus Invalid (output, synchronous) This output indicates that the address bus and related controls are invalid. It defines an idle cycle for the channel.
$\overline{BREQ}$	Bus Request (input, synchronous) This input allows other masters to arbitrate for control of the processor channel.
$\overline{CDA}$	Coprocessor Data Accept (input, synchronous) This signal allows the coprocessor to indicate the acceptance of operands or operation codes. For transfers to the coprocessor, the processor does not expect a DRDY response; an active level on CDA performs the function normally performed by DRDY. CDA may be active whene[illegible] the coprocessor is able to accept transfers.
$CNTL_1$-$CNTL_0$	CPU Control (input, asynchronous) These inputs control the processor mode:

$CNTL_1$	$CNTL_2$	Mode
0	0	Load Test Instruction
0	1	Step
1	0	Halt
1	1	Normal

D_{31}-D_0	Data Bus (bidirectional, synchronous) The Data Bus transfers data to and from the processor for load and store operations.		

Symbol	Name and function
$\overline{\text{DBACK}}$	Data Burst Acknowledge (input, synchronous) This input is active whenever a burst-mode data access has been established. It may be active even though no data are currently being accessed.
$\overline{\text{DBREQ}}$	Data Burst Request (three-state output, synchronous) This signal is used to establish a burst-mode data access and to request data transfers during a burst-mode data access. DBREQ may be active even though the address bus is being used for an instruction access. This signal becomes valid late in the cycle, with respect to DREQ.
$\overline{\text{DERR}}$	Data Error (input, synchronous) This input indicates that an error occurred during the current data access. For a load, the processor ignores the content of the data bus. For a store, the access is terminated. In either case, a Data Access Exception trap occurs. The processor ignores this signal if there is no pending data access.
$\overline{\text{DRDY}}$	Data Ready (input, synchronous) For loads, this input indicates that valid data is on the data bus. For stores, it indicates that the access is complete, and that data need no longer be driven on the data bus. The processor ignores this signal if there is no pending data access.
$\overline{\text{DREQ}}$	Data Request (three-state output, synchronous) This signal requests a data access. When it is active, the address for the access appears on the address bus.
DREQT_1-DREQT_0	Data Request Type (three-state output, synchronous) These signals specify the address space of a data access, as follows (the value "x" is a "don't care"): DREQT_1 / DREQT_0 / Meaning 0 / 0 / Instruction/data memory access 0 / 1 / Input/output access 1 / x / Coprocessor transfer An interrupt/trap vector request is indicated as a data-memory read. If required, the system can identify the vector fetch by the STAT_2-STAT_0 outputs. DREQT_1-DREQT_0 are valid only when DREQ is active.

Symbol	Name and function
I_{31}-I_0	Instruction Bus (input, synchronous) The instruction Bus transfers instructions to the processor.
$\overline{IBACK}$	Instruction Burst Acknowledge (input, synchronous) This input is active whenever a burst-mode instruction access has been established. It may be active even though no instructions are currently being accessed.
$\overline{IBREQ}$	Instruction Burst Request (three-state output, synchronous) This signal is used to establish a burst-mode instruction access and to request instruction transfers during a burst-mode instruction access. IBREQ may be active even though the address bus is being used for a data access. This signal becomes valid late in the cycle with respect to IREQ.
$\overline{IERR}$	Instruction Error (input, synchronous) This indicates that an error occurred during the current instruction access. The processor ignores the content of the instruction bus, and an Instruction Access Exception trap occurs if the processor attempts to execute the invalid instruction. The processor ignores this signal if there is no pending instruction access.
INCLK	Input Clock (input) When the processor generates the clock for the system, this is an oscillator input to the processor at twice the processor's operating frequency. In systems where the clock is not generated by the processor, this signal must be tied High or Low, except in certain master/slave configurations.
$\overline{INTR_3}$-$\overline{INTR_0}$	Interrupt Request (input, asynchronous) These inputs generate prioritized interrupt requests. The interrupt caused by $\overline{INTR_0}$ has the highest priority, and the interrupt caused by $\overline{INTR_3}$ has the lowest priority. The interrupt requests are masked in prioritized order by the Interrupt Mask field in the Current Processor Status Register.
IRDY	Instruction Ready (input, synchronous) This input indicates that a valid instruction is on the instruction bus. The processor ignores this signal if there is no pending instruction access.
$\overline{IREQ}$	Instruction Request (three-state output, synchronous) This signal requests an instruction access. When it is active, the address for the access appears on the address bus.

Symbol	Name and function
IREQT	Instruction Request Type (three-state output, synchronous) This signal specifies the address space of an instruction request when $\overline{\text{IREQ}}$ is active: IREQT — Meaning 0 — Instruction/data memory access 1 — Instruction read-only memory access
$\overline{\text{LOCK}}$	Lock (three-state output, synchronous) This output allows the implementation of various channel and device interlocks. It may be active only for the duration of an access, or active for an extended period of time under control of the Lock bit in the Current Processor Status.
$MPGM_1$-$MPGM_0$	MMU Programmable (three-state output, synchronous) These outputs reflect the value of two PGM bits in the Translation Look-Aside Buffer entry associated with the access. If no address translation is performed, these signals are both Low.
MSERR	Master/Slave Error (output, synchronous) This output shows the result of the comparison of processor outputs with the signals provided internally to the off-chip drivers. If there is a difference for any enabled driver, this line is asserted.
$\overline{\text{PDA}}$	Pipelined Data Access (Three-state Output, synchronous) If $\overline{\text{DREQ}}$ is not active, this output indicates that a data access is pipelined with another in-progress data access. The indicated access cannot be completed until the first access is complete. The completion of the first access is signaled by the assertion of DREQ.
$\overline{\text{PEN}}$	Pipeline Enable (input, synchronous) This signal allows devices that can support pipelined accesses (i.e., that have input latches for the address and required controls) to signal that a second access may begin while the first is being completed.
PIN169	Alignment Pin In the PGA package this pin is used to indicate proper pin-alignment of the device and is used by the ADAPT29K to communicate its presence to the system.

Symbol	Name and function
OPT_2-OPT_0	Option Control (three-state output, synchronous) These outputs reflect the value of bits 18-16 of the load or store instruction that begins an access. Bit 18 of the instruction is reflected on OPT_2, bit 17 on OPT_1, and bit 16 on OPT_0. The standard definitions of these signals (based on DREQT) are as follows (the value "x" is a "don't care"): $DREQT_1$ $DREQT_0$ OPT_2 OPT_1 OPT_0 Meaning 0 x 0 0 0 Word-length access 0 x 0 0 1 Byte access 0 x 0 1 0 Half-word access 0 0 1 0 0 Instruction ROM access (as data) 0 0 1 0 1 Cache control 0 0 1 1 0 ADAPT29K accesses -all others- Reserved During an interrupt/trap vector fetch, the OPT_2-OPT_0 signals indicate a word-length access (000). Also, the system should return an entire aligned word for a read, regardless of the indicated data length. The device does not explicitly prevent a store to the instruction ROM. OPT_3-OPT_0 are valid only when DREQ is active.
$\overline{PIA}$	Pipelined Instruction Access (three-state output, synchronous) If $\overline{IREQ}$ is not active, this output indicates that an instruction access is pipelined with another in-progress instruction access. The indicated access cannot be completed until the first access is complete. The completion of the first access is signaled by the assertion of IREQ.
R/$\overline{W}$	Read/Write (three-state output, synchronous) This signal indicates whether data is being transferred from the processor to the system, or from the system to the processor. R/$\overline{W}$ is valid only when the address bus is valid. R/W will be High when $\overline{IREQ}$ is active.
$\overline{RESET}$	Reset (input, asynchronous) This input places the processor in the Reset mode.
PWRCLK	Power Supply for SYSCLK Driver This pin is a power supply for the SYSCLK output driver. It isolates the SYSCLK driver, and is used to determine whether or not the device generates the clock for the system. If power (+5 volts) is applied to this pin, the device generates a clock on the SYSCLK output. If this pin is grounded, the the device accepts a clock generated by the system on the SYSCLK input.

Symbol	Name and function
$STAT_2$-$STAT_0$	CPU Status (output, synchronous) These outputs indicate the state of the processor's execution stage on the previous cycle. They are encoded as follows:

$STAT_2$	$STAT_1$	$STAT_0$	Condition
0	0	0	Halt or Step Modes
0	0	1	Pipeline Hold Mode
0	1	0	Load Test Instruction Mode, Halt/Freeze
0	1	1	Wait Mode
1	0	0	Interrupt Return
1	0	1	Taking Interrupt or Trap
1	1	0	Non-sequential Instruction Fetch
1	1	1	Executing Mode

Symbol	Name and function
SUP/$\overline{US}$	Supervisor/User Mode (three-state output, synchronous) This output indicates the program mode for an access. The processor does not relinquish the channel (in response to $\overline{BREQ}$) when $\overline{LOCK}$ is active.
SYSCLK	System Clock (bidirectional) This is either a clock output with a frequency that is half that of INCLK, or an input from an external clock generator at the processor's operating frequency
$\overline{TEST}$	Test Mode (input, asynchronous) When this input is active, the processor is in Test mode. All outputs and bidirectional lines, except MSERR, are forced to the high-impedance state.
$\overline{TRAP}_1$-$\overline{TRAP}_0$	Trap Request (input, asynchronous) These inputs generate prioritized trap requests. The trap caused by $\overline{TRAP}_0$ has the highest priority. These trap requests are disabled by the DA bit of the Current Processor Status Register.
$\overline{WARN}$	Warn (input, asynchronous, edge-sensitive) A high-to-low transition on this input causes a non-maskable $\overline{WARN}$ trap to occur. This trap bypasses the normal trap vector fetch sequence, and is useful in situations where the vector fetch may not work (e.g., when data memory is faulty). The following pins are not signal pins, but are named in device documentation because of their special role in the processor and system.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.