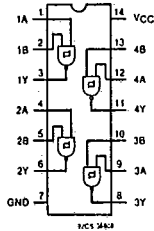


CD54/74HC132 CD54/74HCT132

HARRIS SEMICONDUCTOR 27E D 4302271 0017572 3 HAS

High-Speed CMOS Logic

T-51-21-00



FUNCTIONAL DIAGRAM AND
TERMINAL ASSIGNMENT

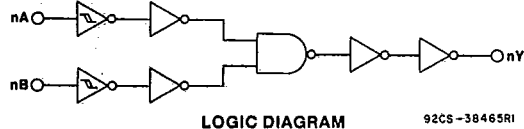
Quad 2-Input NAND Schmitt Trigger

Type Features:

- Unlimited input rise and fall times
- Exceptionally high noise immunity

The RCA-CD54/74HC132 and CD54/74HCT132 each contain four 2-input NAND Schmitt Triggers in one package.

The CD54HC132 and CD54HCT132 are supplied in 14-lead ceramic dual-in-line packages (F suffix). The CD74HC132 and CD74HCT132 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both devices are also available in chip form (H suffix).



LOGIC DIAGRAM

92CS-38465RI

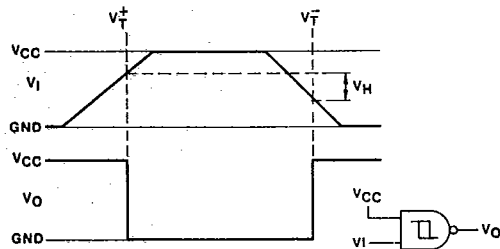
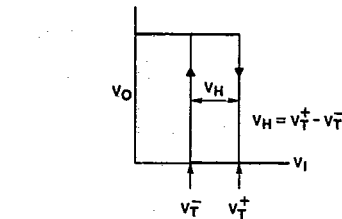


Fig. 1 - Hysteresis definition, characteristic, and test setup.

Family Features:

- Fanout (Over Temperature Range):
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC/HCT: -40 to +85°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High Noise Immunity:
 $N_{IL} = 37\%$, $N_{IH} = 51\%$ of V_{CC} ; @ $V_{CC} = 5$ V
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $V_{IL} = 0.8$ V Max., $V_{IH} = 2$ V Min.
CMOS Input Compatibility
 $I_L \leq 1 \mu A$ @ V_{OL} , V_{OH}

TRUTH TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = High level
L = Low level

92CM-38466

CD54/74HC132 CD54/74HCT132

HARRIS SEMICONDUCTOR 27E D 4302271 0017573 5 HAS

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V _{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I _{IK} (FOR V _i < -0.5 V OR V _i > V _{CC} + 0.5V)	±20mA
DC OUTPUT DIODE CURRENT, I _{OK} (FOR V _o < -0.5 V OR V _o > V _{CC} + 0.5V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I _o) (FOR -0.5 V < V _o < V _{CC} + 0.5V)	±25mA
DC V _{CC} OR GROUND CURRENT (I _{CC})	±50mA
POWER DISSIPATION PER PACKAGE (P _D):	
For T _A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T _A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T _A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T _A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T _A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T _{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)	
with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T _A = Full Package-Temperature Range) V _{CC} .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V _i , V _o	0	V _{CC}	V
Operating Temperature T _A :			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t _r , t _f			
at 2 V	0	Unlimited	ns
at 4.5 V	0	Unlimited	ns
at 6 V	0	Unlimited	ns

*Unless otherwise specified, all voltages are referenced to Ground.

T-51-21

— Technical Data

CD54/74HC132
CD54/74HCT132

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC132/CD54HC132										CD74HCT132/CD54HCT132										UNITS
	TEST CONDITIONS			74HC/54HC TYPE		74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE		74HCT TYPE		54HCT TYPE					
	V _I V	I _O mA	V _{CC} V	+25°C		-40/ +85°C		-55/ +125°C		V _I V	V _{CC} V	+25°C		-40/ +85°C		-55/ +125°C					
				Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max				
Input Switch Points	V _T ⁺		2	0.7	1.5	0.7	1.5	0.7	1.5			—	—	—	—	—	—	V			
			4.5	1.7	3.15	1.7	3.15	1.7	3.15		4.5	1.2	1.9	1.2	1.9	1.2	1.9				
			6	2.1	4.2	2.1	4.2	2.1	4.2		5.5	1.4	2.1	1.4	2.1	1.4	2.1				
	V _T ⁻		2	0.3	1	0.3	1	0.3	1			—	—	—	—	—	—	V			
			4.5	0.9	2.2	0.9	2.2	0.9	2.2		4.5	0.5	1.2	0.5	1.2	0.5	1.2				
			6	1.2	3	1.2	3	1.2	3		5.5	0.6	1.4	0.6	1.4	0.6	1.4				
	V _H		2	0.2	1	0.2	1	0.2	1			—	—	—	—	—	—	V			
			4.5	0.4	1.4	0.4	1.4	0.4	1.4		4.5	0.4	1.4	0.4	1.4	0.4	1.4				
			6	0.6	1.6	0.6	1.6	0.6	1.6		5.5	0.4	1.5	0.4	1.5	0.4	1.5				
High-Level Output Voltage	V _T ⁻	-0.02	2	1.9	—	1.9	—	1.9	—	V _T ⁻		—	—	—	—	—	—	V			
V _{OH}	or		4.5	4.4	—	4.4	—	4.4	—	or	4.5	4.4	—	4.4	—	4.4	—				
CMOS Loads	V _T ⁺		6	5.9	—	5.9	—	5.9	—	V _T ⁺		—	—	—	—	—	—				
TTL Loads	V _T ⁻		—	—	—	—	—	—	—	V _T ⁻		—	—	—	—	—	—	V			
	or	-4	4.5	3.98	—	3.84	—	3.7	—	or	4.5	3.98	—	3.84	—	3.7	—				
	V _T ⁺	-5.2	6	5.48	—	5.34	—	5.2	—	V _T ⁺		—	—	—	—	—	—				
Low-Level Output Voltage	V _T ⁻	0.02	2	—	0.1	—	0.1	—	0.1	V _T ⁻		—	—	—	—	—	—	V			
V _{OL}	or		4.5	—	0.1	—	0.1	—	0.1	—	or	4.5	—	0.1	—	0.1	—		0.1		
CMOS Loads	V _T ⁺		6	—	0.1	—	0.1	—	0.1	—	V _T ⁺		—	—	—	—	—		—		
TTL Loads	V _T ⁻		—	—	—	—	—	—	—	V _T ⁻		—	—	—	—	—	—	V			
	or	4	4.5	—	0.26	—	0.33	—	0.4	or	4.5	—	0.26	—	0.33	—	0.4				
	V _T ⁺	5.2	6	—	0.26	—	0.33	—	0.4	V _T ⁺		—	—	—	—	—	—				
Input Leakage Current	V _{CC} or Gnd		6	—	±0.1	—	±1	—	±1	Any Voltage Between V _{CC} and Gnd	5.5	—	±0.1	—	±1	—	±1	μA			
Quiescent Device Current	V _{CC} or Gnd	0	6	—	2	—	20	—	40	V _{CC} or Gnd	5.5	—	2	—	20	—	40	μA			
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI _{CC} *										V _{CC} -2.1	4.5 to 5.5	Min	Typ	Max			490	μA			

*For dual-supply systems theoretical worst case ($V_I = 2.4$ V, $V_{CC} = 5.5$ V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS*
nA, nB	0.6

*Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC132 CD54/74HCT132

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 6\text{ ns}$)

CHARACTERISTIC	C_L (pF)	TYPICAL		UNITS
		HC	HCT	
Propagation Delay A, B to Y t_{PLH} t_{PHL}	15	10	13	ns
Power Dissipation Capacitance C_{PD}^*	—	30	30	pF

* C_{PD} is used to determine the dynamic power consumption, per gate.

$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where:

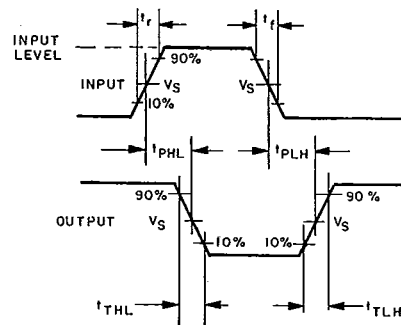
f_i = input frequency

C_L = output load capacitance

V_{CC} = supply voltage

SWITCHING CHARACTERISTICS ($C_L = 50\text{ pF}$, Input $t_r, t_f = 6\text{ ns}$)

CHARACTERISTIC		TEST CONDITIONS V _{CC} (V)	+25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay A, B to Y	t _{PLH} t _{PHL}	2	—	125	—	—	—	156	—	—	—	188	—	—	ns
		4.5	—	25	—	33	—	31	—	41	—	38	—	50	
		6	—	21	—	—	—	27	—	—	—	32	—	—	
Output Transition Time	t _{TLH} t _{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C _i	—	—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3V
V_S	50% V_{CC}	1.3V

92CS-36948R1

Fig. 2 - Transition times and propagation delay times.