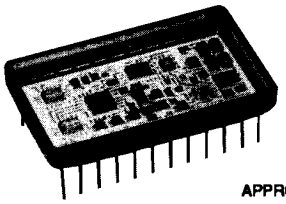
DDC
ILC DATA DEVICE CORPORATION

DAC-02320

12 BIT DEGLITCHED D/A CONVERTER
15 MHz Update Rate; Voltage Output



APPROX.
ACTUAL SIZE

PRELIMINARY

DESCRIPTION

Continuing DDC's series of leadership display DACs, the DAC-02320 is a 12 bit, 15 MHz update rate, deglitched hybrid D/A converter with a low impedance voltage output. Its input registers, precision dc voltage reference, and track/hold deglitcher output provide the complete solution to low noise DAC requirements. Packaged in a small 24 pin DDIP, the DAC-02320 operates over the full -55°C to +125°C temperature range and military processing is available (consult factory).

DAC-02320 is available in linearity grades of 13 bits (±0.006%) and 12 bits (±0.012%). It can be pin programmed for 3 different output voltage ranges. Offset and gain errors can be trimmed to zero with external potentiometers.

APPLICATIONS

With its 12 bit resolution, low glitch voltage output, and small hermetic package, the DAC-02320 is ideal for the most demanding low noise DAC requirements. It is particularly well suited for applications such as vector-stroke CRT displays, waveform generators, and automatic test equipment.

FEATURES

- *FULL FUNCTION:*
  INCLUDES INPUT REGISTERS AND TRACK/HOLD DEGLITCHER OUTPUT
- *HIGH SPEED:*
  15 MHz UPDATE RATE FOR SMALL STEP CHANGES
  200 NSEC SETTLING FOR F.S.
- *SMALL SIZE:*
  24 PIN DDIP HYBRID
- *WIDE OPERATING TEMPERATURE:*
  -55°C to +125°C

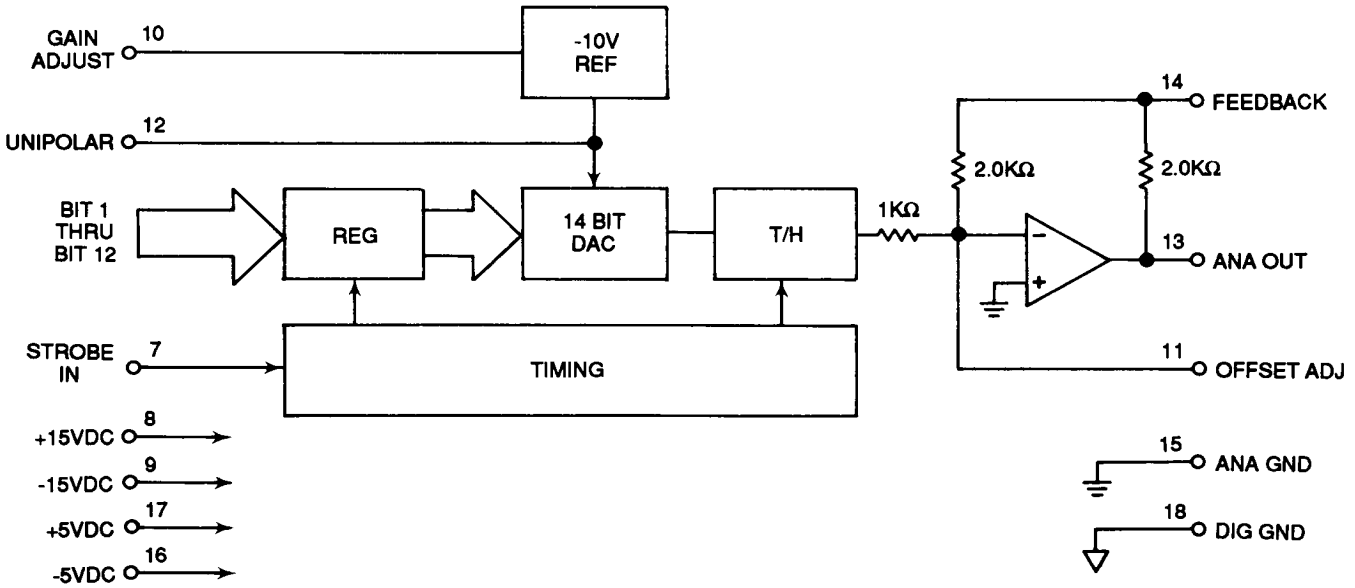


FIGURE 1. DAC-02320 BLOCK DIAGRAM

TABLE 1. DAC-02320 SPECIFICATIONS
Typical values at +25°C case temperature and nominal power supply voltages unless otherwise specified.

PARAMETER	UNITS	VALUES	
		13 BIT LIN	12 BIT LIN
RESOLUTION	Bits	12	12
ACCURACY			
Linearity Error	%FSR	±0.006 max	±0.012 max
Linearity Error Tempco	ppm FSR/°C	±1 max	±2 max
Gain Error(1)	%FSR	±0.1	±0.2
Gain Error Tempco	ppm FSR/°C	±25 max	±25max
Offset Error(1)	mV	±10	±20
Offset Error Tempco	ppm FSR/°C	±20 max	±20max
Monotonicity	Bits	13	12
DYNAMICS			
Settling Time to ±0.01% FSR			
±10V FS Change	nsec	200 max	
±5V FS Change	nsec	180 max	
1 LSB Change	nsec	50 max	
Slew Rate	V/usec	300 typ 200 min	
Glitch (2)			
Voltage	mVpp	10 typ 30 max	
Energy	mV ·nsec	250 typ 750 max	
DIGITAL INPUTS			
Logic Compatibility		TTL	
Data Inputs			
Logic "1" Level	V	+2.0 to +5	
Logic "0" Level	V	0 to +0.8	
Loading		1 standard LS TTL load	
Coding (negative output)		Offset Binary (Bipolar)Binary (Unipolar)	
Strobe Input (3)			
Logic "1" Level	V	+2.0 to 5	
Logic "0" Level	V	0 to + 0.8	
Loading		2 standard S TTL Loads	
Width	nsec	10 min	
ANALOG OUTPUT			
Voltage Ranges (4)	V	±10, ±5, 0 to +10	
Current Load	mA	±20min	
Impedance	ohm	0.1max	
POWER SUPPLIES			
+15 Volt Supply			
Tolerance	%	±5	
Max Voltage	V	+18 max	
Current Drain	mA	70 typ 100 max	
-15 Volt Supply			
Tolerance	%	±5	
Max Voltage	V	-18 max	
Current Drain	mA	35 typ 60 max	
+5 Volt Supply			
Tolerance	%	±10	
Max Voltage	V	+7 max	
Current Drain	mA	70 typ, 100 max	
-5 Volt Supply			
Tolerance	%	±5	
Max Voltage	V	-7 max	
Current Drain	mA	50 typ, 75 max	

TABLE 1. DAC-02320 SPECIFICATIONS (continued)

PARAMETER	UNITS	VALUES
TEMPERATURE RANGE		
Operating (Case)		
-1 Option	°C	-55 to +125
-3 Option	°C	0 to +70
Storage	°C	-65 to +150
PHYSICAL CHARACTERISTICS		
Package		24 pin DDIP hybrid
Size	in	1.300 x 0.790 x 0.210
	(mm)	(33.020 x 20.066 x 5.334)
Weight	oz (g)	0.4 (11.3)

NOTES:
(1) Gain and offset errors are trimmable to zero.
(2) Glitch is at 1 MHz update rate with a 5MHz filter.
(3) Strobe input is a positive pulse. Data transferred on rising edge.
(4) Output voltage ranges are pin programmable.

TECHNICAL DESCRIPTION

GENERAL

DAC-02320 is a complete self-contained deglitched D/A converter. As shown in the block diagram of Figure 1, it contains a precision DAC , input registers, a precision DC reference, a track/hold deglitcher output , and timing circuits. Its layout and compatible components provide the complete solution to low noise DAC design problems.

TIMING

Upon Application of a STROBE IN signal the input registers are updated and the DAC-02320 output is held constant. As shown in Figure 2, the rising edge of the STROBE IN signal latches the input data. Internal timing circuits generate a pulse which is used to open the T/H. The output remains constant since the op amp feedback capacitor is charged. During the hold mode interval of approximately 20 nanoseconds, the DAC is changing value and its output glitch is settling to zero. At the end of the hold interval the T/H returns to its original track mode level. The DAC-02320 then smoothly changes to its new output level. The track/hold has effectively "masked out " the DAC glitch.

EXTERNAL TRIMS

Factory adjustment of DAC-02320 offset and gain errors result in performance that is adequate for most applications. For more critical applications, DAC-02320 provides pins for external trimming offset and gain errors to zero. Figure 3 illustrates trim pot values and circuit connections for external trims.

OUTPUT VOLTAGE PROGRAMMING

DAC-02320 can be programmed for 3 different output voltage ranges by external jumpers between pins: For ±10V range, no external connections ar e required; for ±5V range , pin 14 must be jumpered to pin 13; or for 0 to +10V range , pin 14 must be jumpered to pin 13 and pin 11 must be jumpered to pin 12.

SETTLING

The DAC-02320 settling time of 200 nsec max for a F.S. input and 50 nsec max for a 1LSB change is based on one strobe to the D/A and waiting for settling to ±0.001% FSR. For F.S. settling of the analog output at an update rate of 15MHz the T/H duty cycle must be considered. Since the encode rate is 15MHz, there are a total of 66 ⅔ nsec between strobes. For 20 nsec of this period the T/H is in HOLD where, by definition, the slew rate is zero. The remaining TRACK time of 66 ⅔ nsec slews at 200 V/µsec min. As a consequence the settling time to 0.01% FSR for a full scale change at a 15 MHz update rate is 280 nsec because 4 periods of HOLD, each of 20nsec duration, are added to the overall settling time. The T/H duty cycle must be considered for calculation of settling time at high update frequencies.

LAYOUT PRECAUTIONS

To achieve the minimum noise performance available from the DAC-02320 deglitched D/A converter, high frequency layout considerations must be kept in mind when designing its printed circuit board. All analog conductor lengths must be used to keep ground impedances as low as possible. Digital inputs and analog output must be kept separated from each other to minimize crossstalk. Circuits connected to analog output must be kept close to the D/A converter package as possible. Circuit connections to the external adjustment (offset and gain) pins must be kept separate from digital lines to minimize noise coupling.

POWER SUPPLY DECOUPLING

Decoupling capacitors are recommended on each supply for minimum noise operation. Each of the power supplies should have a 1 microfarad or larger tantalum capacitor in parallel with a 0.01 microfarad ceramic capacitor. All capacitors must be mounted as close as possible to the hybrid package.

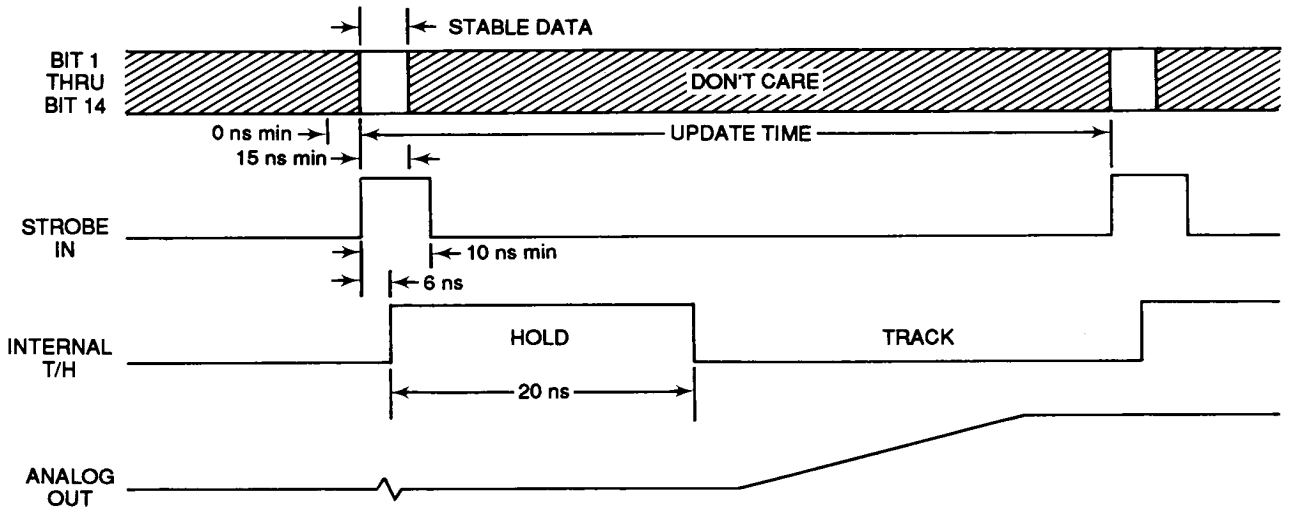


FIGURE 2. TIMING DIAGRAM

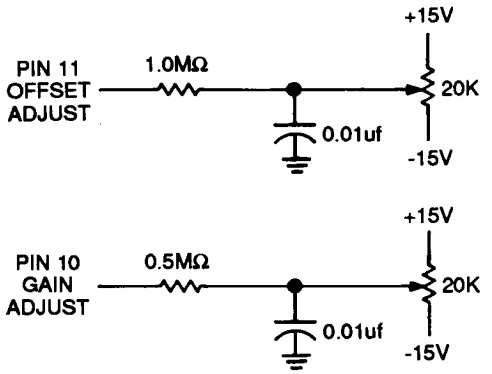
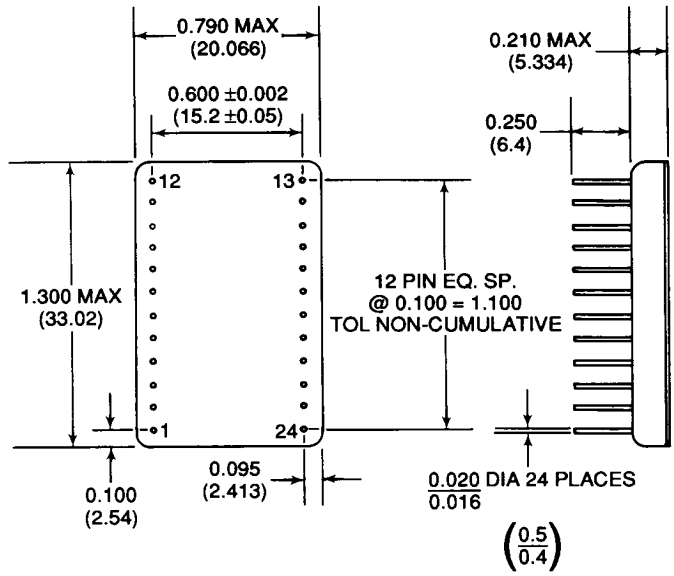


FIGURE 3. EXTERNAL TRIM CIRCUITS

TABLE 2. INPUT DATA CODING		
	OUTPUT VOLTAGE*	
INPUT DATA	BIPOLAR	UNIPOLAR
11 1111 1111 1111	+4.9994V	+9.9994V
10 0000 0000 0000	0	+5.0000V
01 1111 1111 1111	-0.0006V	+4.9994V
00 0000 0000 0000	-5.0000V	0

TABLE 3. PIN FUNCTION TABLE			
PIN	FUNCTION	PIN	FUNCTION
1	Bit 6	24	Bit 7
2	Bit 5	23	Bit 8
3	Bit 4	22	Bit 9
4	Bit 3	21	Bit 10
5	Bit 2	20	Bit 11
6	Bit 1 (MSB)	19	Bit 12 (LSB)
7	Strobe In	18	Digital Ground
8	+15V supply	17	+5V supply
9	-15V supply	16	-5V supply
10	Gain Adjust	15	Analog Ground
11	Offset Adjust	14	Feedback
12	Unipolar	13	V_{out}



Notes:
1. Dimensions shown are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead spacing dimensions apply at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.

FIGURE 4. DAC-02320 MECHANICAL OUTLINE (24 PIN DDIP)

ORDERING INFORMATION

DAC-02320-XXX

- Linearity Grade:
  - 3= 13 bit
  - 2= 12 bit
- Reliability Grade:
  - 0= Standard DDC procedures.
  - 1= Military processing available.*
  - 2= Military processing available but without QCI testing.*
- Operating Temperature Range (case):
  - 1= -55°C to +125°C
  - 3= 0°C to +70°C

*Consult factory for details.

Consult factory for evaluation board.

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