12:2, DIFFERENTIAL-TO-LVDS MULTIPLEXER

ICS854S202I-01

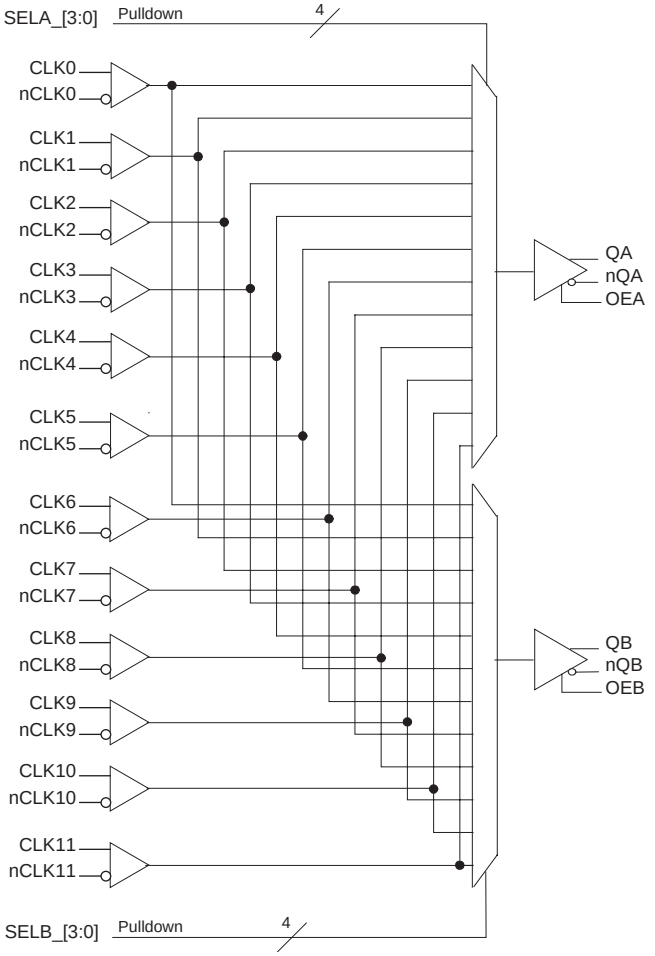
General Description

The ICS854S202I-01 is a 12:2 Differential-to-LVDS Clock Multiplexer which can operate up to 700MHz and is a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS854S202I-01 has 12 selectable differential clock inputs, any of which can be independently routed to either of the two LVDS outputs. The CLKx, nCLKx input pairs can accept LVPECL, LVDS, CML or SSTL levels. The fully differential architecture and low propagation delay make it ideal for use in clock distribution circuits.

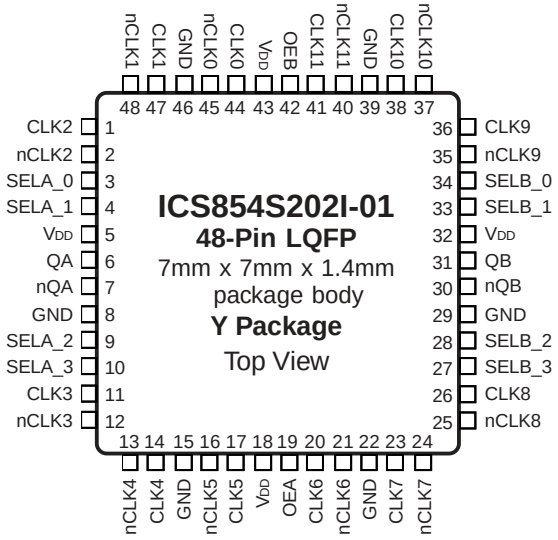
Features

- Two differential 2.5V LVDS clock outputs
- Twelve selectable differential clock inputs
- CLKx, nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, HSTL, SSTL, HCSL
- Maximum output frequency: >3GHz
- Propagation delay: 650ps (typical)
- Input skew: TBD
- Output skew: 25ps (typical)
- Part-to-part skew: TBD
- Additive phase jitter, RMS (12kHz – 20MHz): 0.16ps (typical)
- Full 2.5V operating supply mode
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS (CONTINUED ON NEXT PAGE)

Number	Name	Type		Description
1	CLK2	Input	Pullup	Non-inverting differential clock input.
2	nCLK2	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
3, 4, 9, 10	SELA_0, SELA_1, SELA_2, SELA_3	Input	Pulldown	Clock select pins for Bank A outputs. See Control Input Function Table. LVCMOS/LVTTL interface levels. See Table 3B.
5, 32, 43	V_{DD}	Power		Positive supply pins.
6, 7	QA, nQA	Output		Clock outputs. LVDS interface levels.
8, 15, 22, 29, 39, 46	GND	Power		Power supply ground.
11	CLK3	Input	Pullup	Non-inverting differential clock input.
12	nCLK3	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
13	nCLK4	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
14	CLK4	Input	Pullup	Non-inverting differential clock input.
16	nCLK5	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
17	CLK5	Input	Pullup	Non-inverting differential clock input.
18, 43	V_{DD}	Power		Positive supply pins.
19	OEA	Input	Pullup	Output enable pin. Controls enabling and disabling of QA/nQA outputs. LVCMOS/LVTTL internface levels.
20	CLK6	Input	Pullup	Non-inverting differential clock input.
21	nCLK6	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
23	CLK7	Input	Pullup	Non-inverting differential clock input.
24	nCLK7	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
25	nCLK8	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
26	CLK8	Input	Pullup	Non-inverting differential clock input.
27, 28, 33, 34	SELB_3, SELB_2, SELB_1, SELB_0	Input	Pulldown	Clock select pins for Bank B outputs. See Control Input Function Table. LVCMOS/LVTTL interface levels. See Table 3C.
30, 31	nQB, QB	Output		Clock outputs. LVDS interface levels.
35	nCLK9	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
36	CLK9	Input	Pullup	Non-inverting differential clock input.
37	nCLK10	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
38	CLK10	Input	Pullup	Non-inverting differential clock input.
40	nCLK11	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
41	CLK11	Input	Pullup	Non-inverting differential clock input.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 1. PIN DESCRIPTIONS (CONTINUED)

Number	Name	Type		Description
42	OEB	Input	Pullup	Output enable pin. Controls enabling and disabling of QB/nQB outputs. LVCMOS/LVTTL internface levels. See Table 3A.
44	CLK0	Input	Pullup	Non-inverting differential clock input.
45	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
47	CLK1	Input	Pullup	Non-inverting differential clock input.
48	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

TABLE 3B. OEA, OEB CONTROL INPUT FUNCTION TABLE

Input	Output
OEA, OEB	**QA/nQA, QB/nQB**
0	Disabled (Logic LOW)
1	Active

TABLE 3B. SEL_A CONTROL INPUT FUNCTION TABLE

Control Input				Input Selected to QA/nQA
SELA_3	SELA_2	SELA_1	SELA_0	
0	0	0	0	CLK0, nCLK0
0	0	0	1	CLK1, nCLK1
0	0	1	0	CLK2, nCLK2
0	0	1	1	CLK3, nCLK3
0	1	0	0	CLK4, nCLK4
0	1	0	1	CLK5, nCLK5
0	1	1	0	CLK6, nCLK6
0	1	1	1	CLK7, nCLK7
1	0	0	0	CLK8, nCLK8
1	0	0	1	CLK9, nCLK9
1	0	1	0	CLK10, nCLK10
1	0	1	1	CLK11, nCLK11
1	1	0	0	L/H
1	1	0	1	L/H
1	1	1	0	L/H
1	1	1	1	L/H

TABLE 3C. SEL_B CONTROL INPUT FUNCTION TABLE

Control Input				Input Selected to QB/nQB
SELB_3	SELB_2	SELB_1	SELB_0	
0	0	0	0	CLK0, nCLK0
0	0	0	1	CLK1, nCLK1
0	0	1	0	CLK2, nCLK2
0	0	1	1	CLK3, nCLK3
0	1	0	0	CLK4, nCLK4
0	1	0	1	CLK5, nCLK5
0	1	1	0	CLK6, nCLK6
0	1	1	1	CLK7, nCLK7
1	0	0	0	CLK8, nCLK8
1	0	0	1	CLK9, nCLK9
1	0	1	0	CLK10, nCLK10
1	0	1	1	CLK11, nCLK11
1	1	0	0	L/H
1	1	0	1	L/H
1	1	1	0	L/H
1	1	1	1	L/H

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, I_O (LVDS)	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	67.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{DD} = 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			110		mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.7	V
I_{IH}	Input High Current	SELA_0:3, SELB_0:3	V_{DD} = 2.625V			150	µA
		OEA, OEB	V_{DD} = 2.625V			5	µA
I_{IL}	Input Low Current	SELA_0:3, SELB_0:3	V_{DD} = 2.625V, V_{IN} = 0V	-5			µA
		OEA, OEB	V_{DD} = 2.625V, V_{IN} = 0V	-150			µA

Table 4C. Differential DC Characteristics, V_{DD} = 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0:CLK11 nCLK0:nCLK11	V_{DD} = V_{IN} = 2.625V			150	µA
I_{IL}	Input Low Current	CLK0:CLK11	V_{DD} = 2.625V, V_{IN} = 0V	-5			µA
		nCLK0:nCLK11	V_{DD} = 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLKx, nCLKx is V_{DD} + 0.3V.

TABLE 4D. LVDS DC CHARACTERISTICS, V_{DD} = 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			400		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.3		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

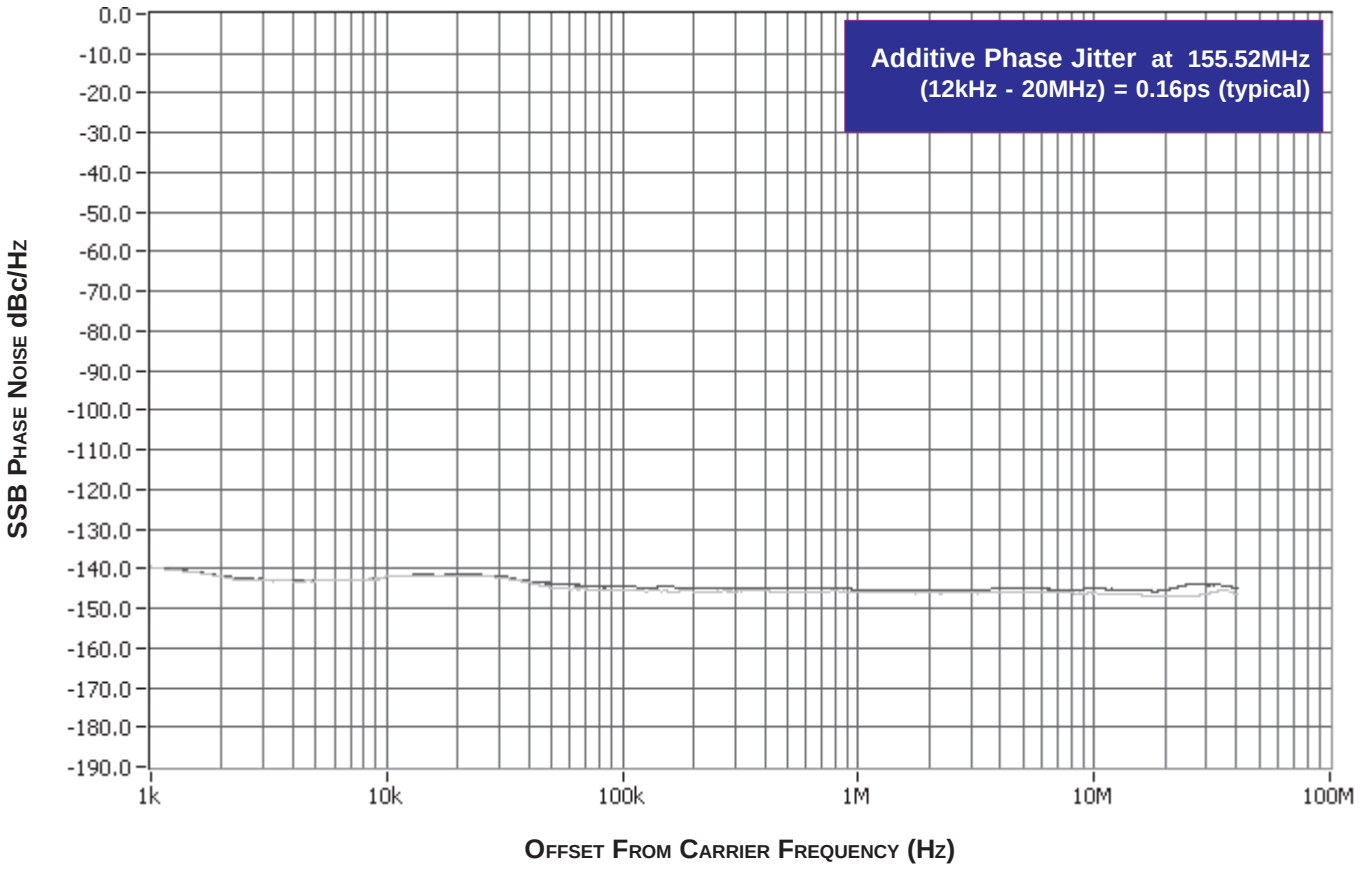
TABLE 5. AC CHARACTERISTICS, V_{DD} = 2.5V ± 5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				>3	GHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1			650		ps
tp_{HL}	Propagation Delay, High to Low; NOTE 1			650		ps
*t*sk(o)	Output Skew; NOTE 2, 3			25		ps
*t*sk(i)	Input Skew; NOTE 3			TBD		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			TBD		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 5	155.52MHz, Integration Range: 12kHz - 20MHz		0.16		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		110		ps
odc	Output Duty Cycle			50		%
$MUX_{ISOLATION}$	MUX Isolation	f_{OUT} < 1.2GHz		45		dB

All parameters measured at 500MHz, unless noted otherwise.
NOTE 1: Measured from V_{DD}/2 of the input to V_{DD}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DD}/2.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DD}/2.
NOTE 5: Driving only one input clock.

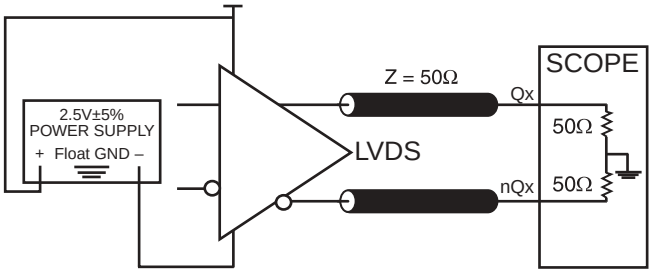
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

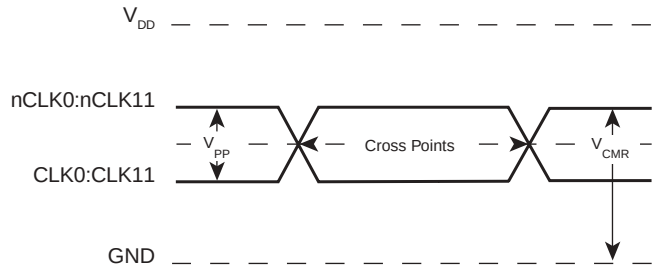


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

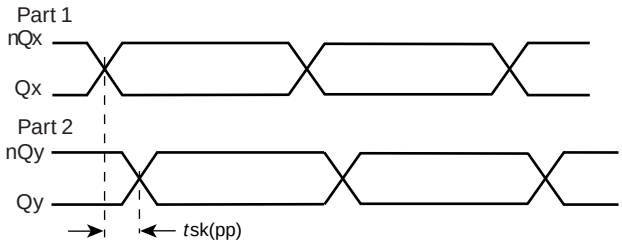
PARAMETER MEASUREMENT INFORMATION



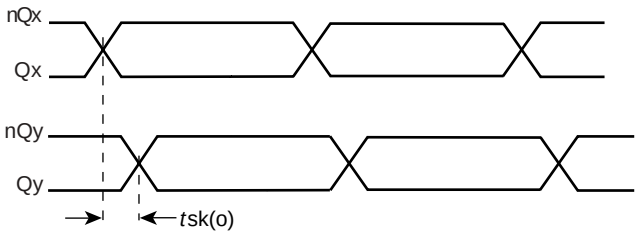
2.5V OUTPUT LOAD AC TEST CIRCUIT



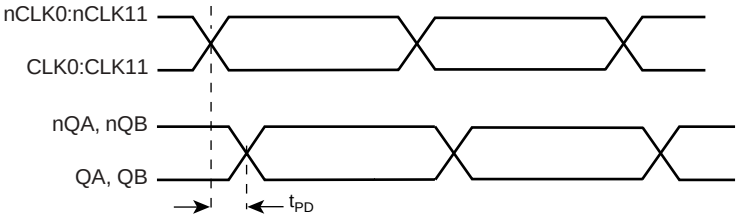
DIFFERENTIAL INPUT LEVEL



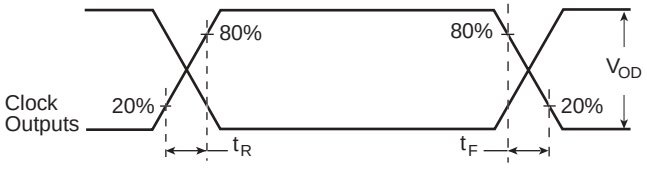
PART-TO-PART SKEW



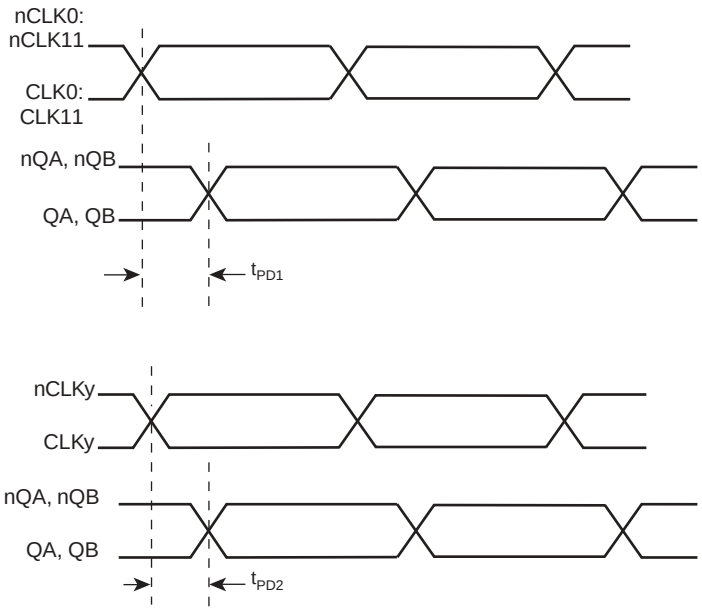
OUTPUT SKEW



PROPAGATION DELAY

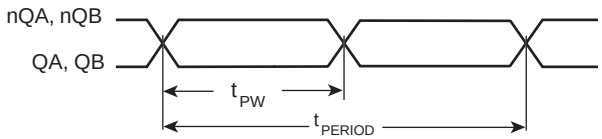


OUTPUT RISE/FALL TIME



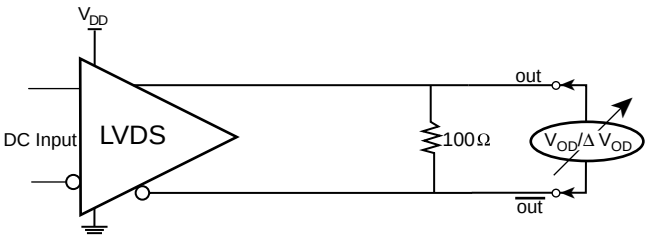
$tsk(i) = |t_{PD1} - t_{PD2}|$

INPUT SKEW

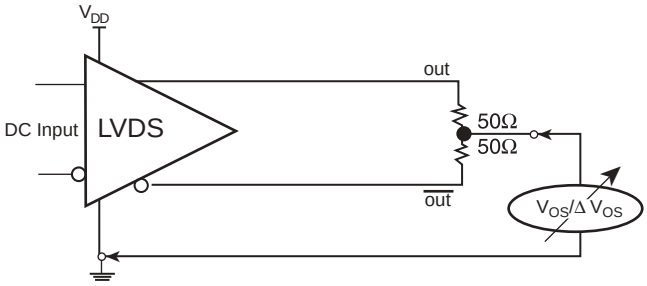


$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



DIFFERENTIAL OUTPUT VOLTAGE SETUP



OFFSET VOLTAGE SETUP

APPLICATION INFORMATION

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK/nCLK INPUT:
For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVDS OUTPUT
All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V

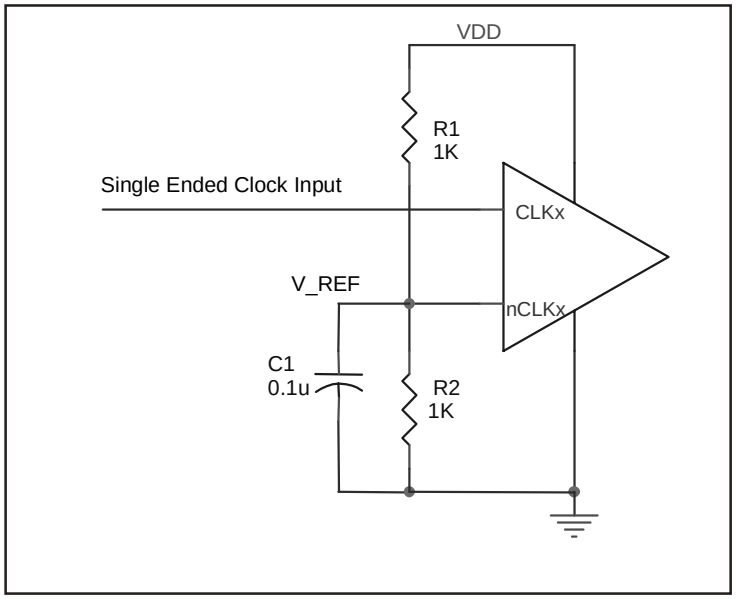


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A,* the input termination applies for IDT HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

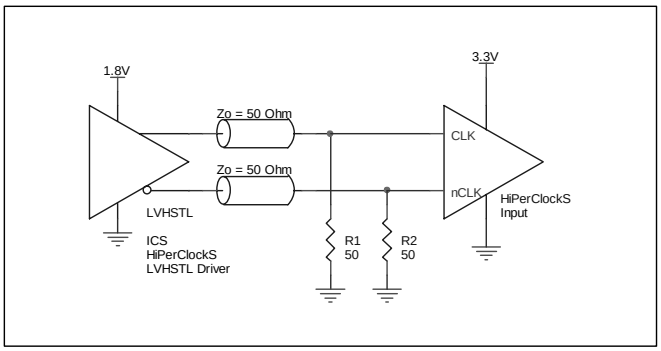


FIGURE 2A. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY IDT HIPERCLOCKS LVHSTL DRIVER

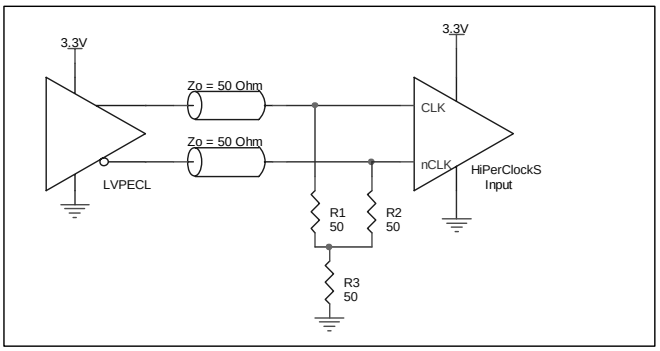


FIGURE 2B. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

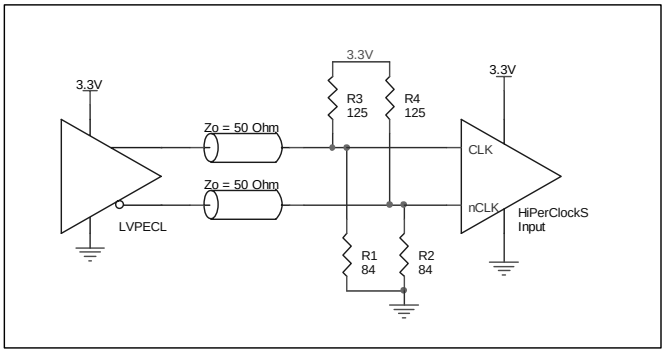


FIGURE 2C. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

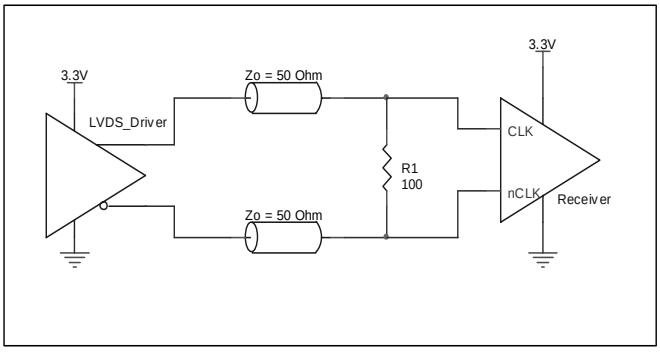


FIGURE 2D. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

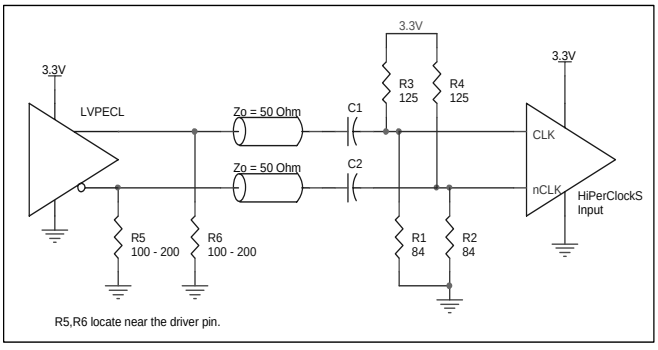


FIGURE 2E. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE

2.5V LVDS Driver Termination

Figure 3 shows a typical termination for LVDS driver in characteristic impedance of 100Ω differential (50Ω single) transmission line environment. For buffer with multiple LDVS driver, it is recommended to terminate the unused outputs.

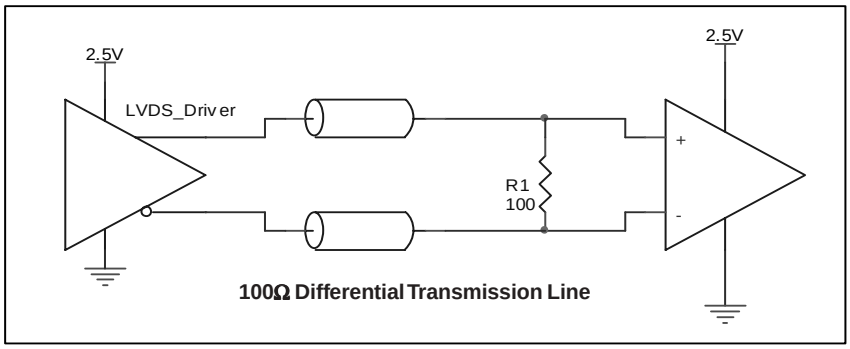


Figure 3. Typical LVDS Driver Termination

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS854S202I-01.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS854S202I-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 2.5V + 5% = 2.625V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 2.625V * 110mA = **288.75mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 57.4°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.289W * 57.4°C/W = 101.6°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 48-LEAD LQFP, FORCED CONVECTION

θ_{JA} vs. Air Flow (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	67.2°C/W	57.4°C/W	53.8°C/W

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 48 LEAD LQFP

θ_{JA} vs. Air Flow (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	67.2°C/W	57.4°C/W	53.8°C/W

TRANSISTOR COUNT

The transistor count for ICS854S202I-01 is: 8,485

Package Outline - Y Suffix for 48 Lead LQFP

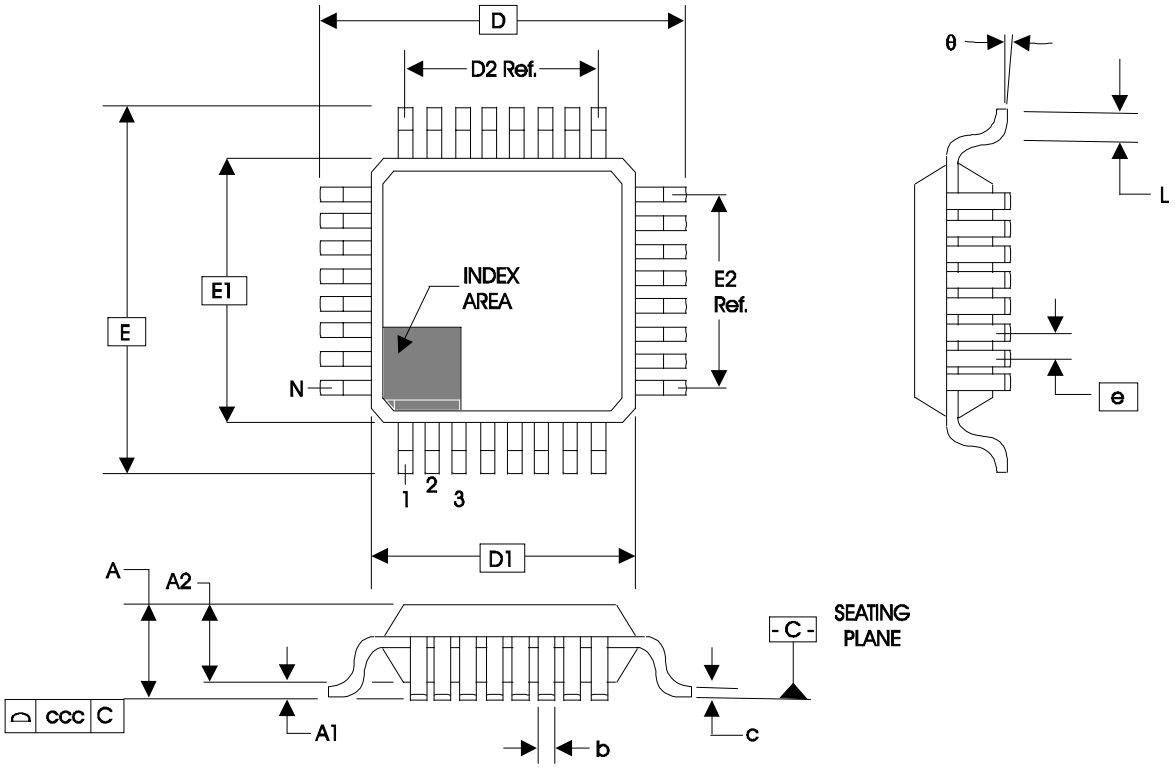


Table 8. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N		48	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50 Ref.	
e		0.50 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS854S202AYI-01	ICS4S202AI01	48 Lead LQFP	tray	-40°C to 85°C
ICS854S202AYI-01T	ICS4S202AI01	48 Lead LQFP	1000 tape & reel	-40°C to 85°C
ICS854S202AYI-01LF	TBD	48 Lead "Lead-Free" LQFP	tray	-40°C to 85°C
ICS854S202AYI-01LFT	TBD	48 Lead "Lead-Free" LQFP	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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