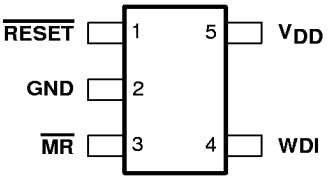
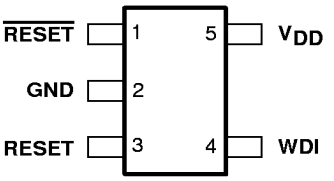
- **Power-On Reset Generator with Fixed Delay Time of 200 ms, no External Capacitor Needed**
- **Manual Reset Input (TPS3823 Devices Only)**
- **Pin-For-Pin Compatible with the MAX823 and MAX824**
- **Supply Voltage Supervision Range 2.5 V, 3 V, 3.3 V, 5 V**
- **Watchdog Timer Retriggers $\overline{\text{RESET}}$ Output at $V_{DD} \geq V_{IT+}$**
- **Maximum Supply Current of 25 μA**
- **SOT23-5 Package**
- **Temperature Range . . . –40°C to 85°C**

TPS3823 . . . DBV PACKAGE
(TOP VIEW)



TPS3824 . . . DBV PACKAGE
(TOP VIEW)



description

The TPS3823, TPS3824 family of micropower supply-voltage supervisors provides circuit initialization and timing supervision, primarily for microprocessor-based systems.

During power-on, $\overline{\text{RESET}}$ is asserted when supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors V_{DD} and keeps $\overline{\text{RESET}}$ active as long as V_{DD} remains below the threshold voltage V_{IT+}. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, $t_d$typ = 200 ms, starts after V_{DD} has risen above the threshold voltage V_{IT+}. When the supply voltage drops below the threshold voltage V_{IT-}, the output becomes active (low) again. No external components are required. All the devices of this family have a fixed-sense threshold voltage V_{IT-} set by an internal voltage divider.

The TPS3823-xx devices incorporate a manual reset input, $\overline{\text{MR}}$. A low level at $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to become active. The TPS3824-xx devices do not have the input $\overline{\text{MR}}$, but include a high-level output RESET. Each circuit also has a watchdog timer that is periodically triggered by a positive or negative transition at WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, $t_{t(out)}$ = 1.6 s, $\overline{\text{RESET}}$ becomes active for the time period t_d. This event also reinitializes the watchdog timer. Leaving WDI unconnected disables the watchdog.

PACKAGE INFORMATION

DEVICE NAME	THRESHOLD VOLTAGE	MARKING	CHIP FORM (Y)
TPS3823-25DBVR	2.25 V	PAPI	TPS3823-25Y
TPS3823-30DBVR	2.63 V	PAQI	TPS3823-30Y
TPS3823-33DBVR	2.93 V	PARI	TPS3823-33Y
TPS3823-50DBVR	4.55 V	PASI	TPS3823-50Y
TPS3824-25DBVR	2.25 V	PATI	TPS3824-25Y
TPS3824-30DBVR	2.63 V	PAUI	TPS3824-30Y
TPS3824-33DBVR	2.93 V	PAVI	TPS3824-33Y
TPS3824-50DBVR	4.55 V	PAWI	TPS3824-50Y

description (continued)

The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in a 5-pin SOT23-5 package. The TPS3823, TPS3824 devices are characterized for operation over a temperature range of -40°C to 85°C.

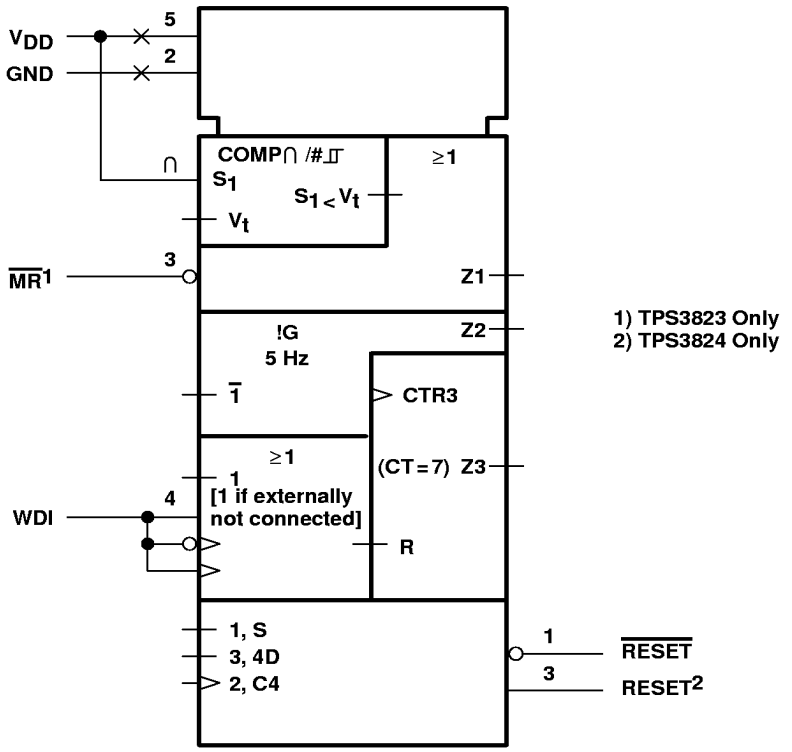
FUNCTION/TRUTH TABLE, TPS3823

$\overline{MR}$	$V_{DD}>V_{IT}$	$\overline{RESET}$
L	0	L
L	1	L
H	0	L
H	1	H

FUNCTION/TRUTH TABLE, TPS3824

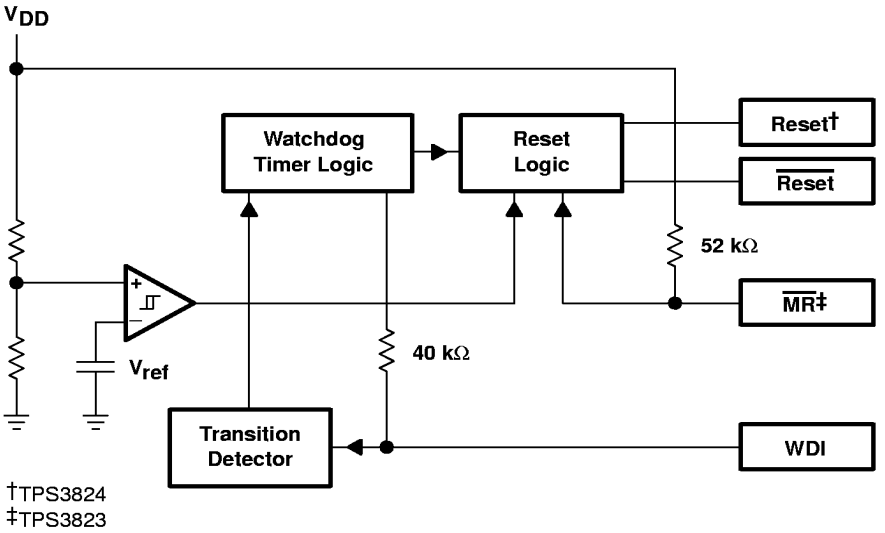
$V_{DD}>V_{IT}$	$\overline{RESET}$	RESET
0	L	H
1	H	L

logic symbol†

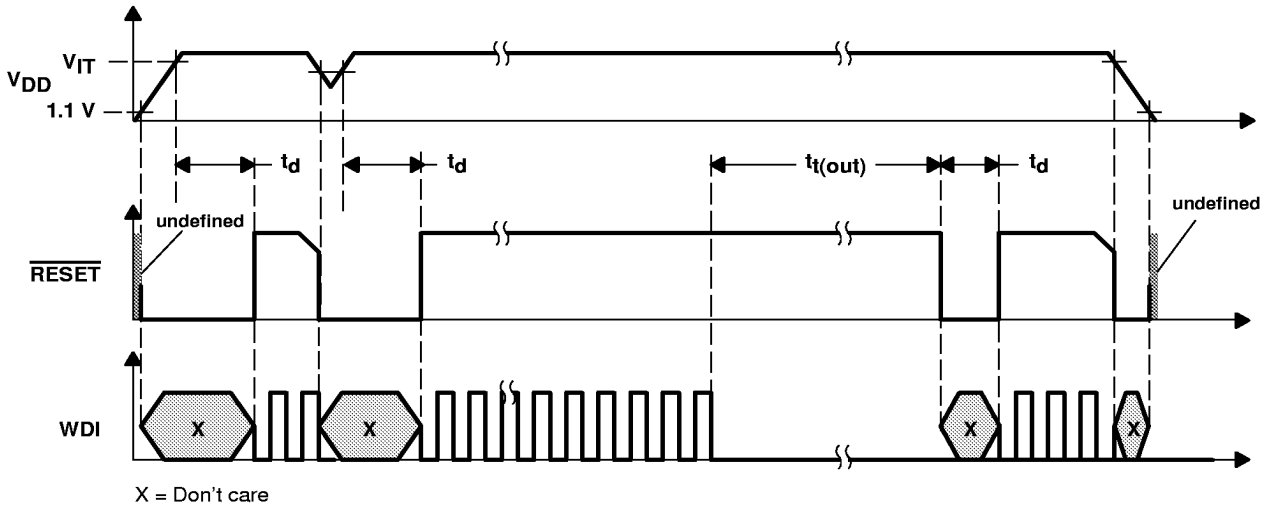


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

functional block diagram



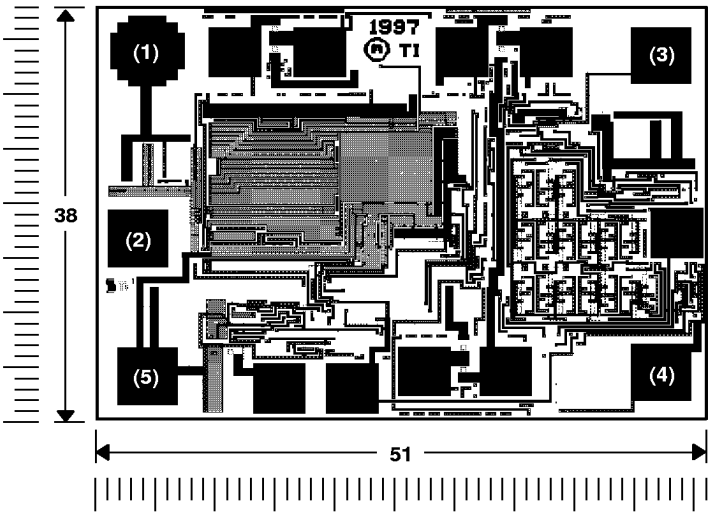
timing diagram

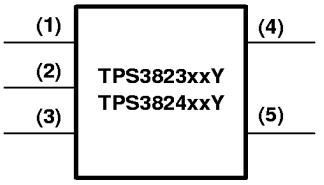


TPS38xxY chip information

These chips when properly assembled, display characteristics similar to those of the TPS38xx. Thermal compression or ultrasonic bonding may be caused on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 10 MILS TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

Terminal Functions

TERMINAL		NO.	I/O	DESCRIPTION
NAME				
$\overline{\text{RESET}}$		1	O	
GND		2		Ground
$\overline{\text{MR}}$	TPS3823	3	I	Manual reset
RESET	TPS3824		O	Reset
WDI		4	I	Watchdog input. WDI is the input for the watchdog timer.
V_{DD}		5		Supply voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 6 V
Input voltage, $\overline{MR}$, WDI (see Note 1) . . . . . –0.3 V to (V_{DD} + 0.3 V)
Maximum low output current, I_{OL} . . . . . 5 mA
Maximum high output current, I_{OH} . . . . . –5 mA
Input clamp current range, I_{IK} (V_I < 0 or V_I > V_{DD}) . . . . . ±10 mA
Output clamp current range, I_{OK} (V_O < 0 or V_O > V_{DD}) . . . . . ±10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Soldering temperature . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DBV	150 mW	1.2 mW/°C	96 mW	78 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1.1	5.5	V
Input voltage, V_I	0	V_{DD} + 0.3	V
High-level input voltage at $\overline{MR}$ and WDI, V_{IH}	0.7 × V_{DD}		V
Low-level input voltage, V_{IL}		0.3 × V_{DD}	V
Input transition rise and fall rate at $\overline{MR}$ or WDI, $\Delta t/\Delta V$		100	ns/V
Operating free-air temperature range, T_A	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{\text{RESET}}$	TPS382x-25	$V_{DD} = V_{IT+} + 0.2$ V, $I_{OH} = -20$ µA	$0.8 \times V_{DD}$			V
			TPS382x-30, TPS382x-33	$V_{DD} = V_{IT+} + 0.2$ V, $I_{OH} = -30$ µA				
			TPS382x-50	$V_{DD} = V_{IT+} + 0.2$ V, $I_{OH} = -120$ µA	$V_{DD} - 1.5$ V			
		RESET	TPS3824-25	$V_{DD} \geq 1.8$ V, $I_{OH} = -100$ µA	$0.8 \times V_{DD}$			V
			TPS3824-30, TPS3824-33, TPS3824-50	$V_{DD} \geq 1.8$ V, $I_{OH} = -150$ µA				
V_{OL}	Low-level output voltage	RESET	TPS3824-25	$V_{DD} = V_{IT+} + 0.2$ V, $I_{OL} = 1$ mA			0.4	V
			TPS3824-30, TPS3824-33	$V_{DD} = V_{IT+} + 0.2$ V, $I_{OL} = 1.2$ mA				
			TPS3824-50	$V_{DD} = V_{IT+} + 0.2$ V, $I_{OL} = 3$ mA			0.4	
		$\overline{\text{RESET}}$	TPS382x-25	$V_{DD} = V_{IT-} - 0.2$ V, $I_{OL} = 1$ mA			0.4	V
			TPS382x-30, TPS382x-33	$V_{DD} = V_{IT-} - 0.2$ V, $I_{OL} = 1.2$ mA				
			TPS382x-50	$V_{DD} = V_{IT-} - 0.2$ V, $I_{OL} = 3$ mA			0.4	
	Power-up reset voltage (see Note 2)			$V_{DD} \geq 1.1$ V, $I_{OL} = 20$ µA			0.4	V
V_{IT-}	Negative-going input threshold voltage (see Note 3)		TPS382x-25	$T_A = 0°C - 85°C$	2.21	2.25	2.30	V
			TPS382x-30		2.59	2.63	2.69	
			TPS382x-33		2.88	2.93	3	
			TPS382x-50		4.49	4.55	4.64	
			TPS382x-25	$T_A = -40°C - 85°C$	2.20	2.25	2.30	V
			TPS382x-30		2.57	2.63	2.69	
			TPS382x-33		2.86	2.93	3	
			TPS382x-50		4.46	4.55	4.64	
V_{hys}	Hysteresis at V_{DD} input		TPS382x-25, TPS382x-30, TPS382x-33			30		mV
			TPS382x-50			50		
$I_{IH(AV)}$	Average high-level input current		WDI	WDI = V_{DD}, time average (dc = 88%)		120		µA
$I_{IL(AV)}$	Average low-level input current			WDI = 0.3 V, V_{DD} = 5.5 V, time average (dc = 12%)		–15		
I_{IH}	High-level input current		WDI	WDI = V_{DD}		140	190	
			$\overline{\text{MR}}$	$\overline{\text{MR}} = V_{DD} \times 0.7$, V_{DD} = 5.5 V		–40	–60	
I_{IL}	Low-level input current		WDI	WDI = 0.3 V, V_{DD} = 5.5 V		140	190	
			$\overline{\text{MR}}$	$\overline{\text{MR}}$ = 0.3 V, V_{DD} = 5.5 V		–110	–160	

NOTES: 2. The lowest supply voltage at which $\overline{\text{RESET}}$ becomes active. $t_{r,\ VDD} \geq 15$ µs/V
3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near the supply terminals.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OS}	Output short-circuit current (see Note 4)	$\overline{\text{RESET}}$	TPS382x-25	$V_{DD} = V_{IT,\ max} + 0.2$ V, $V_O = 0$ V			–400	µA
			TPS382x-30					
			TPS382x-33					
			TPS382x-50				–800	
I_{DD}	Supply current			WDI and $\overline{\text{MR}}$ unconnected, Outputs unconnected		15	25	µA
	Internal pull-up resistor at $\overline{\text{MR}}$					52		kΩ
C_i	Input capacitance at $\overline{\text{MR}}$, WDI			$V_I = 0$ V to 5.5 V		5		pF

NOTE 4: The $\overline{\text{RESET}}$ short-circuit current is the maximum pull-up current when $\overline{\text{RESET}}$ is driven low by a µP bidirectional reset pin.

timing requirements at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
t_w	Pulse width	at V_{DD}	$V_{DD} = V_{IT+} + 0.2$ V, $V_{DD} = V_{IT-} - 0.2$ V	6		µs
		at $\overline{\text{MR}}$	$V_{DD} \geq V_{IT+} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	1		µs
		at WDI	$V_{DD} \geq V_{IT+} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	100		ns

switching characteristics at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{t(out)}$	Watchdog time out		$V_{DD} \geq V_{IT+} + 0.2$ V	0.9	1.6	2.5	s
t_d	Delay time		$V_{DD} \geq V_{IT+} + 0.2$ V, See timing diagram	120	200	300	ms
t_{pHL}	Propagation (delay) time, high-to-low-level output	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$ delay(TPS3823)	$V_{DD} \geq V_{IT+} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$			0.1	µs
		V_{DD} to $\overline{\text{RESET}}$ delay	$V_{IL} = V_{IT-} - 0.2$ V, $V_{IH} = V_{IT-} + 0.2$ V			25	
		V_{DD} to RESET delay (TPS3824)				25	

TYPICAL CHARACTERISTICS

NORMALIZED INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE AT V_{DD}

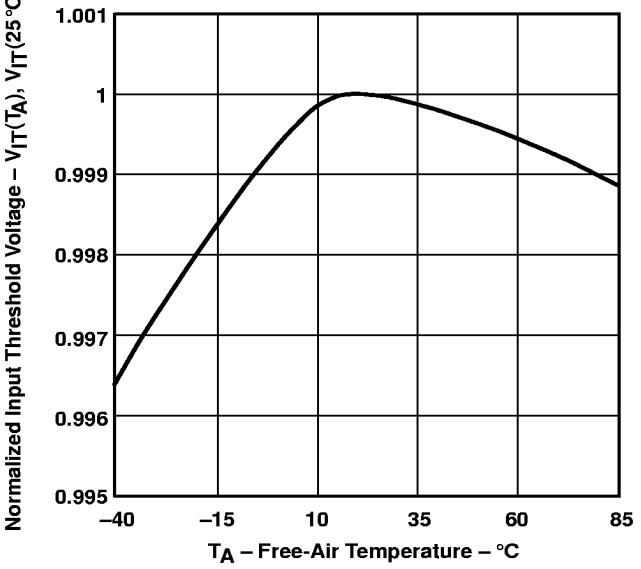


Figure 1

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

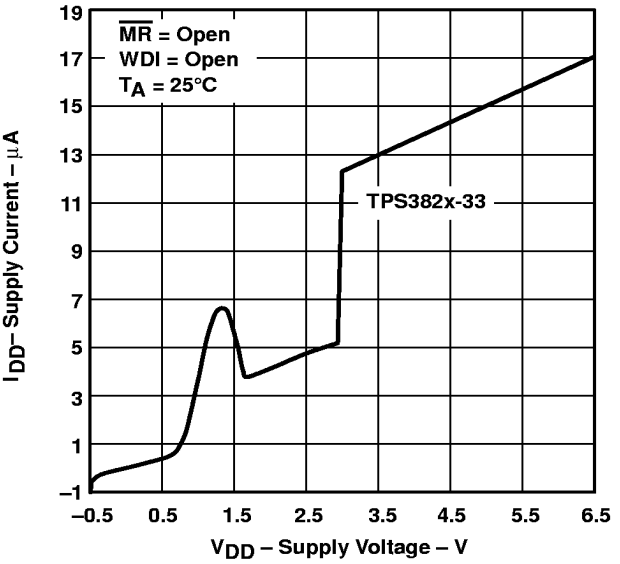


Figure 2

INPUT CURRENT
vs
INPUT VOLTAGE AT $\overline{MR}$

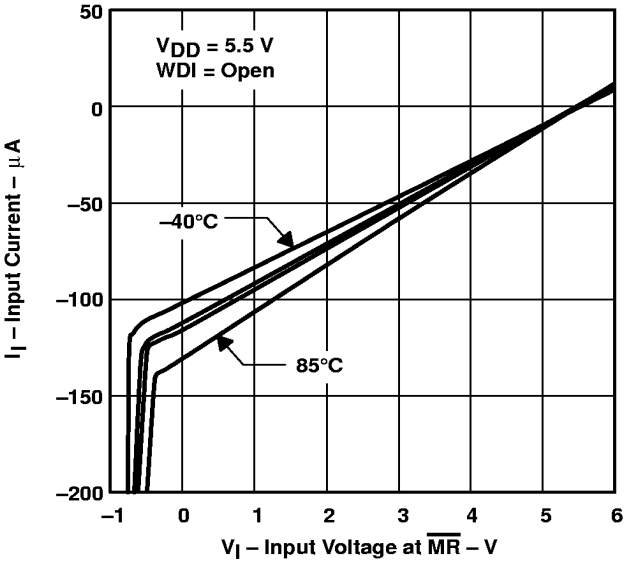


Figure 3

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

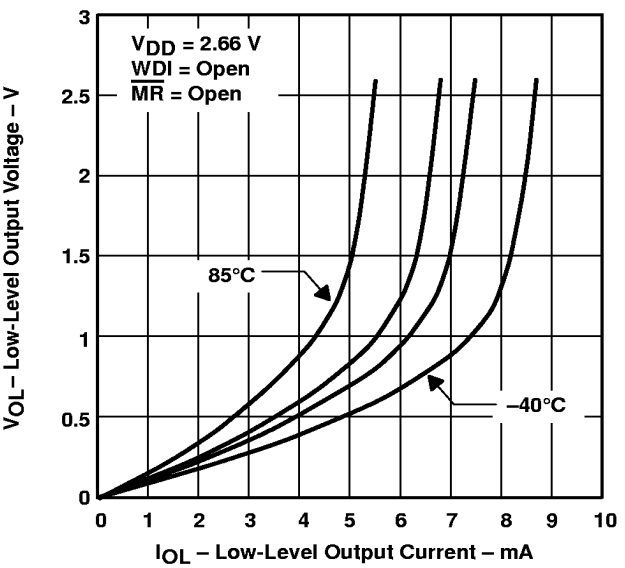


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

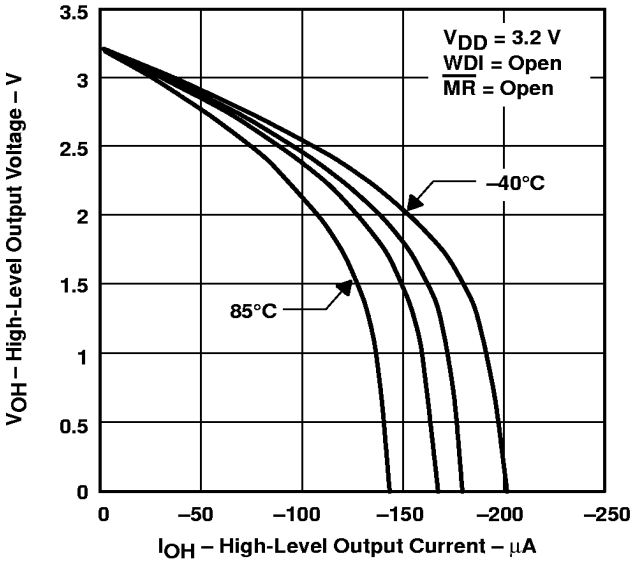


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

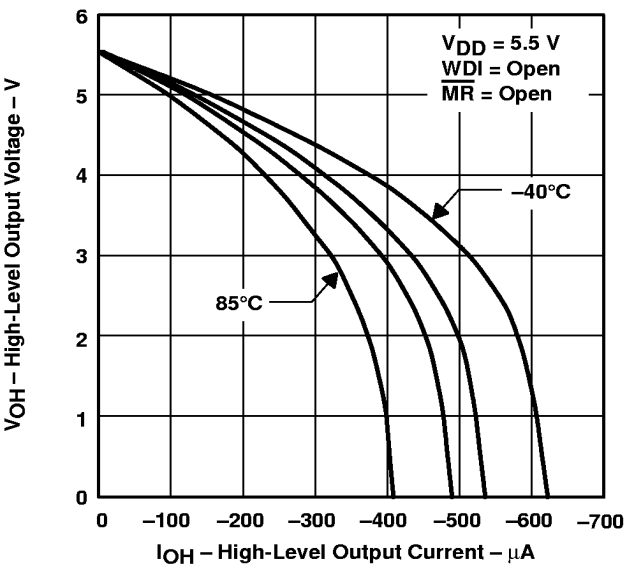


Figure 6

MINIMUM PULSE DURATION AT V_{DD}
vs
V_{DD} THRESHOLD OVERDRIVE

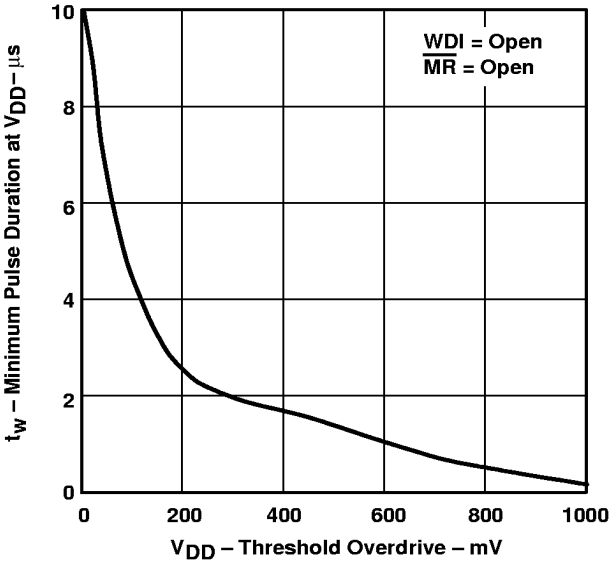
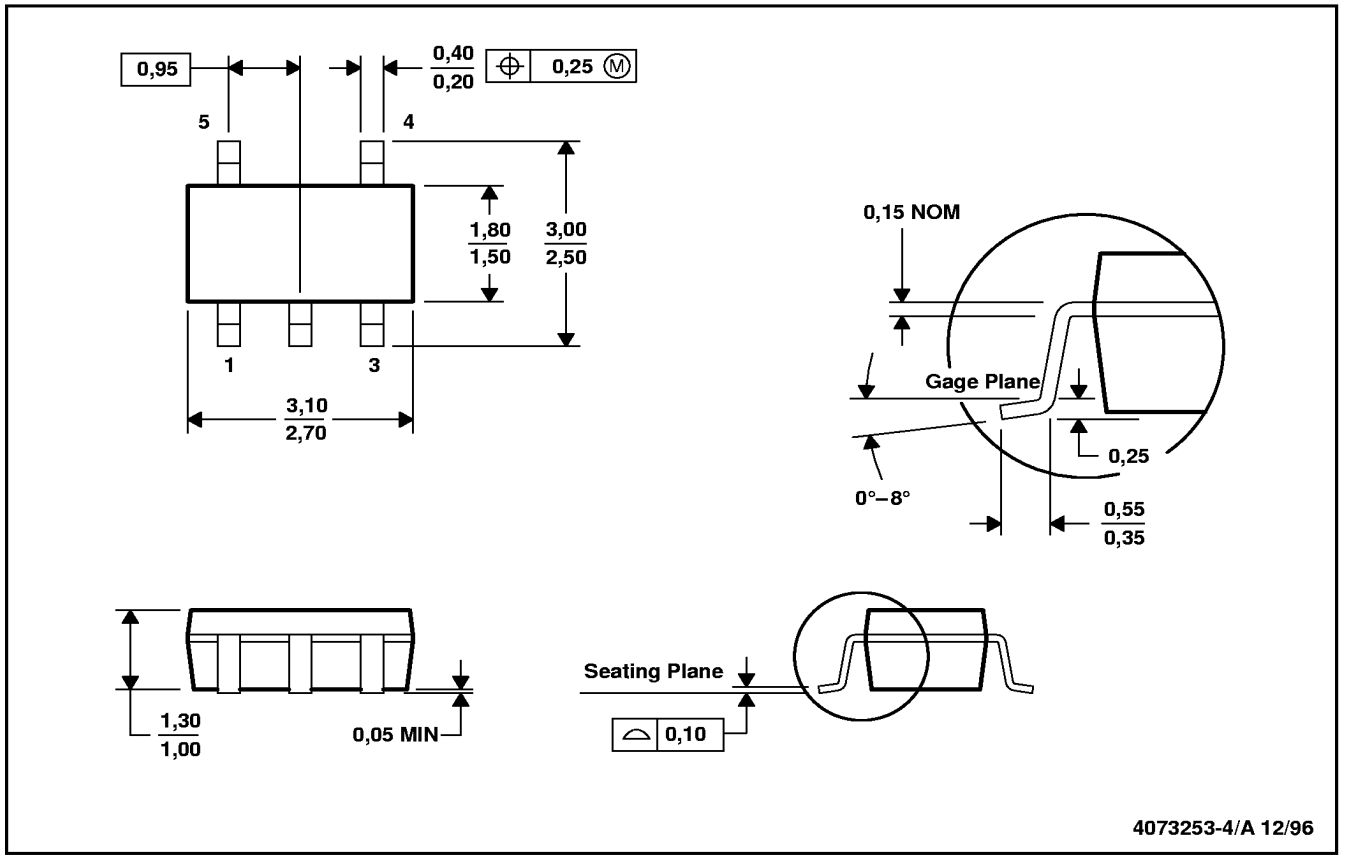


Figure 7

MECHANICAL DATA

DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

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