REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

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	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19				

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
13 FEBRUARY 1989

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, MEMORY, DIGITAL, CMOS
2K X 8 EEPROM, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-88676
A	67268	

SHEET 1 OF 19

DESC FORM 193
SEP 87

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5962-E944

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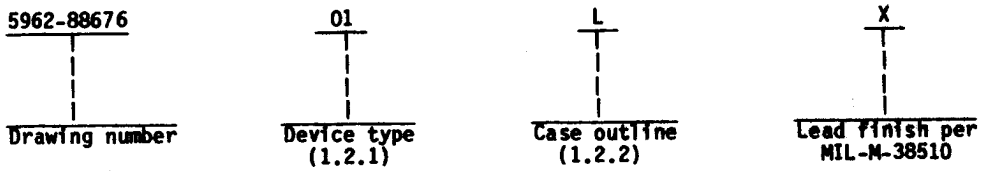
1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time	Write speed	Write mode	End of write indicator	Endurance
01	(see 6.4)	2K X 8 EEPROM	90 ns	1.0 ms	byte	DATA polling	10,000 cycles
02	(See 6.4)	2K X 8 EEPROM	70 ns	1.0 ms	byte	DATA polling	10,000 cycles
03	(see 6.4)	2K X 8 EEPROM	55 ns	1.0 ms	byte	DATA polling	10,000 cycles

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
J	D-3 (24-lead, 1.290" x .610" x .225"), dual-in-line package
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
X	C-12 (32-terminal, .560" x .458" x .120"), rectangular chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.3 V dc to +6.25 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J) 2/	+175°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Input voltage range (V_{IL}, V_{IH})	-0.3 V dc to +6.25 V dc
Data retention	10 years (minimum)
Endurance	10,000 cycles (minimum)
Chip clear voltage (V_H)	12.0 V dc

1.4 Recommended operating conditions. 1/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Input voltage, low range (V_{IL})	-0.1 V dc to +0.8 V dc
Input voltage, high range (V_{IH})	+2.0 V dc to V_{CC} +0.3 V dc

1/ All voltages are referenced to V_{SS} (ground).
2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, V_{SS} = 0 V, 4.5 V $\le V_{CC} \le$ 5.5 V, unless otherwise specified 1/	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Supply current (operating)	I_{CC1}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, all I/O's = 0.0 mA, inputs = 5.5 V, f = 1/ t_{AVAV} (min)	1, 2, 3	All		80	mA
Supply current (TTL standby)	I_{CC2}	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$, all I/O's = 0.0 mA, inputs = V_{CC}-0.3 V, f = 0.0 MHz	1, 2, 3	All		3.0	mA
Supply current (CMOS standby)	I_{CC3}	$\overline{CE} = V_{CC}$ - 0.3 V, all I/O's = 0.0 mA, inputs = V_{IL} or V_{CC} - 0.3 V, f = 0.0 MHz	1, 2, 3	All		100	µA
Input leakage high	I_{IH}	V_{IN} = 5.5 V	1, 2, 3	All		+10	µA
Input leakage low	I_{IL}	V_{IN} = 0.1 V	1, 2, 3	All	-10		µA
Output leakage high	I_{OHZ}	V_{OUT} = 5.5 V, $\overline{CE} = V_{IH}$ 2/	1, 2, 3	All		+10	µA
Output leakage low	I_{OLZ}	V_{OUT} = 0.1 V, $\overline{CE} = V_{IH}$ 2/	1, 2, 3	All	-10		µA
Input voltage low	V_{IL}		1, 2, 3	All	-0.1	0.8	V
Input voltage high	V_{IH}		1, 2, 3	All	2.0	V_{CC} +0.3V	V
Output voltage low	V_{OL}	I_{OL} = 12 mA, V_{IH} = 2.0 V, V_{CC} = 4.5 V, V_{IL} = 0.8 V	1, 2, 3	All		0.45	V
Output voltage high	V_{OH}	I_{OH} = -4.0 mA, V_{IH} = 2.0 V, V_{CC} = 4.5 V, V_{IL} = 0.8 V	1, 2, 3	All	2.4		V
$\overline{OE}$ high leakage (chip erase)	I_{OE}	V_H = 13 V	1, 2, 3	All	-10	100	µA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{SS} = 0$ V, $4.5 V \le V_{CC} \le 5.5$ V, unless otherwise specified 1/	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input capacitance	C_I	$V_I = 0.0$ V, $V_{CC} = 5.0$ V, $T_A = 25°C$, f = 1.0 MHz, see 4.3.1c 3/ 4/	4	All		6.0	pF
Output capacitance	C_O	$V_O = 0.0$ V, $V_{CC} = 5.0$ V, $T_A = 25°C$, f = 1.0 MHz, see 4.3.1c 3/ 4/	4	All		12	pF
Read cycle time 4/	t_{AVAV}	See figure 3 5/	9, 10, 11	01	90		ns
				02	70		
				03	55		
Address access time	t_{AVQV}		9, 10, 11	01		90	ns
				02		70	
				03		55	
Chip enable access time	t_{ELQV}		9, 10, 11	01		90	ns
				02		70	
				03		55	
Output enable access time	t_{OLQV}		9, 10, 11	01		50	ns
				02		50	
				03		40	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{SS} = 0$ V, $4.5 V \le V_{CC} \le 5.5$ V, unless otherwise specified 1/	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Chip enable to output in low Z 4/	t_{ELQX}	See figure 3 5/	9, 10, 11	All	0		ns
Chip disable to output in high Z 4/	t_{EHQZ}		9, 10, 11	01		50	ns
				02		50	
				03		40	
Output enable to output in low Z 4/	t_{OLQX}		9, 10, 11	All	0		ns
Output disable to output in high Z 4/	t_{OHQZ}		9, 10, 11	01		50	ns
				02		50	
				03		40	
Output hold from address change	t_{AXQX}		9, 10, 11	All	0		ns
Write cycle time	t_{WHWL} t_{EHEL1}	See figures 4 and 5 as applicable 5/	9, 10, 11	All		1.0	ms
Address setup time	t_{AVEL} t_{AVWL}		9, 10, 11	All	0		ns
Address hold time	t_{ELAX} t_{WLAX}		9, 10, 11	All	5.0		ns
Write setup time	t_{WLEL} t_{ELWL}		9, 10, 11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{SS} = 0$ V, $4.5 V \le V_{CC} \le 5.5$ V, unless otherwise specified 1/	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Write hold time	t_{EHWH} t_{WHEH}	See figures 4 and 5 as applicable 5/	9, 10, 11	All	0		ns
$\overline{OE}$ setup time	t_{OHEL} t_{OHWL}		9, 10, 11	All	0		ns
$\overline{OE}$ hold time	t_{EHOL} t_{WHOL}		9, 10, 11	All	0		ns
$\overline{WE}$ pulse width	t_{ELEH} t_{WLWH1}		9, 10, 11	All	100		ns
Data setup time	t_{DVEH} t_{DVWH}		9, 10, 11	All	50		ns
Delay to next write 4/	t_{DVWL} t_{DVEL}		9, 10, 11	All		0	µs
Data hold time	t_{EHDX} t_{WHDX}		9, 10, 11	All	0		ns
Last byte loaded to data polling 4/	t_{WHEL} t_{EHEL}		9, 10, 11	All		0	ns
$\overline{CE}$ setup time	t_{ELWL1}	See figure 6 5/	9, 10, 11	All	5.0		µs
Output setup time	t_{OVHWL}		9, 10, 11	All	5.0		µs
$\overline{CE}$ hold time	t_{WHEH1}		9, 10, 11	All	5.0		µs
$\overline{OE}$ hold time	t_{WHOH}		9, 10, 11	All	5.0		µs
High voltage	V_H		9, 10, 11	All	12	13	V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{SS} = 0$ V, $4.5 V \le V_{CC} \le 5.5$ V, unless otherwise specified 1/	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Chip erase	t_{WLWH2}	See figure 6 5/	9, 10, 11	All	10	210	ms

1/ DC and read mode.

2/ Connect all address inputs and $\overline{OE}$ to V_{IH} and measure I_{OLZ} and I_{OHZ} with the output under test connected to V_{OUT}.

3/ All pins not being tested are to be open.

4/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

5/ Tested by application of specified timing signals and conditions, including;

Equivalent ac test conditions:
Devices types: 01 through 03
Output load: 1 TTL gate and C_L = 100 pF (minimum) or equivalent circuit.
Input rise and fall times $\le$ 10 ns
Input pulse levels: 0.4 and 2.4 V
Timing measurements reference levels:
Inputs 1.0 V and 2.0 V
Outputs 0.8 V and 2.0 V

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.9 Processing EEPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

Device type	All	
Case outline	J and L	X
Terminal number	Terminal symbol	
1	A_7	NC
2	A_6	NC
3	A_5	NC
4	A_4	A_7
5	A_3	A_6
6	A_2	A_5
7	A_1	A_4
8	A_0	A_3
9	I/O_0	A_2
10	I/O_1	A_1
11	I/O_2	A_0
12	V_{SS}	NC
13	I/O_3	I/O_0
14	I/O_4	I/O_1
15	I/O_5	I/O_2
16	I/O_6	V_{SS}
17	I/O_7	NC
18	$\overline{CE}$	I/O_3
19	A_{10}	I/O_4
20	$\overline{OE}$	I/O_5
21	$\overline{WE}$	I/O_6
22	A_9	I/O_7
23	A_8	$\overline{CE}$
24	V_{CC}	A_{10}
25	--	$\overline{OE}$
26	--	NC
27	--	NC
28	--	A_9
29	--	A_8
30	--	NC
31	--	$\overline{WE}$
32	--	V_{CC}

FIGURE 1. Terminal connections.

Device types 01 thru 03

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Data out
Standby/write inhibit	V_{IH}	X	X	High impedance state
Chip clear	V_{IL}	V_H	V_{IL}	High impedance state
Byte write	V_{IL}	V_{IH}	V_{IL}	Data in
Write inhibit	X	V_{IL}	X	
Write inhibit	X	X	V_{IH}	
Output disable	X	V_{IH}	X	High impedance state

V_{IH} = Logic high voltage level

V_{IL} = Logic low voltage level

V_H = Chip clear voltage

X = Don't care

FIGURE 2. Truth table for unprogrammed devices.

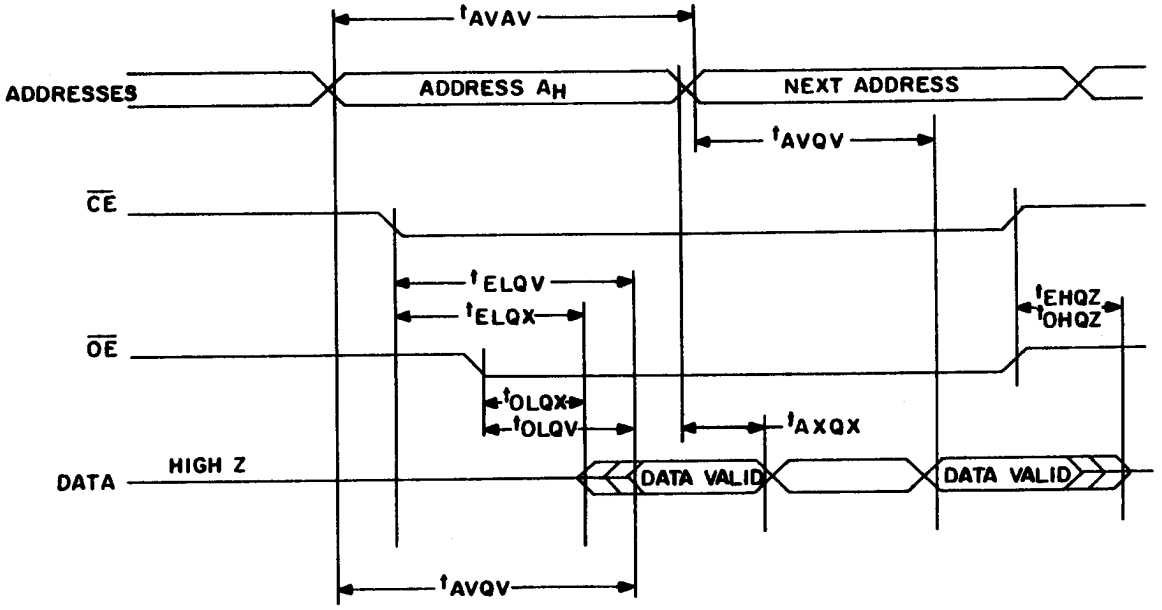

FIGURE 3. Read cycle waveforms.

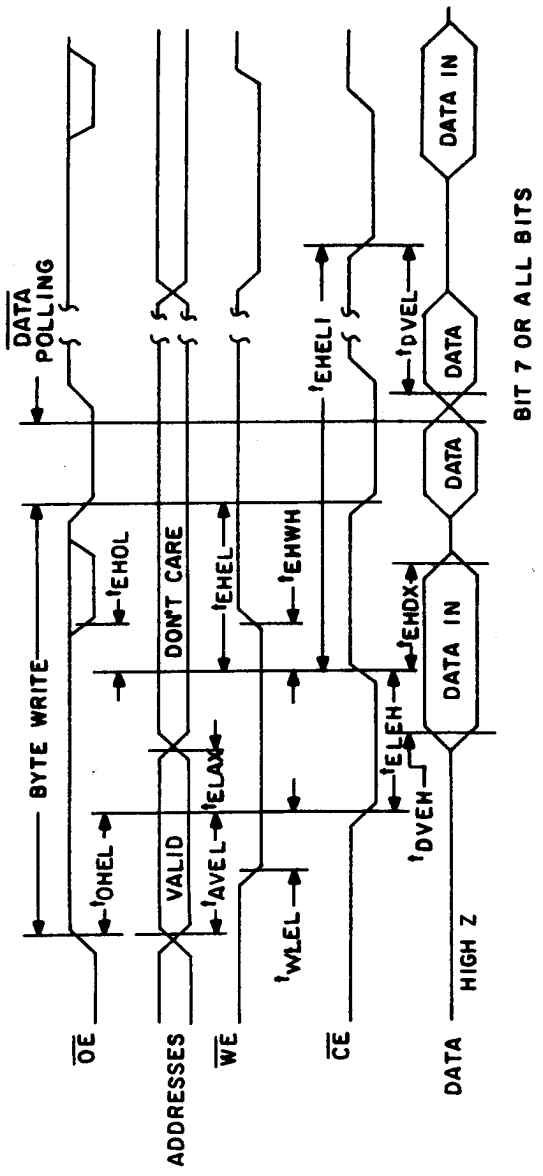

FIGURE 4. $\overline{CE}$ controlled byte write programming waveforms.

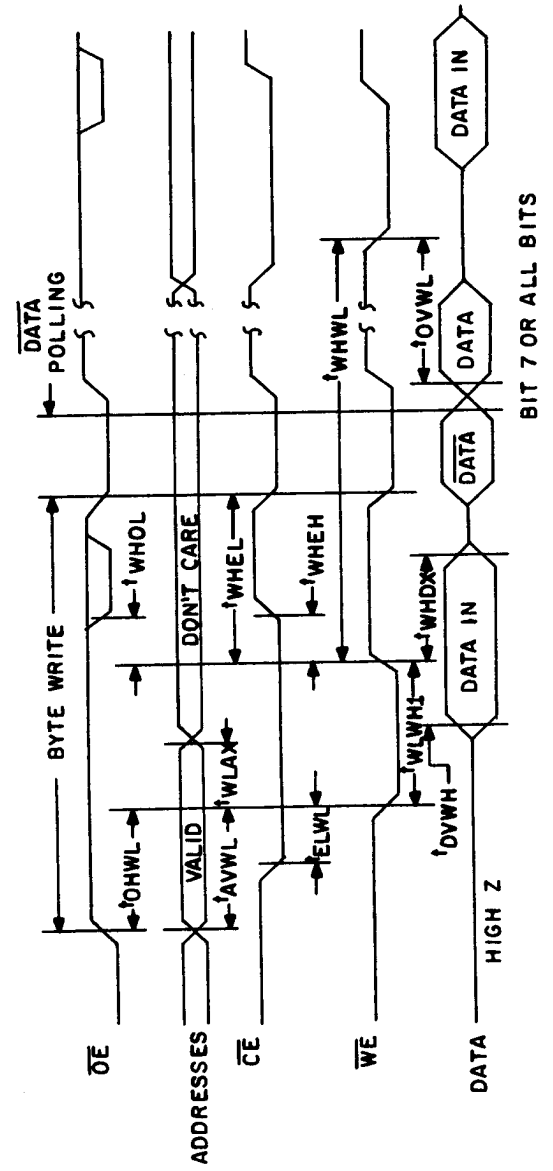

FIGURE 5. $\overline{WE}$ controlled byte write programming waveforms.

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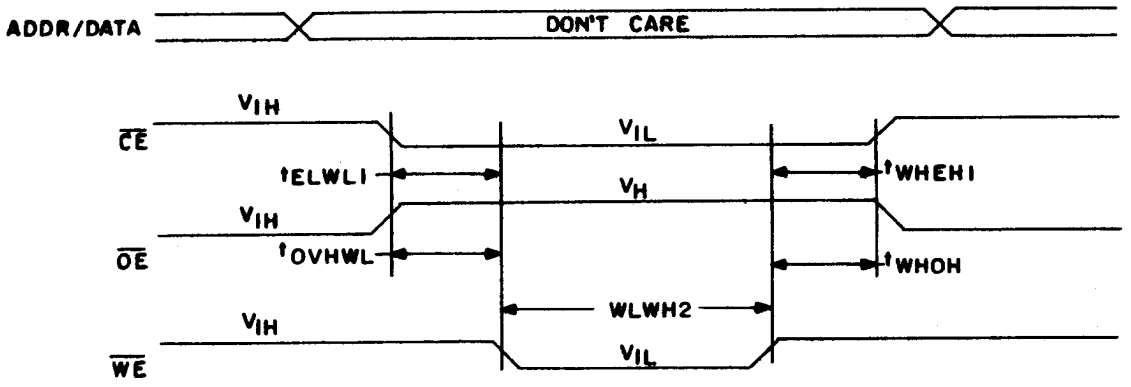

FIGURE 6. Chip clear waveforms.

3.9.1 Erasure of EEPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.5.3. Devices shall be shipped in the erased (logic "1's") and verified state unless otherwise specified.

3.9.2 Programmability of EEPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.2.

3.9.3 Verification of erasure or programmability of EEPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of reading the device in accordance with the procedures and characteristics specified in 4.5.4. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D or F using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Devices shall be burned-in containing a checkerboard pattern or equivalent.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. An endurance/retention test prior to burn-in, in accordance with method 1033 of MIL-STD-883, shall be included as part of the screening procedure with the following conditions:

(1) Cycling may be block, byte, or page at equipment room ambient temperature and shall cycle all bytes for a minimum of 10,000 cycles.

(2) After cycling, perform a high temperature unbiased bake for 72 hours at 150°C (minimum). The storage time may be accelerated by using higher temperature in accordance with the Arrhenius Relationship:

$$A_F = e^{-\frac{E_A}{K}\left[\frac{1}{T_1} - \frac{1}{T_2}\right]}$$

A_F = acceleration factor (unitless quantity) = t_1/t_2.
T = temperature in Kelvin (i.e., °C + 273 = K).
t_1 = time (hrs) at temperature T_1.
t_2 = time (hrs) at temperature T_2.
K = Boltzmanns constant = 8.62×10^{-5} eV/°K using an apparent activation energy (E_A) of 0.6 eV.
The maximum storage temperature shall not exceed 200°C for packaged devices or +300°C for unassembled devices.

(3) Read the data retention pattern and test using subgroups 1, 7, and 9 (minimum, e.g., high temperature equivalent subgroups 2, 8A, and 10 may be used) after cycling and bake, prior to burn-in. Devices having bits not in the proper state after storage shall constitute a device failure.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial qualification and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 tests sufficient to verify the truth table.

4.3.2 Groups C inspections. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. All devices requiring end-point electrical testing shall be programmed with a checkerboard or equivalent alternating bit pattern.

c. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition D or F using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

d. An endurance test, in accordance with method 1033 of MIL-STD-883, shall be added to group C1 inspection prior to performing the steady state life test (see 4.3.2c) and extended data retention (see 4.3.2e). Cycling may be block, byte, or page from devices passing group A after the completion of the requirements of 4.2 herein. Initially, two groups of devices shall be formed, cell 1 and cell 2. The following conditions shall be met:

(1) Cell 1 shall be cycled at -55°C and cell 2 shall be cycled at +125°C for a minimum of 10,000 cycles.

(2) Perform group A subgroups 1, 7, and 9 after cycling. Form two new cells (cells 3 and 4) for steady-state life and extended data retention. Cell 3 for steady-state life test consists of one-half of the devices from cell 1 and one-half of the devices from cell 2. Cell 4 for extended data retention consists of the remaining devices from cells 1 and 2.

(3) The sample plans for cell 1, cell 2, cell 3, and cell 4 shall individually be the same as for group C1, as specified in method 5005 of MIL-STD-883.

e. Extended data retention shall consist of:

(1) All devices shall be programmed with a charge on all memory cells in each device, such that the cell will read opposite the state that the cell would read in its equilibrium state (e.g., worst case pattern, see 4.2c.(2)).

(2) Unbiased bake for 1,000 hours (minimum) at +150°C (minimum). The unbiased bake time may be accelerated by using higher temperature in accordance with the Arhennius Relationship:

$$A_F = e^{-\frac{E_A}{K}\left[\frac{1}{T_1} - \frac{1}{T_2}\right]}$$

A_F = acceleration factor (unitless quantity) = t_1/t_2.
T = temperature in Kelvin (i.e., °C + 273 = K).
t_1 = time (hrs) at temperature T_1.
t_2 = time (hrs) at temperature T_2.
K = Boltzmanns constant = 8.62×10^{-5} eV/°K using an apparent activation energy of (E_A) of 0.6 eV.
The maximum storage temperature shall not exceed 200°C for packaged devices or 300°C for unassembled devices.

(3) Read the pattern after bake and perform end-point electrical tests for table II herein for group C.

4.3.3 Groups D inspections. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. All devices requiring end-point electrical testing shall be programmed with a checkerboard or equivalent alternating bit pattern.

4.4 Electrostatic discharge sensitivity inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. The option to categorize as ESD sensitive without performing the test is not allowed. Only those device types that pass ESDS testing at 2,000 V or greater shall be considered as conforming to the requirements of this drawing. ESDS testing shall be measured only for initial inspection and after process or design changes which may affect ESDS classification.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables of method 5005 of MIL-STD-883 and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.5.2 Programming procedure. The following procedure shall be followed when programming (Write) is performed. The waveforms and timing relationships shown in figure 5 and the conditions specified in table I shall be adhered to. Information is introduced by selectively programming a TTL low or TTL high on each I/O of the address desired. Functionality shall be verified at all temperatures (group A, subgroups 7 and 8) by programming all bytes of each device and verifying the pattern used.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/ 5/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1,7,9, or 2,8 (+125°C),10
Final electrical test parameters (method 5004)	1*,2,3,7*,8, 9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7,8, 9,10, 11
Groups C and D end-point electrical parameters (method 5005)	1,2,3,7,8, 9,10,11

1/ (*) indicates PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using multifunction testers.
3/ Subgroups 7 and 8 shall consist of writing and reading the data pattern specified in accordance with the limits of table I, subgroups 9, 10, and 11.
4/ For all electrical tests, the device shall be programmed to the data pattern specified.
5/ (**) indicates that subgroup 4 will only be performed during initial testing and after design or process changes, (see 4.3.1c).

4.5.3 Erasing procedure. There are two forms of erasure, chip and byte, whereby all bits or the address selected will be erased to a TTL high.

a. Chip erase is performed in accordance with the waveforms and timing relationships shown on figure 6 and the conditions specified in table I.

b. Byte erase is performed in accordance with the waveforms and timing relationships shown on figures 4 and 5.

4.5.4 Read mode operation. The waveforms and timing relationships shown on figure 3 and the conditions specified in table I shall be applied when reading the device. Pattern verification utilizes the read mode.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-88676D1JX	1FN41	AT28HC16L-90DM/883	---
5962-8867601LX	1FN41	AT28HC16LN-90DM/883	---
5962-8867601XX	1FN41	AT28HC16L-90LM/883	---
5962-8867602JX	1FN41	AT28HC16L-70DM/883	---
5962-8867602LX	1FN41	AT28HC16LN-70DM/883	---
5962-8867602XX	1FN41	AT28HC16L-70LM/883	---
5962-8867603JX	1FN41	AT28HC16L-55DM/883	---
5962-8867603LX	1FN41	AT28HC16LN-55DM/883	---
5962-8867603XX	1FN41	AT28HC16L-55LM/883	---

1/ Caution. Do not use this number for item acquisition. Items acquired by this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
1FN41	ATMEL Corporation 2095 Ringwood Avenue San Jose, CA 95131

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