8-Bit Programmable 2- to 5-Phase Synchronous Buck Controller

ADP3189

FEATURES

Selectable 2-, 3-, 4-, or 5-phase operation at up to 1 MHz per phase

±7.7 mV worst-case differential sensing error over temperature

Logic-level PWM outputs for interface to external high-power drivers

Active current balancing between all output phases

Built-in power good/crowbar blanking supports on-the-fly VID code changes

Digitally programmable 0.5 V to 1.6 V output— supports both VR10.x and VR11 specifications

Programmable short-circuit protection with programmable latch-off delay

APPLICATIONS

Desktop PC power supplies for

Next generation Intel® processors

VRM modules

GENERAL DESCRIPTION

The ADP3189[1] is a highly efficient multi-phase synchronous buck switching regulator controller optimized for converting a 12 V main supply into the core supply voltage required by high performance Intel processors. It uses an internal 8-bit DAC to read a voltage identification (VID) code directly from the processor, which is used to set the output voltage between 0.5 V and 1.6 V.

This device uses a multi-mode PWM architecture to drive the logic-level outputs at a programmable switching frequency that can be optimized for VR size and efficiency. The phase relationship of the output signals can be programmed to provide 2-, 3-, 4-, or 5-phase operation, allowing for the construction of up to five complementary buck switching stages.

The ADP3189 also includes programmable no-load offset and slope functions to adjust the output voltage as a function of the load current, so it is optimally positioned for a system transient. The ADP3189 also provides accurate and reliable short-circuit protection, adjustable current limiting, and a delayed power good output that accommodates on-the-fly output voltage changes requested by the CPU.

ADP3189 is specified over the extended commercial temperature range of 0°C to +85°C and is available in a 40-lead LFCSP package.

[1] Protected by U.S. Patent Number 6,683,441; others pending.

Rev. 0

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REVISION HISTORY

7/05—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

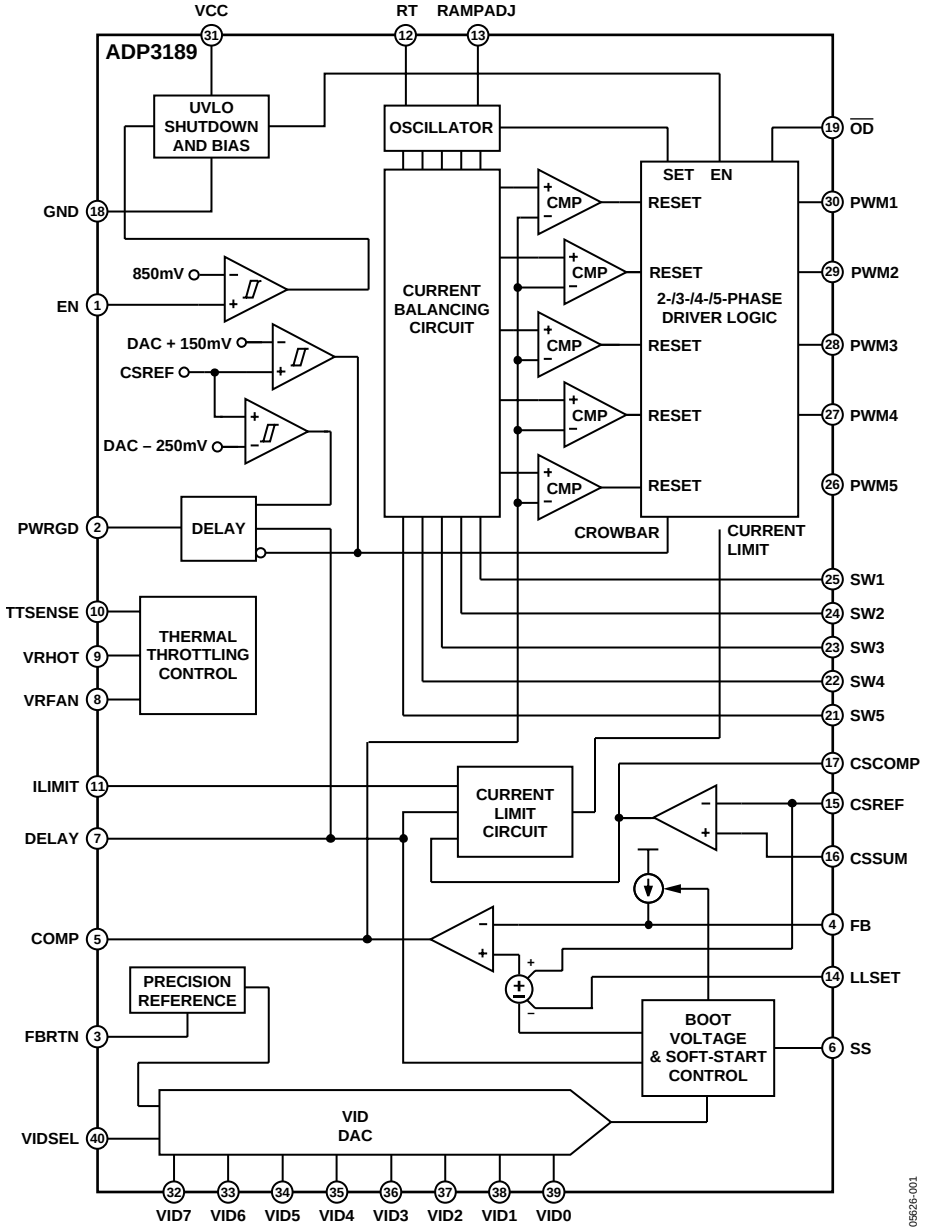

Figure 1.

SPECIFICATIONS

VCC = 12 V, FBRTN = GND, T_A = 0°C to 85°C, unless otherwise noted.[1]

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ERROR AMPLIFIER						
Output Voltage Range[2]	V_{COMP}		0.95		3.95	V
Accuracy	V_{FB}	Relative to nominal DAC output, referenced to FBRTN, LLSET = CSREF, Figure 2,				
		VIDSEL = GND,	−7.7		+7.7	mV
		VIDSEL = 1.25 V, VID Range 1.00625 V to 1.60000 V	−7.7		+7.7	mV
	$V_{FB(BOOT)}$	In start-up	1.092	1.1	1.108	V
Load Line Positioning Accuracy		CSREF − LLSET = 80 mV	−78	−80	−82	mV
Differential Non-Linearity			−1		+1	LSB
Line Regulation	ΔV_{FB}	VCC = 10 V to 14 V		0.003		%
Input Bias Current	I_{FB}		13.5	15	16.5	µA
FBRTN Current	I_{FBRTN}			125	200	µA
Output Current	I_{COMP}	FB forced to V_{OUT} − 3%		500		µA
Gain Bandwidth Product	$GBW_{(ERR)}$	COMP = FB		20		MHz
Slew Rate		COMP = FB		25		V/µs
LLSET Input Voltage Range	V_{LLSET}	Relative to CSREF	−250		+250	mV
LLSET Input Bias Current	I_{LLSET}		−120		+120	nA
BOOT Voltage Hold Time	t_{BOOT}	C_{DELAY} = 10 nF		2		ms
VID INPUTS						
Input Low Voltage	$V_{IL(VID)}$	VIDx, VIDSEL			0.4	V
Input High Voltage	$V_{IH(VID)}$	VIDx, VIDSEL	0.8			V
Max V_{IH} for VID on Fly[2]					1.26	V
Input Current	$I_{IN(VID)}$			−1		µA
VID Transition Delay Time[2]		VID code change to FB change	200			ns
No CPU Detection Turn-Off Delay Time[2]		VID code change to PWM going low	200			ns
OSCILLATOR						
Frequency Range[2]	f_{OSC}		0.25		5	MHz
Frequency Variation	f_{PHASE}	T_A = 25°C, R_T = 243 kΩ, 5-phase	180	200	220	kHz
		T_A = 25°C, R_T = 113 kΩ, 5-phase		400		kHz
		T_A = 25°C, R_T = 51 kΩ, 5-phase		800		kHz
Output Voltage	V_{RT}	R_T = 243 kΩ to GND	1.6	1.7	1.8	V
RAMPADJ Output Voltage	$V_{RAMPADJ}$	RAMPADJ − FB	−50		+50	mV
RAMPADJ Input Current Range	$I_{RAMPADJ}$		1		50	µA
CURRENT SENSE AMPLIFIER						
Offset Voltage	$V_{OS(CSA)}$	CSSUM − CSREF, Figure 3	−1.0		+1.0	mV
Input Bias Current	$I_{BIAS(CSSUM)}$		−50		+50	nA
Gain Bandwidth Product	$GBW_{(CSA)}$	CSSUM = CSCOMP		10		MHz
Slew Rate		C_{CSCOMP} = 10 pF		10		V/µs
Input Common-Mode Range		CSSUM and CSREF	0		3	V
Output Voltage Range			0.05		2.8	V
Output Current	I_{CSCOMP}			500		µA
Current Limit Latch-Off Delay Time	$t_{OC(DELAY)}$	C_{DELAY} = 10 nF		8		ms

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CURRENT BALANCE AMPLIFIER						
Common Mode Range	$V_{SW(X)CM}$		−600		+200	mV
Input Resistance	$R_{SW(X)}$	SWx = 0 V	35	50	65	kΩ
Input Current	$I_{SW(X)}$	SWx = 0 V	2.5	4.0	5.5	µA
Input Current Matching	$\Delta I_{SW(X)}$	SWx = 0 V	−5		+5	%
CURRENT LIMIT COMPARATOR						
Output Voltage	V_{ILIMIT}	R_{ILIMIT} = 143 kΩ	1.6	1.7	1.8	V
Output Current	I_{ILIMIT}	R_{ILIMIT} = 143 kΩ		12		µA
Maximum Output Current[2]			60			µA
Current Limit Threshold Voltage	V_{CL}	$V_{CSREF} - V_{CSCOMP}$, R_{ILIMIT} = 143 kΩ	105	120	135	mV
Current Limit Setting Ratio		V_{CL}/I_{ILIMIT}		10		mV/µA
DELAY TIMER						
Normal Mode Output Current	I_{DELAY}		12	15	18	µA
Output Current in Current Limit	$I_{DELAY(CL)}$		3.0	3.75	4.5	µA
Threshold Voltage	$V_{DELAY(TH)}$		1.6	1.7	1.8	V
SOFT START						
Output Current	I_{SS}	During start-up	12	15	18	µA
ENABLE INPUT						
Threshold Voltage	$V_{TH(EN)}$		800	850	900	mV
Hysteresis	$V_{HYS(EN)}$		80	100	120	mV
Input Current	$I_{IN(EN)}$		−1		+1	µA
Delay Time	$t_{DELAY(EN)}$	EN > 950 mV, C_{DELAY} = 10 nF		2		ms
$\overline{OD}$ OUTPUT						
Output Low Voltage	$V_{OL(\overline{OD})}$			100	500	mV
Output High Voltage	$V_{OH(\overline{OD})}$		4	5		V
THERMAL THROTTLING CONTROL						
TTSENSE Voltage Range		Internally limited	0		5.3	V
TTSENSE VRFAN Threshold Voltage			1.08	1.11	1.14	V
TTSENSE VRHOT Threshold Voltage			780	810	840	mV
TTSENSE Hysteresis				55		mV
TTSENSE Input Current			−105	−120	−135	µA
VRFAN Output Low Voltage	$V_{OL(VRFAN)}$	$I_{VRFAN (SINK)}$ = −4 mA		150	300	mV
VRHOT Output Low Voltage	$V_{OL(VRHOT)}$	$I_{VRHOT (SINK)}$ = −4 mA		150	300	mV
POWER GOOD COMPARATOR						
Undervoltage Threshold	$V_{PWRGD(UV)}$	Relative to nominal DAC output	−200	−250	−300	mV
Overvoltage Threshold	$V_{PWRGD(OV)}$	Relative to nominal DAC output	100	150	200	mV
Output Low Voltage	$V_{OL(PWRGD)}$	$I_{PWRGD(SINK)}$ = −4 mA		150	300	mV
Power Good Delay Time						
During Soft Start[2]		C_{DELAY} = 10 nF		2		ms
VID Code Changing			100	400		µs
VID Code Static				200		ns
Crowbar Trip Point	$V_{CROWBAR}$	Relative to nominal DAC output	100	150	200	mV
Crowbar Reset Point		Relative to FBRTN	320	375	430	mV
Crowbar Delay Time	$t_{CROWBAR}$	Overvoltage to PWM going low				
VID Code Changing			100	400		µs
VID Code Static				400		ns
PWM OUTPUTS						
Output Low Voltage	$V_{OL(PWM)}$	$I_{PWM(SINK)}$ = −400 µA		160	500	mV
Output High Voltage	$V_{OH(PWM)}$	$I_{PWM(SOURCE)}$ = 400 µA	4.0	5		V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY						
DC Supply Current				6	10	mA
UVLO Threshold Voltage	V_{UVLO}	VCC rising	7	7.4	7.8	V
UVLO Hysteresis			0.4	0.6	0.8	V

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
[2] Guaranteed by design or bench characterization, not tested in production.

TEST CIRCUITS

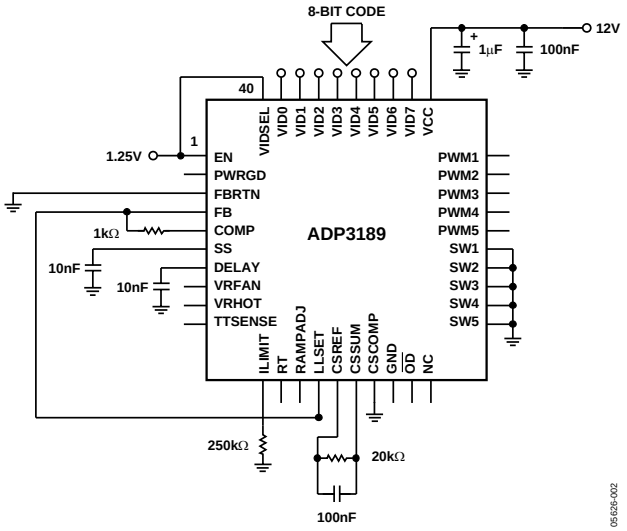

Figure 2. Closed-Loop Output Voltage Accuracy

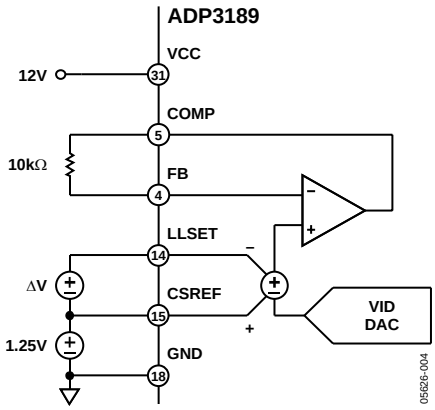

Figure 4. Positioning Voltage

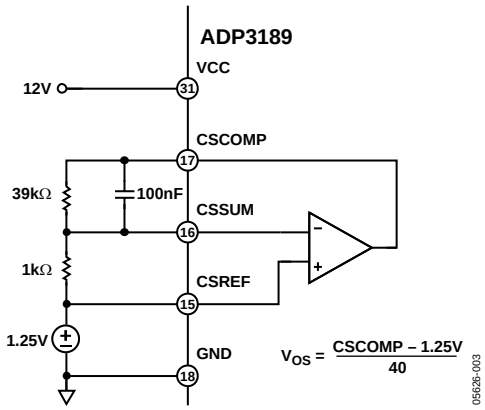

Figure 3. Current Sense Amplifier V_{OS}

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC	−0.3 V to +15 V
FBRTN	−0.3 V to +0.3 V
PWM3 to PWM5, RAMPADJ	−0.3 V to VCC + 0.3 V
SW1 to SW5	−5 V to +25 V
<200 ns	−10 V to +25 V
All Other Inputs and Outputs	−0.3 V to +5.5 V
Storage Temperature	−65°C to +150°C
Operating Ambient Temperature Range	0°C to +85°C
Operating Junction Temperature	125°C
Thermal Impedance (θ_{JA})	100°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Infrared (15 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified all other voltages re referenced to GND.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

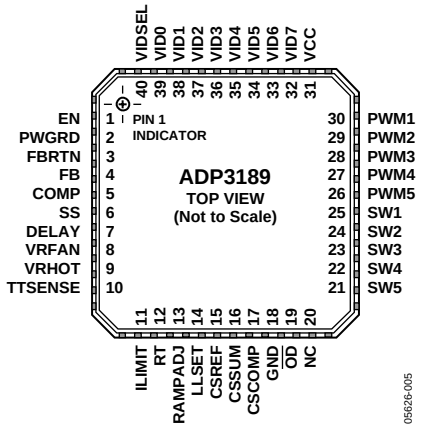

Figure 5. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	EN	Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs and pulls the PWRGD output low.
2	PWRGD	Power Good Output. Open-drain output that signals when the output voltage is outside of the proper operating range.
3	FBRTN	Feedback Return. VID DAC and error amplifier reference for remote sensing of the output voltage.
4	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage. An external resistor between this pin and the output voltage sets the no-load offset point.
5	COMP	Error Amplifier Output and Compensation Point.
6	SS	Soft Start Delay Setting Input. An external capacitor connected between this pin and GND sets the soft start ramp-up time.
7	DELAY	Delay Timer Setting Input. An external capacitor connected between this pin and GND sets the overcurrent latch-off delay time, BOOT voltage hold time, EN delay time, and PWRGD delay time.
8	VRFAN	VR Fan Activation Output. Active high open drain output that signals when the temperature at the monitoring point connected to TTSENSE exceeds the programmed VRFAN temperature threshold.
9	VRHOT	VR Hot Output. Active high open drain output that signals when the temperature at the monitoring point connected to TTSENSE exceeds the programmed VRHOT temperature threshold.
10	TTSENSE	VR Hot Thermal Throttling Sense Input. An NTC thermistor between this pin and GND is used to remotely sense the temperature at the desired thermal monitoring point.
11	ILIMIT	Current Limit Set Point. An external resistor from this pin to GND sets the current limit threshold of the converter.
12	RT	Frequency Setting Resistor Input. An external resistor connected between this pin and GND sets the oscillator frequency of the device.
13	RAMPADJ	PWM Ramp Current Input. An external resistor from the converter input voltage to this pin sets the internal PWM ramp.
14	LLSET	Output Load Line Programming Input. This pin can be directly connected to CSCOMP, or it can be connected to the center point of a resistor divider between CSCOMP and CSREF. Connecting LLSET to CSREF disables positioning.
15	CSREF	Current Sense Reference Voltage Input. The voltage on this pin is used as the reference for the current sense amplifier and the power good and crowbar functions. This pin should be connected to the common point of the output inductors.
16	CSSUM	Current Sense Summing Node. External resistors from each switch node to this pin sum the average inductor currents together to measure the total output current.
17	CSCOMP	Current Sense Compensation Point. A resistor and capacitor from this pin to CSSUM determines the gain of the current sense amplifier and the positioning loop response time.
18	GND	Ground. All internal biasing and the logic output signals of the device are referenced to this ground.
19	$\overline{OD}$	Output Disable Logic Output. This pin is actively pulled low when the ADP3189 EN input is low or when VCC is below its UVLO threshold to signal to the Driver IC that the driver high-side and low-side outputs should go low.
20	NC	No Connect.

Pin No.	Mnemonic	Description
21 to 25	SW5 to SW1	Current Balance Inputs. Inputs for measuring the current level in each phase. The SW pins of unused phases should be left open.
26 to 30	PWM5 to PMW1	Logic-Level PWM Outputs. Each output is connected to the input of an external MOSFET driver such as the ADP3120. Connecting the PWM3, PWM4, and/or PWM5 outputs to VCC will cause that phase to turn off, allowing the ADP3189 to operate as a 2-, 3-, 4-, or 5-phase controller.
31	VCC	Supply Voltage for the Device.
32 to 39	VID7 to VID0	Voltage Identification DAC Inputs. These eight pins are pulled down to GND, providing a logic zero if left open. When in normal operation mode, the DAC output programs the FB regulation voltage from 0.5 V to 1.6 V (see Table 4).
40	VIDSEL	VID DAC Selection Pin. The logic state of this pin determines whether the internal VID DAC decodes VID0 to VID7 as extended VR10 or VR11 inputs.

TYPICAL PERFORMANCE CHARACTERISTICS

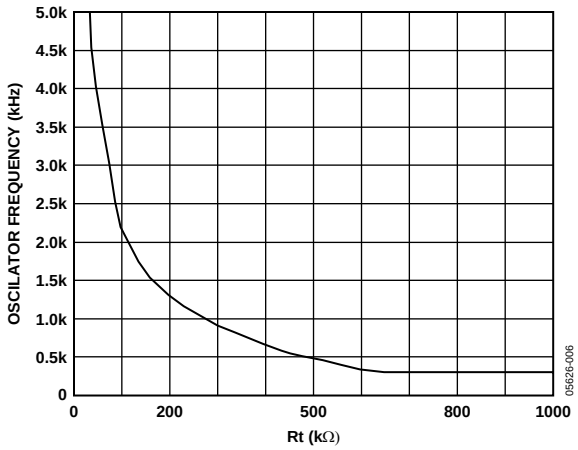

Figure 6. Master Clock Frequency vs. RT

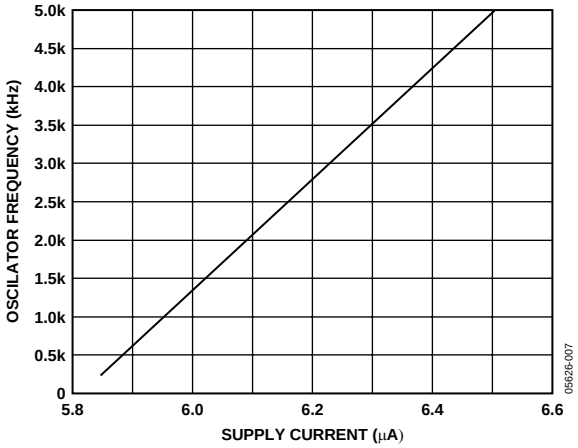

Figure 7. Oscillator Frequency vs .Supply Current

THEORY OF OPERATION

The ADP3189 combines a multimode, fixed frequency PWM control with multiphase logic outputs for use in 2-, 3-, 4-, and 5-phase synchronous buck CPU core supply power converters. The internal VID DAC is designed to interface with the Intel 8-bit VRD/VRM 11- and 7-bit VRD/VRM 10x-compatible CPUs. Multiphase operation is important for producing the high currents and low voltages demanded by today's microprocessors. Handling the high currents in a single-phase converter places high thermal demands on the components in the system, such as the inductors and MOSFETs.

The multimode control of the ADP3189 ensures a stable, high performance topology for the following:

- Balancing currents and thermals between phases
- High speed response at the lowest possible switching frequency and output decoupling
- Minimizing thermal switching losses by using lower frequency operation
- Tight load line regulation and accuracy
- High current output from having up to 5-phase operation
- Reduced output ripple due to multiphase cancellation
- PC board layout noise immunity
- Ease of use and design due to independent component selection
- Flexibility in operation for tailoring design to low cost or high performance

START-UP SEQUENCE

The ADP3189 follows the VR11 start-up sequence shown in Figure 8. After both the EN and UVLO conditions are met, the DELAY pin goes through one cycle (TD1). After this cycle, the internal oscillator is enabled. The first five clock cycles are blanked from the PWM outputs and used for phase detection as explained in the Phase Detection Sequence section. Then, the soft start ramp is enabled (TD2), and the output comes up to the boot voltage of 1.1 V. The boot hold time is determined by the DELAY pin as it goes through a second cycle (TD3). During TD3, the processor VID pins settle to the required VID code. When TD3 is over, the ADP3189 soft starts either up or down to the final VID voltage (TD4). After TD4 has been completed and the PWRGD masking time (equal to VID on the fly masking) is finished, a third ramp on the DELAY pin sets the PWRGD blanking (TD5).

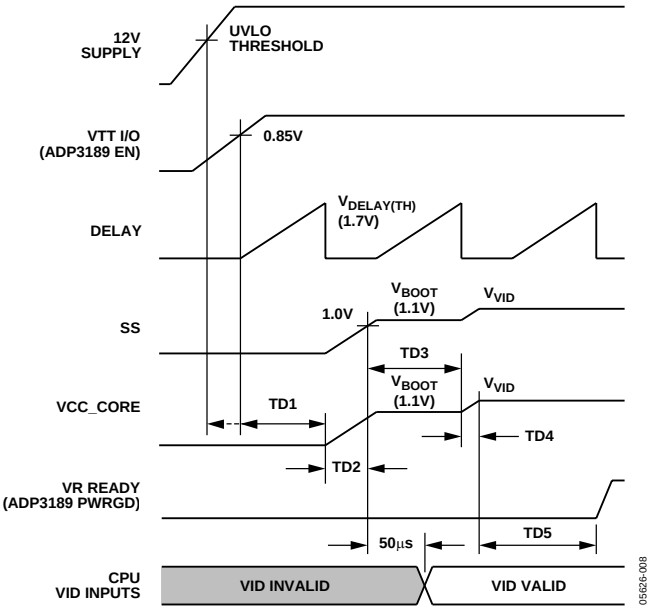

Figure 8. System Start-Up Sequence

PHASE DETECTION SEQUENCE

During start-up, the number of operational phases and their phase relationship is determined by the internal circuitry monitoring the PWM outputs. Normally, the ADP3189 operates as a 5-phase PWM controller. Connecting the PWM5 pin to VCC programs a 4-phase operation, and connecting the PWM5 pin and PWM4 pin to VCC programs a 3-phase operation. For 2-phase operation, connect PWM5, PWM4, and PWM3 to VCC.

Prior to soft start, while EN is low, the PWM3, PWM4, and PWM5 pins sink approximately 100 µA. An internal comparator checks each pin's voltage vs. a threshold of 3.15 V. If the pin is tied to VCC, it is above the threshold. Otherwise, an internal current sink pulls the pin to GND, which is below the threshold. PWM1 and PWM2 are low during the phase detection interval, which occurs during the first five clock cycles of the internal oscillator. After this time, if the remaining PWM outputs are not pulled to VCC, the 100 µA current sink is removed, and they function as normal PWM outputs. If they are pulled to VCC, the 100 µA current source is removed, and the outputs are put into a high-impedance state.

The PWM outputs are logic-level devices intended for driving external gate drivers such as the ADP3120. Since each phase is monitored independently, operation approaching 100% duty cycle is possible. Also, more than one output can be on at the same time to allow overlapping phases.

MASTER CLOCK FREQUENCY

The clock frequency of the ADP3189 is set with an external resistor connected from the RT pin to ground. The frequency follows the graph in Figure 6. To determine the frequency per phase, the clock is divided by the number of phases in use. If all phases are in use, divide by 5. If PWM5 is tied to VCC, then divide the master clock by 4 for the frequency of the remaining phases. If PWM4 and PWM5 are tied to VCC, then divide by 3. If PWM3, PWM4, and PWM5 are tied to VCC, then divide by 2.

OUTPUT VOLTAGE DIFFERENTIAL SENSING

The ADP3189 combines differential sensing with a high accuracy VID DAC and reference and a low offset error amplifier. This maintains a worst-case specification of ±7.7 mV differential sensing error over its full operating output voltage and temperature range. The output voltage is sensed between the FB pin and FBRTN pin. FB should be connected through a resistor to the regulation point, usually the remote sense pin of the microprocessor. FBRTN should be connected directly to the remote sense ground point. The internal VID DAC and precision reference are referenced to FBRTN, which has a minimal current of 125 µA to allow accurate remote sensing. The internal error amplifier compares the output of the DAC to the FB pin to regulate the output voltage.

OUTPUT CURRENT SENSING

The ADP3189 provides a dedicated current-sense amplifier (CSA) to monitor the total output current for proper voltage positioning vs. load current and for current-limit detection. Sensing the load current at the output gives the total average current being delivered to the load, which is an inherently more accurate method than peak current detection or sampling the current across a sense element such as the low-side MOSFET. This amplifier can be configured several ways, depending on the objectives of the system, as follows:

- Output inductor DCR sensing without a thermistor for lowest cost.
- Output inductor DCR sensing with a thermistor for improved accuracy with tracking of inductor temperature.
- Sense resistors for highest accuracy measurements.

The positive input of the CSA is connected to the CSREF pin, which is connected to the output voltage. The inputs to the amplifier are summed together through resistors from the sensing element, such as the switch node side of the output inductors, to the inverting input, CSSUM. The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier, and a filter capacitor is placed in parallel with this resistor. The gain of the amplifier is programmable by adjusting the feedback resistor.

An additional resistor divider connected between CSREF and CSCOMP, with the mid point connected to LLSET, can be used to set the load line required by the microprocessor. The current information is then given as CSREF – LLSET. This difference signal is used internally to offset the VID DAC for voltage positioning. The difference between CSREF and CSCOMP is then used as a differential input for the current-limit comparator. This allows for the load line to be set independently of the current-limit threshold. In the event that the current limit threshold and load line are not independent, the resistor divider between CSREF and CSCOMP can be removed and the CSCOMP pin can be directly connected to LLSET. To disable voltage positioning entirely (that is, no load line) connect LLSET to CSREF.

To provide the best accuracy for sensing current, the CSA is designed to have a low offset input voltage. Also, the sensing gain is determined by external resistors, so that it can be made extremely accurate.

ACTIVE IMPEDANCE CONTROL MODE

For controlling the dynamic output voltage droop as a function of output current, a signal proportional to the total output current at the LLSET pin can be scaled to be equal to the droop impedance of the regulator times the output current. This droop voltage is then used to set the input control voltage to the system. The droop voltage is subtracted from the DAC reference input voltage directly to tell the error amplifier where the output voltage should be. This allows enhanced feed-forward response.

CURRENT CONTROL MODE AND THERMAL BALANCE

The ADP3189 has individual inputs (SW1 to SW5) for each phase, which are used for monitoring the current of each phase. This information is combined with an internal ramp to create a current balancing feedback system that has been optimized for initial current balance accuracy and dynamic thermal balancing during operation. This current balance information is independent of the average output current information used for positioning as described in the Output Current Sensing section.

The magnitude of the internal ramp can be set to optimize the transient response of the system. It also monitors the supply voltage for feed-forward control for changes in the supply. A resistor connected from the power input voltage to the RAMPADJ pin determines the slope of the internal PWM ramp. External resistors can be placed in series with individual phases to create an intentional current imbalance if desired, such as when one phase has better cooling and can support higher currents. Resistors R_{SW1} through R_{SW5} (see the Typical Application Circuit in Figure 11) can be used for adjusting thermal balance. It is best to have the ability to add these resistors during the initial design, so ensure that placeholders are provided in the layout.

To increase the current in any given phase, enlarge R_{SW} for that phase (make R_{SW} = 0 for the hottest phase and do not change during balancing). Increasing R_{SW} to only 500 Ω makes a substantial increase in phase current. Increase each R_{SW} value by small amounts to achieve balance, starting with the coolest phase first.

VOLTAGE CONTROL MODE

A high gain-bandwidth voltage mode error amplifier is used for the voltage-mode control loop. The control input voltage to the positive input is set via the VID logic according to the voltages listed in Table 4.

This voltage is also offset by the droop voltage for active positioning of the output voltage as a function of current, commonly known as active voltage positioning. The output of the amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.

The negative input (FB) is tied to the output sense location with a resistor R_B and is used for sensing and controlling the output voltage at this point. A current source from the FB pin flowing through R_B is used for setting the no-load offset voltage from the VID voltage. The no-load voltage is negative with respect to the VID DAC. The main loop compensation is incorporated into the feedback network between FB and COMP.

DELAY TIMER

The delay times for the start-up timing sequence are set with a capacitor from the DELAY pin to ground. In UVLO, or when EN is logic low, the DELAY pin is held at ground. After the UVLO and EN signals are asserted, the first delay time (TD1 in Figure 8) is initiated. A 15 µA current flows out of the DELAY pin to charge C_{DLY}. A comparator monitors the DELAY voltage with a threshold of 1.7 V. The delay time is therefore set by the 15 µA charging a capacitor from 0 V to 1.7 V. This DELAY pin is used for multiple delay timings (TD1, TD3, and TD5) during the start-up sequence. Also, DELAY is used for timing the current limit latch off, as explained in the Current Limit, Short Circuit, and Latch-Off Protection section.

SOFT START

The Soft Start times for the output voltage are set with a capacitor from the SS pin to ground. After TD1 and the phase detection cycle have been completed, the SS time (TD2 in Figure 8) starts. The SS pin is disconnected from GND, and the capacitor is charged up to the 1.1 V boot voltage by the SS amplifier, which has a limited output current of 15 µA. The voltage at the FB pin follows the ramping voltage on the SS pin, limiting the inrush current during start-up. The soft start time depends on the value of the boot voltage and C_{SS}.

Once the SS voltage is within 100 mV of the boot voltage, the boot voltage delay time (TD3) is started. The end of the boot voltage delay time signals the beginning of the second soft start time (TD4). The SS voltage now changes from the boot voltage to the programmed VID DAC voltage (either higher or lower) using the SS amplifier with the limited output current of 15 µA. The voltage of the FB pin follows the ramping voltage of the SS pin, limiting the inrush current during the transition from the boot voltage to the final DAC voltage. The second soft start time depends on the boot voltage, the programmed VID DAC voltage, and C_{SS}.

If either EN is taken low or VCC drops below UVLO, DELAY and SS are reset to ground to be ready for another soft start cycle. Figure 9 shows typical start-up waveforms for the ADP3189.

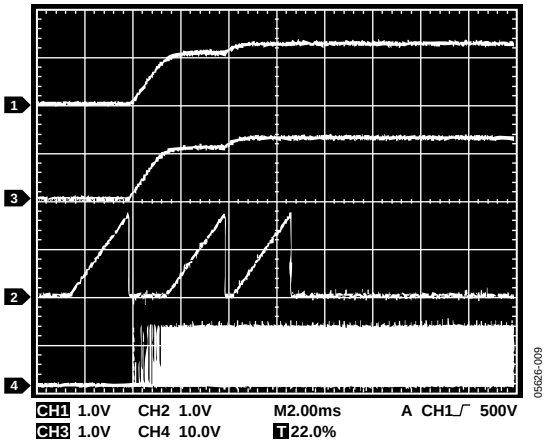

Figure 9. Typical Start-up Waveforms
Channel 1: CSREF, Channel 2: DELAY,
Channel 3: SS, Channel 4: Phase 1 Switch Node

CURRENT LIMIT, SHORT CIRCUIT, AND LATCH-OFF PROTECTION

The ADP3189 compares a programmable current-limit set point to the voltage from the output of the current-sense amplifier. The level of current limit is set with the resistor from the ILIMIT pin to ground. During operation, the voltage on ILIMIT is 1.7 V. The current through the external resistor is internally scaled to give a current limit threshold of 10 mV/μA. If the difference in voltage between CSREF and CSCOMP rises above the current limit threshold, the internal current limit amplifier controls the internal COMP voltage to maintain the average output current at the limit.

If the limit is reached and TD5 has completed, a latch-off delay time starts, and the controller shuts down if the fault is not removed. The current limit delay time shares the DELAY pin timing capacitor with the start-up sequence timing. However, during current limit, the DELAY pin current is reduced to 3.75 μA. A comparator monitors the DELAY voltage and shuts off the controller when the voltage reaches 1.7 V. Therefore, the current limit latch-off delay time is set by the current of 3.75 μA, charging the delay capacitor from 0 V to 1.7 V. This delay is four times longer than the delay time during the start-up sequence.

The current limit delay time starts only after the TD5 has completed. If there is a current limit during start-up, the ADP3189 goes through TD1 to TD5, and then starts the latch-off time. Because the controller continues to cycle the phases during the latch-off delay time, if the short is removed before the 1.7 V threshold is reached, the controller returns to normal operation, and the DELAY capacitor is reset to GND.

The latch-off function can be reset by either removing and reapplying the supply voltage to the ADP3189, or by toggling the EN pin low for a short time. To disable the short circuit latch-off function, an external resistor should be placed in parallel with C_{DLY}. This prevents the DELAY capacitor from charging up to the 1.7 V threshold. The addition of this resistor will cause a slight increase in the delay times.

During start-up, when the output voltage is below 200 mV, a secondary current limit is active. This is necessary because the voltage swing of CSCOMP cannot go below ground. This secondary current limit controls the internal COMP voltage to the PWM comparators to 1.5 V. This limits the voltage drop across the low-side MOSFETs through the current balance circuitry. An inherent per-phase current limit protects individual phases if one or more phases stop functioning because of a faulty component. This limit is based on the maximum normal mode COMP voltage. Typical overcurrent latch-off waveforms are shown in Figure 10.

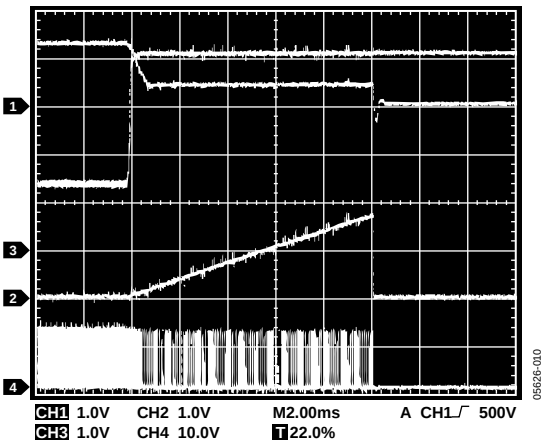

Figure 10. Overcurrent Latch-Off Waveforms
Channel 1: CSREF, Channel 2: DELAY,
Channel 3: COMP, Channel 4: Phase 1 Switch Node

DYNAMIC VID

The ADP3189 has the ability to dynamically change the VID inputs while the controller is running. This allows the output voltage to change while the supply is running and supplying current to the load. This is commonly referred to as VID on-the-fly (OTF). A VID OTF can occur under light or heavy load conditions. The processor signals the controller by changing the VID inputs in multiple steps from the start code to the finish code. This change can be positive or negative.

When a VID input changes state, the ADP3189 detects the change and ignores the DAC inputs for a minimum of 200 ns. This time prevents a false code due to logic skew while the eight VID inputs are changing. Additionally, the first VID change initiates the PWRGD and crowbar blanking functions for a minimum of 100 μs to prevent a false PWRGD or crowbar event. Each VID change resets the internal timer.

POWER GOOD MONITORING

The power good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open-drain output whose high level, when connected to a pull-up resistor, indicates that the output voltage is within the nominal limits specified based on the VID voltage setting. PWRGD goes low if the output voltage is outside of this specified range, if the VID DAC inputs are in no CPU mode, or whenever the EN pin is pulled low. PWRGD is blanked during a VID OTF event for a period of 400 μs to prevent false signals during the time the output is changing.

The PWRGD circuitry also incorporates an initial turn-on delay time (TD5), based on the DELAY timer. Prior to the SS voltage reaching the programmed VID DAC voltage and the PWRGD masking time finishing, the PWRGD pin is held low. Once the SS pin is within 100 mV of the programmed DAC voltage, the capacitor on the DELAY pin begins to charge up. A comparator monitors the DELAY voltage and enables PWRGD when the voltage reaches 1.7 V. The PWRGD delay time is, therefore, set by a current of 15 μA, charging a capacitor from 0 V to 1.7 V.

OUTPUT CROWBAR

As part of the protection for the load and output components of the supply, the PWM outputs are driven low, turning on the low-side MOSFETs, when the output voltage exceeds the upper crowbar threshold. This crowbar action stops once the output voltage falls below the release threshold of approximately 375 mV.

Turning on the low-side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output overvoltage is due to a short in the high-side MOSFET, this action current-limits the input supply or blows its fuse, protecting the microprocessor from being destroyed.

OUTPUT ENABLE AND UVLO

For the ADP3189 to begin switching, the input supply (VCC) to the controller must be higher than the UVLO threshold, and the EN pin must be higher than its 0.85 V threshold. This initiates a system start up sequence. If either UVLO or EN is less than their respective thresholds, the ADP3189 is disabled. This holds the PWM outputs at ground, shorts the DELAY capacitor to ground, and forces PWRGD and $\overline{OD}$ signals low.

In the application circuit, the $\overline{OD}$ pin should be connected to the $\overline{OD}$ inputs of the ADP3120 driver. Grounding $\overline{OD}$ disables the drivers such that both DRVH and DRVL are grounded. This feature is important in preventing the discharge of the output capacitors when the controller is shut off. If the driver outputs were not disabled, a negative voltage can be generated during output due to the high current discharge of the output capacitors through the inductors.

THERMAL MONITORING

The ADP3189 includes a thermal monitoring circuit to detect when a point on the VR has exceeded two different user-defined temperatures. The thermal monitoring circuit requires an NTC thermistor to be placed between TTSENSE and GND. A fixed current of 120 μA is sourced out of the TTSENSE pin and into the thermistor. The current source is internally limited to 5 V. An internal circuit compares the TTSENSE voltage to a 1.11 V and a 0.81 V threshold, and outputs an open-drain signal at the VRFAN and VRHOT outputs, respectively. Once the voltage on the TTSENSE pin goes below its respective threshold, the open drain outputs assert high to signal the system that an overtemperature event has occurred. Since the TTSENSE voltage changes slowly with respect to time, 55 mV of hysteresis is built into these comparators. The thermal monitoring circuitry does not depend on EN and is active when UVLO is above its threshold. When UVLO is below its threshold, VRFAN and VRHOT are forced low.

Table 4.VR11 and VR10.x VID Codes for the ADP3189

VR11 DAC CODES: VIDSEL = HIGH									VR10.x DAC CODES: VIDSEL = LOW						
OUTPUT	**VID7**	**VID6**	**VID5**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID5**	**VID6**
OFF	0	0	0	0	0	0	0	0	N/A						
OFF	0	0	0	0	0	0	0	1	N/A						
1.60000	0	0	0	0	0	0	1	0	0	1	0	1	0	1	1
1.59375	0	0	0	0	0	0	1	1	0	1	0	1	0	1	0
1.58750	0	0	0	0	0	1	0	0	0	1	0	1	1	0	1
1.58125	0	0	0	0	0	1	0	1	0	1	0	1	1	0	0
1.57500	0	0	0	0	0	1	1	0	0	1	0	1	1	1	1
1.56875	0	0	0	0	0	1	1	1	0	1	0	1	1	1	0
1.56250	0	0	0	0	1	0	0	0	0	1	1	0	0	0	1
1.55625	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0
1.55000	0	0	0	0	1	0	1	0	0	1	1	0	0	1	1
1.54375	0	0	0	0	1	0	1	1	0	1	1	0	0	1	0
1.53750	0	0	0	0	1	1	0	0	0	1	1	0	1	0	1
1.53125	0	0	0	0	1	1	0	1	0	1	1	0	1	0	0
1.52500	0	0	0	0	1	1	1	0	0	1	1	0	1	1	1
1.51875	0	0	0	0	1	1	1	1	0	1	1	0	1	1	0
1.51250	0	0	0	1	0	0	0	0	0	1	1	1	0	0	1
1.50625	0	0	0	1	0	0	0	1	0	1	1	1	0	0	0
1.50000	0	0	0	1	0	0	1	0	0	1	1	1	0	1	1
1.49375	0	0	0	1	0	0	1	1	0	1	1	1	0	1	0
1.48750	0	0	0	1	0	1	0	0	0	1	1	1	1	0	1
1.48125	0	0	0	1	0	1	0	1	0	1	1	1	1	0	0
1.47500	0	0	0	1	0	1	1	0	0	1	1	1	1	1	1
1.46875	0	0	0	1	0	1	1	1	0	1	1	1	1	1	0
1.46250	0	0	0	1	1	0	0	0	1	0	0	0	0	0	1
1.45625	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0
1.45000	0	0	0	1	1	0	1	0	1	0	0	0	0	1	1
1.44375	0	0	0	1	1	0	1	1	1	0	0	0	0	1	0
1.43750	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1
1.43125	0	0	0	1	1	1	0	1	1	0	0	0	1	0	0
1.42500	0	0	0	1	1	1	1	0	1	0	0	0	1	1	1
1.41875	0	0	0	1	1	1	1	1	1	0	0	0	1	1	0
1.41250	0	0	1	0	0	0	0	0	1	0	0	1	0	0	1
1.40625	0	0	1	0	0	0	0	1	1	0	0	1	0	0	0
1.40000	0	0	1	0	0	0	1	0	1	0	0	1	0	1	1
1.39375	0	0	1	0	0	0	1	1	1	0	0	1	0	1	0
1.38750	0	0	1	0	0	1	0	0	1	0	0	1	1	0	1
1.38125	0	0	1	0	0	1	0	1	1	0	0	1	1	0	0
1.37500	0	0	1	0	0	1	1	0	1	0	0	1	1	1	1
1.36875	0	0	1	0	0	1	1	1	1	0	0	1	1	1	0
1.36250	0	0	1	0	1	0	0	0	1	0	1	0	0	0	1
1.35625	0	0	1	0	1	0	0	1	1	0	1	0	0	0	0
1.35000	0	0	1	0	1	0	1	0	1	0	1	0	0	1	1
1.34375	0	0	1	0	1	0	1	1	1	0	1	0	0	1	0
1.33750	0	0	1	0	1	1	0	0	1	0	1	0	1	0	1
1.33125	0	0	1	0	1	1	0	1	1	0	1	0	1	0	0
1.32500	0	0	1	0	1	1	1	0	1	0	1	0	1	1	1
1.31875	0	0	1	0	1	1	1	1	1	0	1	0	1	1	0

	VR11 DAC CODES: VIDSEL = HIGH								VR10.x DAC CODES: VIDSEL = LOW						
OUTPUT	**VID7**	**VID6**	**VID5**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID5**	**VID6**
1.31250	0	0	1	1	0	0	0	0	1	0	1	1	0	0	1
1.30625	0	0	1	1	0	0	0	1	1	0	1	1	0	0	0
1.30000	0	0	1	1	0	0	1	0	1	0	1	1	0	1	1
1.29375	0	0	1	1	0	0	1	1	1	0	1	1	0	1	0
1.28750	0	0	1	1	0	1	0	0	1	0	1	1	1	0	1
1.28125	0	0	1	1	0	1	0	1	1	0	1	1	1	0	0
1.27500	0	0	1	1	0	1	1	0	1	0	1	1	1	1	1
1.26875	0	0	1	1	0	1	1	1	1	0	1	1	1	1	0
1.26250	0	0	1	1	1	0	0	0	1	1	0	0	0	0	1
1.25625	0	0	1	1	1	0	0	1	1	1	0	0	0	0	0
1.25000	0	0	1	1	1	0	1	0	1	1	0	0	0	1	1
1.24375	0	0	1	1	1	0	1	1	1	1	0	0	0	1	0
1.23750	0	0	1	1	1	1	0	0	1	1	0	0	1	0	1
1.23125	0	0	1	1	1	1	0	1	1	1	0	0	1	0	0
1.22500	0	0	1	1	1	1	1	0	1	1	0	0	1	1	1
1.21875	0	0	1	1	1	1	1	1	1	1	0	0	1	1	0
1.21250	0	1	0	0	0	0	0	0	1	1	0	1	0	0	1
1.20625	0	1	0	0	0	0	0	1	1	1	0	1	0	0	0
1.20000	0	1	0	0	0	0	1	0	1	1	0	1	0	1	1
1.19375	0	1	0	0	0	0	1	1	1	1	0	1	0	1	0
1.18750	0	1	0	0	0	1	0	0	1	1	0	1	1	0	1
1.18125	0	1	0	0	0	1	0	1	1	1	0	1	1	0	0
1.17500	0	1	0	0	0	1	1	0	1	1	0	1	1	1	1
1.16875	0	1	0	0	0	1	1	1	1	1	0	1	1	1	0
1.16250	0	1	0	0	1	0	0	0	1	1	1	0	0	0	1
1.15625	0	1	0	0	1	0	0	1	1	1	1	0	0	0	0
1.15000	0	1	0	0	1	0	1	0	1	1	1	0	0	1	1
1.14375	0	1	0	0	1	0	1	1	1	1	1	0	0	1	0
1.13750	0	1	0	0	1	1	0	0	1	1	1	0	1	0	1
1.13125	0	1	0	0	1	1	0	1	1	1	1	0	1	0	0
1.12500	0	1	0	0	1	1	1	0	1	1	1	0	1	1	1
1.11875	0	1	0	0	1	1	1	1	1	1	1	0	1	1	0
1.11250	0	1	0	1	0	0	0	0	1	1	1	1	0	0	1
1.10625	0	1	0	1	0	0	0	1	1	1	1	1	0	0	0
1.10000	0	1	0	1	0	0	1	0	1	1	1	1	0	1	1
1.09375	0	1	0	1	0	0	1	1	1	1	1	1	0	1	0
OFF	N/A								1	1	1	1	1	0	1
OFF	N/A								1	1	1	1	1	0	0
OFF	N/A								1	1	1	1	1	1	1
OFF	N/A								1	1	1	1	1	1	0
1.08750	0	1	0	1	0	1	0	0	0	0	0	0	0	0	1
1.08125	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0
1.07500	0	1	0	1	0	1	1	0	0	0	0	0	0	1	1
1.06875	0	1	0	1	0	1	1	1	0	0	0	0	0	1	0
1.06250	0	1	0	1	1	0	0	0	0	0	0	0	1	0	1
1.05625	0	1	0	1	1	0	0	1	0	0	0	0	1	0	0
1.05000	0	1	0	1	1	0	1	0	0	0	0	0	1	1	1
1.04375	0	1	0	1	1	0	1	1	0	0	0	0	1	1	0
1.03750	0	1	0	1	1	1	0	0	0	0	0	1	0	0	1

VR11 DAC CODES: VIDSEL = HIGH									VR10.x DAC CODES: VIDSEL = LOW						
OUTPUT	**VID7**	**VID6**	**VID5**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID5**	**VID6**
1.03125	0	1	0	1	1	1	0	1	0	0	0	1	0	0	0
1.02500	0	1	0	1	1	1	1	0	0	0	0	1	0	1	1
1.01875	0	1	0	1	1	1	1	1	0	0	0	1	0	1	0
1.01250	0	1	1	0	0	0	0	0	0	0	0	1	1	0	1
1.00625	0	1	1	0	0	0	0	1	0	0	0	1	1	0	0
1.00000	0	1	1	0	0	0	1	0	0	0	0	1	1	1	1
0.99375	0	1	1	0	0	0	1	1	0	0	0	1	1	1	0
0.98750	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
0.98125	0	1	1	0	0	1	0	1	0	0	1	0	0	0	0
0.97500	0	1	1	0	0	1	1	0	0	0	1	0	0	1	1
0.96875	0	1	1	0	0	1	1	1	0	0	1	0	0	1	0
0.96250	0	1	1	0	1	0	0	0	0	0	1	0	1	0	1
0.95625	0	1	1	0	1	0	0	1	0	0	1	0	1	0	0
0.95000	0	1	1	0	1	0	1	0	0	0	1	0	1	1	1
0.94375	0	1	1	0	1	0	1	1	0	0	1	0	1	1	0
0.93750	0	1	1	0	1	1	0	0	0	0	1	1	0	0	1
0.93125	0	1	1	0	1	1	0	1	0	0	1	1	0	0	0
0.92500	0	1	1	0	1	1	1	0	0	0	1	1	0	1	1
0.91875	0	1	1	0	1	1	1	1	0	0	1	1	0	1	0
0.91250	0	1	1	1	0	0	0	0	0	0	1	1	1	0	1
0.90625	0	1	1	1	0	0	0	1	0	0	1	1	1	0	0
0.90000	0	1	1	1	0	0	1	0	0	0	1	1	1	1	1
0.89375	0	1	1	1	0	0	1	1	0	0	1	1	1	1	0
0.88750	0	1	1	1	0	1	0	0	0	1	0	0	0	0	1
0.88125	0	1	1	1	0	1	0	1	0	1	0	0	0	0	0
0.87500	0	1	1	1	0	1	1	0	0	1	0	0	0	1	1
0.86875	0	1	1	1	0	1	1	1	0	1	0	0	0	1	0
0.86250	0	1	1	1	1	0	0	0	0	1	0	0	1	0	1
0.85625	0	1	1	1	1	0	0	1	0	1	0	0	1	0	0
0.85000	0	1	1	1	1	0	1	0	0	1	0	0	1	1	1
0.84375	0	1	1	1	1	0	1	1	0	1	0	0	1	1	0
0.83750	0	1	1	1	1	1	0	0	0	1	0	1	0	0	1
0.83125	0	1	1	1	1	1	0	1	0	1	0	1	0	0	0
0.82500	0	1	1	1	1	1	1	0	N/A						
0.81875	0	1	1	1	1	1	1	1	N/A						
0.81250	1	0	0	0	0	0	0	0	N/A						
0.80625	1	0	0	0	0	0	0	1	N/A						
0.80000	1	0	0	0	0	0	1	0	N/A						
0.79375	1	0	0	0	0	0	1	1	N/A						
0.78750	1	0	0	0	0	1	0	0	N/A						
0.78125	1	0	0	0	0	1	0	1	N/A						
0.77500	1	0	0	0	0	1	1	0	N/A						
0.76875	1	0	0	0	0	1	1	1	N/A						
0.76250	1	0	0	0	1	0	0	0	N/A						
0.75625	1	0	0	0	1	0	0	1	N/A						
0.75000	1	0	0	0	1	0	1	0	N/A						
0.74375	1	0	0	0	1	0	1	1	N/A						
0.73750	1	0	0	0	1	1	0	0	N/A						
0.73125	1	0	0	0	1	1	0	1	N/A						

VR11 DAC CODES: VIDSEL = HIGH									VR10.x DAC CODES: VIDSEL = LOW						
OUTPUT	**VID7**	**VID6**	**VID5**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID4**	**VID3**	**VID2**	**VID1**	**VID0**	**VID5**	**VID6**
0.72500	1	0	0	0	1	1	1	0	N/A						
0.71875	1	0	0	0	1	1	1	1	N/A						
0.71250	1	0	0	1	0	0	0	0	N/A						
0.70625	1	0	0	1	0	0	0	1	N/A						
0.70000	1	0	0	1	0	0	1	0	N/A						
0.69375	1	0	0	1	0	0	1	1	N/A						
0.68750	1	0	0	1	0	1	0	0	N/A						
0.68125	1	0	0	1	0	1	0	1	N/A						
0.67500	1	0	0	1	0	1	1	0	N/A						
0.66875	1	0	0	1	0	1	1	1	N/A						
0.66250	1	0	0	1	1	0	0	0	N/A						
0.65625	1	0	0	1	1	0	0	1	N/A						
0.65000	1	0	0	1	1	0	1	0	N/A						
0.64375	1	0	0	1	1	0	1	1	N/A						
0.63750	1	0	0	1	1	1	0	0	N/A						
0.63125	1	0	0	1	1	1	0	1	N/A						
0.62500	1	0	0	1	1	1	1	0	N/A						
0.61875	1	0	0	1	1	1	1	1	N/A						
0.61250	1	0	1	0	0	0	0	0	N/A						
0.60625	1	0	1	0	0	0	0	1	N/A						
0.60000	1	0	1	0	0	0	1	0	N/A						
0.59375	1	0	1	0	0	0	1	1	N/A						
0.58750	1	0	1	0	0	1	0	0	N/A						
0.58125	1	0	1	0	0	1	0	1	N/A						
0.57500	1	0	1	0	0	1	1	0	N/A						
0.56875	1	0	1	0	0	1	1	1	N/A						
0.56250	1	0	1	0	1	0	0	0	N/A						
0.55625	1	0	1	0	1	0	0	1	N/A						
0.55000	1	0	1	0	1	0	1	0	N/A						
0.54375	1	0	1	0	1	0	1	1	N/A						
0.53750	1	0	1	0	1	1	0	0	N/A						
0.53125	1	0	1	0	1	1	0	1	N/A						
0.52500	1	0	1	0	1	1	1	0	N/A						
0.51875	1	0	1	0	1	1	1	1	N/A						
0.51250	1	0	1	1	0	0	0	0	N/A						
0.50625	1	0	1	1	0	0	0	1	N/A						
0.50000	1	0	1	1	0	0	1	0	N/A						
OFF	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0
OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

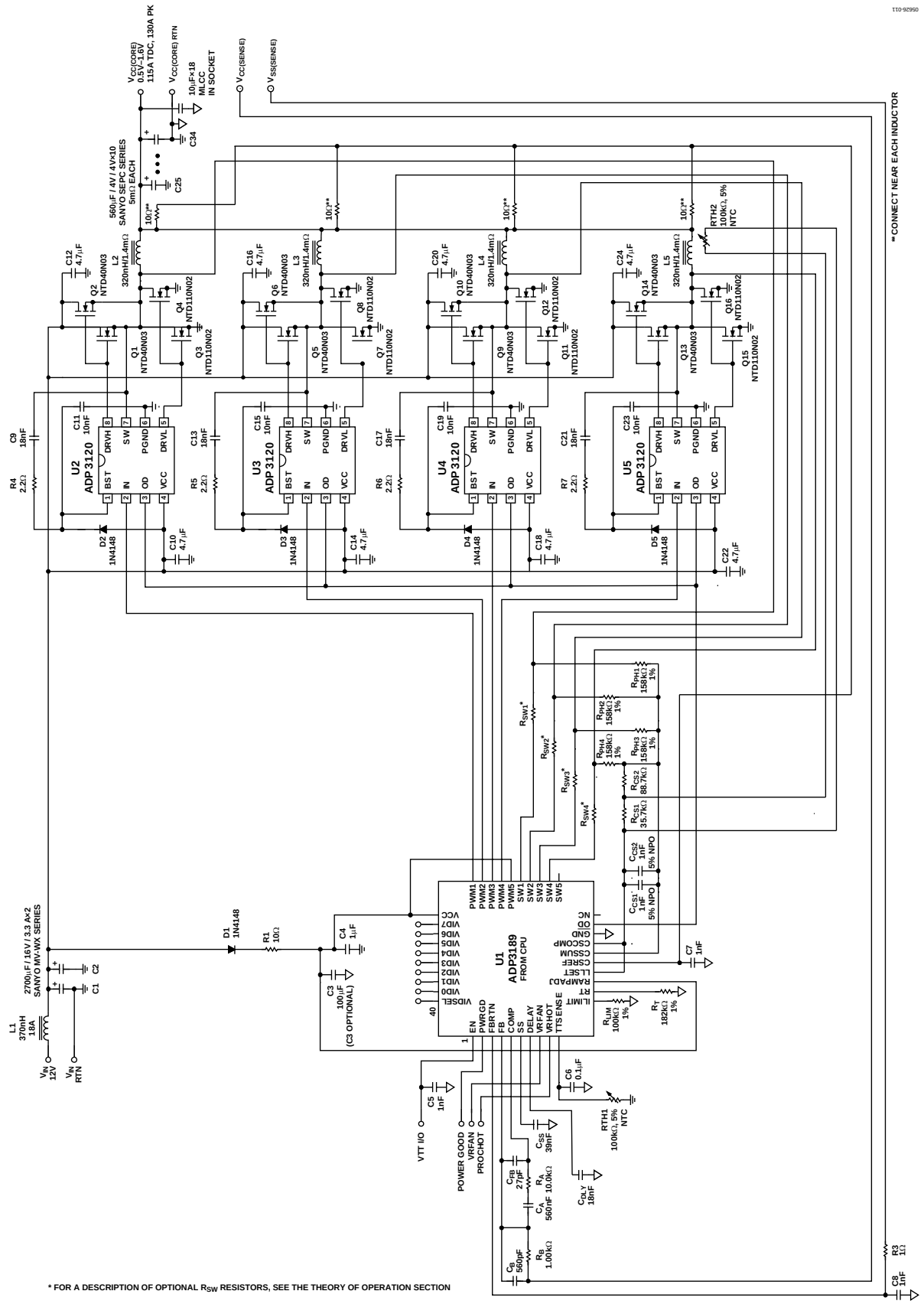

Figure 11.Typical 4-Phase Application Circuit

APPLICATION INFORMATION

The design parameters for a typical Intel VRD 11 compliant CPU application are as follows:

- Input voltage (V_{IN}) = 12 V
- VID setting voltage (V_{VID}) = 1.300 V
- Duty cycle (D) = 0.108
- Nominal output voltage at no load (V_{ONL}) = 1.285 V
- Nominal output voltage at 115 A load (V_{OFL}) = 1.170 V
- Static output voltage drop based on a 1.0 mΩ load line (R_O) from no load to full load (V_D) = $V_{ONL} - V_{OFL}$ = 1.285 V − 1.170 V = 115 mV
- Maximum output current (I_O) = 130 A
- Maximum output current step (ΔI_O) = 100 A
- Maximum output current slew-rate (S_R) = 200 A/μ sec
- Number of phases (n) = 4
- Switching frequency per phase (f_{SW}) = 330 kHz

SETTING THE CLOCK FREQUENCY

The ADP3189 uses a fixed-frequency control architecture. The frequency is set by an external timing resistor (R_T). The clock frequency and the number of phases determine the switching frequency per phase, which relates directly to switching losses and the sizes of the inductors, and of the input and output capacitors. With n = 4 for four phases, a clock frequency of 1.32 MHz sets the switching frequency (f_{SW}) of each phase to 330 kHz, which represents a practical trade-off between the switching losses and the sizes of the output filter components. Equation 1 shows that to achieve a 1.32 MHz oscillator frequency, the correct value for R_T is 181 kΩ. Alternatively, the value for R_T can be calculated using

$$R_T = \frac{1}{n \times f_{SW} \times 3.9\ \text{pF}} - 13\ \text{k}\Omega \quad (1)$$

where 3.9 pF and 13 kΩ are internal IC component values. For good initial accuracy and frequency stability, a 1% resistor is recommended.

SOFT START DELAY TIME

The value of C_{SS} sets the soft start time. The ramp is generated with a 15 μA internal current source. The value for C_{SS} can be found using:

$$C_{SS} = 15\,\mu\text{A} \times \frac{TD2}{V_{BOOT}} \quad (2)$$

where *TD2* is the desired soft start time and V_{BOOT} is internally set to 1.1 V. Assuming a desired *TD2* time of 3 ms, C_{SS} is 41 nF. The closest standard value for C_{SS} is 39 nF. Although C_{SS} also controls the time delay for *TD4* (which is determined by the final VID voltage), the minimum specification for *TD4* is 0 ns. This means that as long as the *TD2* time requirement is met, *TD4* will be within the specification.

CURRENT LIMIT LATCH-OFF DELAY TIMES

The start-up and current limit delay times are determined by the capacitor connected to the DELAY pin. The first step is to set C_{DLY} for the TD1, TD3, and TD5 delay times (see Figure 8). The DELAY ramp (I_{DELAY}) is generated using a 15 μA internal current source. The value for C_{DLY} can be approximated using:

$$C_{DLY} = I_{DELAY} \times \frac{TD(x)}{V_{DELAY(TH)}} \quad (3)$$

where *TD(x)* is the desired delay time for TD1, TD3, and TD5. The DELAY threshold voltage ($V_{DELAY(TH)}$) is given as 1.7 V. In this example, 2 ms is chosen for all three delay times, which meets Intel's specification. Solving for C_{DLY} gives a value of 17.6 nF. The closest standard value for C_{DLY} is 18 nF.

When the ADP3189 goes into current limit, the internal current source changes from 15 μA to 3.75 μA. This makes the latch-off delay time 4 times longer than the start-up delay time. Longer latch-off delay times can be achieved by placing a resistor in parallel with C_{DLY}.

INDUCTOR SELECTION

The choice of inductance for the inductor determines the ripple current in the inductor. Less inductance leads to more ripple current, which increases the output ripple voltage and conduction losses in the MOSFETs, but allows using smaller inductors and, for a specified peak-to-peak transient deviation, less total output capacitance. Conversely, a higher inductance means lower ripple current and reduced conduction losses, but requires larger inductors and more output capacitance for the same peak-to-peak transient deviation.

In any multiphase converter, a practical value for the peak-to-peak inductor ripple current is less than 50% of the maximum dc current in the same inductor. Equation 4 shows the relationship between the inductance, oscillator frequency, and peak-to-peak ripple current in the inductor.

Equation 5 can be used to determine the minimum inductance based on a given output ripple voltage.

$$I_R = \frac{V_{VID} \times (1-D)}{f_{SW} \times L} \quad (4)$$

$$L \geq \frac{V_{VID} \times R_O \times \left(1-(n \times D)\right)}{f_{SW} \times V_{RIPPLE}} \quad (5)$$

Solving Equation 5 for an 8 mV p-p output ripple voltage yields

$$L \geq \frac{1.3\ \text{V} \times 1.0\ \text{m}\Omega \times (1-0.432)}{330\ \text{kHz} \times 8\ \text{mV}} = 280\ \text{nH}$$

If the resulting ripple voltage is less than that designed for, the inductor can be made smaller until the ripple value is met. This allows optimal transient response and minimum output decoupling.

The smallest possible inductor should be used to minimize the number of output capacitors. For this example, choosing a 320 nH inductor is a good starting point and gives a calculated ripple current of 11 A. The inductor should not saturate at the peak current of 35.5 A and should be able to handle the sum of the power dissipation caused by the average current of 30 A in the winding and core loss.

Another important factor in the inductor design is the DCR (R_L), which is used for measuring the phase currents. A large DCR can cause excessive power losses, while too small a value can lead to increased measurement error. A good rule is to have the DCR be about 1 to 1½ times the droop resistance (R_O). This example uses an inductor with a DCR of 1.4 mΩ.

DESIGNING AN INDUCTOR

Once the inductance and DCR are known, the next step is to either design an inductor or to find a standard inductor that comes as close as possible to meeting the overall design goals. It is also important to have the inductance and DCR tolerance specified to control the accuracy of the system. 15% inductance and 7% DCR, at room temperature, are reasonable tolerances most manufacturers can meet.

The first decision in designing the inductor is choosing the core material. Several possibilities for providing low core loss at high frequencies include the powder cores (for example, Kool-Mμ® from Magnetics, Inc. or from Micrometals) and the gapped soft ferrite cores (for example, 3F3 or 3F4 from Philips). Low frequency powdered iron cores should be avoided due to their high core loss, especially when the inductor value is relatively low and the ripple current is high.

The best choice for a core geometry is a closed-loop type such as a potentiometer core; PQ, U, or E core; or toroid. A good compromise between price and performance is a core with a toroidal shape.

Many useful magnetics design references are available for quickly designing a power inductor, such as

- Magnetic Designer Software
  Intusoft (www.intusoft.com)
- *Designing Magnetic Components for High-Frequency DC-DCConverters*, by William T. McLyman, Kg Magnetics, Inc., ISBN 1883107008

Selecting a Standard Inductor

The following power inductor manufacturers can provide design consultation and deliver power inductors optimized for high power applications upon request.

- Coilcraft
  www.coilcraft.com
- Coiltronics
  www.coiltronics.com
- Sumida Electric Company
  www.sumida.com
- Vishay Intertechnology
  www.vishay.com

CURRENT SENSE AMPLIFIER

Most designs require the regulator output voltage, measured at the CPU pins, to drop when the output current increases. The specified voltage drop corresponds to a dc output resistance (R_O), also referred to as a load line. The ADP3189 has the flexibility of adjusting R_O, independent of current limit or compensation components, and it can also support CPUs that do not require a load line.

For designs requiring a load line, the impedance gain of the CS amplifier (R_{CSA}) must be to be greater than or equal to the load line. All designs, whether they have a load line or not, should keep $R_{CSA} \geq 1$ mΩ.

The output current is measured by summing the voltage across each inductor and passing the signal through a low-pass filter. This summer filter is the CS amplifier configured with resistors $R_{PH(X)}$ (summers), and R_{CS} and C_{CS} (filter). The impedance gain of the regulator is set by the following equations, where R_L is the DCR of the output inductors:

$$R_{CSA} = \frac{R_{CS}}{R_{PH(x)}} \times R_L \quad (6)$$

$$C_{CS} = \frac{L}{R_L \times R_{CS}} \quad (7)$$

The user has the flexibility of choosing either R_{CS} or $R_{PH(X)}$. However, it is best to select R_{CS} equal to 100 kΩ, and then solve for $R_{PH(X)}$ by rearranging Equation 6. Here $R_{CSA} = R_O = 1$ mΩ since this is equal to our design loadline.

$$R_{PH(x)} = \frac{R_L}{R_{CSA}} \times R_{CS}$$

$$R_{PH(x)} = \frac{1.4\ \text{m}\Omega}{1.0\ \text{m}\Omega} \times 100\ \text{k}\Omega = 140\ \text{k}\Omega$$

Next, use Equation 7 to solve for C_{CS}.

$$C_{CS} = \frac{320\ \text{nH}}{1.4\ \text{m}\Omega \times 100\ \text{k}\Omega} = 2.28\ \text{nF}$$

It is best to have a dual location for C_{CS} in the layout so that standard values can be used in parallel to get as close to the value desired. For best accuracy, C_{CS} should be a 5% or 10% NPO capacitor. This example uses a 5% combination for C_{CS} of two 1 nF capacitors in parallel. Recalculating R_{CS} and $R_{PH(X)}$ using this capacitor combination yields 114 kΩ and 160 kΩ. The closest standard 1% value for $R_{PH(X)}$ is 158 kΩ.

INDUCTOR DCR TEMPERATURE CORRECTION

With the inductor's DCR is used as the sense element and copper wire is the source of the DCR, the user needs to compensate for temperature changes of the inductor's winding. Fortunately, copper has a well known temperature coefficient (TC) of 0.39%/°C.

If R_{CS} is designed to have an opposite and equal percentage change in resistance to that of the wire, it cancels the temperature variation of the inductor's DCR. Due to the nonlinear nature of NTC thermistors, resistors R_{CS1} and R_{CS2} are needed. See Figure 12 to linearize the NTC and produce the desired temperature tracking.

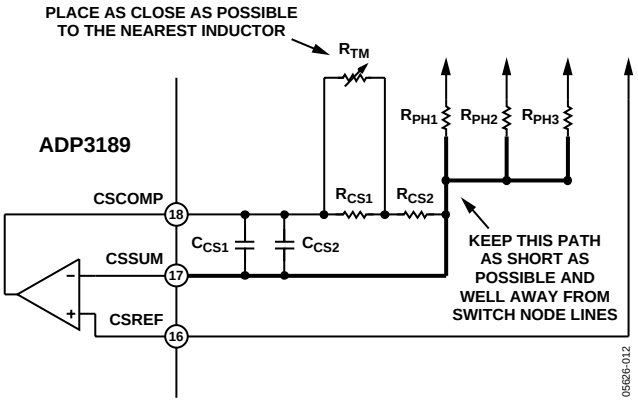

Figure 12. Temperature Compensation Circuit Values

The following procedure and expressions yield values to use for R_{CS1}, R_{CS2}, and R_{TH} (the thermistor value at 25°C) for a given R_{CS} value.

1. Select an NTC based on type and value. Since the value is unknown, use a thermistor with a value close to R_{CS}. The NTC should also have an initial tolerance of better than 5%.

2. Based on the type of NTC, find its relative resistance value at two temperatures. The temperatures that work well are 50°C and 90°C. These resistance values are called A ($R_{TH(50°C)}/R_{TH(25°C)}$) and B ($R_{TH(90°C)}/R_{TH(25°C)}$). The NTC's relative value is always 1 at 25°C.

3. Find the relative value of R_{CS} required for each of these temperatures. This is based on the percentage change needed, which in this example is initially 0.39%/°C. These are called r_1 ($1/(1 + TC \times (T_1 - 25))$) and r_2 ($1/(1 + TC \times (T_2 - 25))$), where $TC = 0.0039$ for copper. $T_1 = 50$°C and $T_2 = 90$°C are chosen. From this, calculate that $r_1 = 0.9112$ and $r_2 = 0.7978$.

1. Compute the relative values for R_{CS1}, R_{CS2}, and R_{TH} using

$$r_{CS2} = \frac{(A-B)\times r_1 \times r_2 - A\times(1-B)\times r_2 + B\times(1-A)\times r_1}{A\times(1-B)\times r_1 - B\times(1-A)\times r_2 - (A-B)} \quad (8)$$

$$r_{CS1} = \frac{(1-A)}{\frac{1}{1-r_{CS2}} - \frac{A}{r_1 - r_{CS2}}} \quad (9)$$

$$r_{TH} = \frac{1}{\frac{1}{1-r_{CS2}} - \frac{1}{r_{CS1}}} \quad (10)$$

Calculate $R_{TH} = r_{TH} \times R_{CS}$, then select the closest value of thermistor available. Also, compute a scaling factor k based on the ratio of the actual thermistor value used relative to the computed one:

$$k = \frac{R_{TH(ACTUAL)}}{R_{TH(CALCULATED)}} \quad (11)$$

2. Calculate values for R_{CS1} and R_{CS2} using Equation 12 and Equation 13:

$$R_{CS1} = R_{CS} \times k \times r_{CS1} \quad (12)$$

$$R_{CS2} = R_{CS} \times ((1-k) + (k \times r_{CS2})) \quad (13)$$

In this example, R_{CS} was calculated to be 114 kΩ. Look for an available 100 kΩ thermistor, 0603 size. One such thermistor is the Vishay NTHS0603N01N1003JR NTC thermistor with A = 0.3602 and B = 0.09174. From these values, compute r_{CS1} = 0.3795, r_{CS2} = 0.7195, and r_{TH} = 1.075.

Solving for R_{TH} yields 122.55 kΩ, so 100 kΩ is chosen, making k = 0.816. Next find R_{CS1} and R_{CS2} to be 35.3 kΩ and 87.9 kΩ. Finally, choose the closest 1% resistor values, which yields a choice of 35.7 kΩ and 88.7 kΩ.

LOAD LINE SETTING

For load line values greater than 1 mΩ, R_{CSA} can be set equal to R_O, and the LLSET pin can be directly connected to the CSCOMP pin. When the load line value needs to be less than 1 mΩ, two additional resistors are required. Figure 13 shows the placement of these resistors.

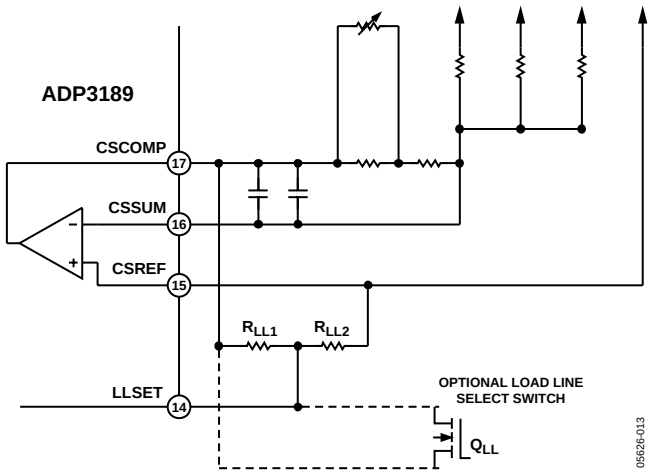

Figure 13. Load Line Setting Resistors

The two resistors R_{LL1} and R_{LL2} set up a divider between the CSCOMP pin and CSREF pin. This resistor divider is input into the LLSET pin to set the load line slope R_O of the VR according to the following equation:

$$R_O = \frac{R_{LL2}}{R_{LL1} + R_{LL2}} \times R_{CSA} \quad (14)$$

For best results, start with a 1% resistor of 20.0 kΩ for R_{LL2}. Then, solve for the required value of R_{LL1} by rearranging Equation 14 as follows:

$$R_O = \frac{R_{LL2}}{R_{LL1} + R_{LL2}} \times R_{CSA}$$

Another useful feature for some VR applications is the ability to select different load lines. Figure 13 shows an optional MOSFET switch that allows this. Here, design for $R_{CSA} = R_{O(MAX)}$ (selected with Q_{LL} on) and then use Equation 14 to set $R_O = R_{O(MIN)}$ (selected with Q_{LL} off).

For this design, $R_{CSA} = R_O$ = 1 mΩ, so connect LLSET directly to CSCOMP, and the resistors R_{LL1} and R_{LL2} are not needed.

OUTPUT OFFSET

The Intel specification requires that at no load the nominal output voltage of the regulator is offset to a value lower than the nominal voltage corresponding to the VID code. The offset is set by a constant current source flowing out of the FB pin (I_{FB}) and flowing through R_B. The value of R_B can be found using Equation 15:

$$R_B = \frac{V_{VID} - V_{ONL}}{I_{FB}}$$

$$R_B = \frac{1.3\text{ V} - 1.285\text{ V}}{15\ \mu\text{A}} = 1.00\ \text{k}\Omega \quad (15)$$

The closest standard 1% resistor value is 1.00 kΩ.

C_{OUT} SELECTION

The required output decoupling for the regulator is typically recommended by Intel for various processors and platforms. Use some simple design guidelines to determine the requirements. These guidelines are based on having both bulk capacitors and ceramic capacitors in the system.

First, select the total amount of ceramic capacitance. This is based on the number and type of capacitor to be used. The best location for ceramic capacitors is inside the socket, with 12 to 18 of size, 1206 being the physical limit. Other capacitors can be placed along the outer edge of the socket as well.

To aid in determining the minimum amount of ceramic capacitance required, start with a worst-case load step occurring right after a switching cycle has stopped. The ceramic capacitance then delivers the charge to the load while the load is ramping up and until the VR has responded with the next switching cycle.

The following equation gives the designer a rough approximation for determining the minimum ceramic capacitance needed. Due to the complexity of the PCB parasitics and bulk capacitors, the actual amount of ceramic capacitance required may vary.

$$C_{Z(MIN)} \geq \frac{1}{R_O} \times \left[\frac{1}{f_{SW}} \times \left(\frac{1}{n} - D \right) - \frac{\Delta I_O}{2\ S_R} \right] \quad (16)$$

The typical ceramic capacitors used are made up of multiple 10 µF or 22 µF capacitors. For this example, Equation 16 yields 180.8 µF, so eighteen 10 uF ceramics will suffice.

Next, there is an upper limit imposed on the total amount of bulk capacitance (C_X) when the user considers the VID on-the-fly voltage stepping of the output (voltage step V_V in time t_V with error of V_{ERR}).

A lower limit is based on meeting the capacitance for load release for a given maximum load step ΔI_O and a maximum allowable overshoot. The total amount of load release voltage is given as $\Delta V_O = \Delta I_O \times R_O + \Delta V_{rl}$, where ΔV_{rl} is the maximum allowable overshoot voltage.

$$C_{x(MIN)} \geq \left(\frac{L \times \Delta I_O}{n \times \left(R_O + \frac{\Delta V_{rl}}{\Delta I_O} \right) \times V_{VID}} - C_z \right) \quad (17)$$

$$C_{x(MAX)} \leq \quad (18)$$

$$\frac{L}{nK^2 R_O^2} \times \frac{V_V}{V_{VID}} \times \left(\sqrt{1 + \left(t_v \frac{V_{VID}}{V_V} \times \frac{nKR_O}{L} \right)^2} - 1 \right) - C_z$$

where $K = -1n\left(\frac{V_{ERR}}{V_V} \right)$

To meet the conditions of these expressions and transient response, the ESR of the bulk capacitor bank (R_X) should be less than two times the droop resistance (R_O). If the $C_{X(MIN)}$ is larger than $C_{X(MAX)}$, the system cannot meet the VID on-the-fly specification and can require the use of a smaller inductor or more phases (and may have to increase the switching frequency to keep the output ripple the same).

This example uses eighteen 10 µF 1206 MLC capacitors (C_Z = 180 F). The VID on-the-fly step change is 450 mV in 230 µs with a setting error of 2.5 mV. The maximum allowable load release overshoot for this example is 50 mV, therefore solving for the bulk capacitance yields

$$C_{x(MIN)} \leq \left(\frac{320\text{ nH} \times 100\text{ A}}{4 \times \left(1.0\ \text{m}\Omega + \frac{50\text{ mV}}{100\text{ A}} \right) \times 1.3\text{ V}} - 180\ \mu\text{F} \right) = 3.92\text{ mF}$$

$$C_{x(MAX)} \leq \frac{320\text{ nH} \times 450\text{ mV}}{4 \times 5.2^2 \times (1.0\ \text{m}\Omega)^2 \times 1.3\text{ V}} \times$$

$$\left(\sqrt{1 + \left(\frac{230\ \mu\text{s} \times 1.3\ V \times 4 \times 5.2 \times 1.0\ \text{m}\Omega}{450\text{ mV} \times 320\text{ nH}} \right)^2} - 1 \right) - 180\ \mu\text{F}$$

$$= 43.0\text{ mF}$$

where $K = 5.2$

Using ten 560 µF Al-Poly capacitors with a typical ESR of 6 mΩ each yields C_X = 5.6 mF with an R_X = 0.6 mΩ.

One last check should be made to ensure that the ESL of the bulk capacitors (L_X) is low enough to limit the high frequency ringing during a load change.

This is tested using

$$L_x \le C_z \times R_O{}^2 \times Q^2$$
$$L_x \le 180\,\mu\text{F} \times (1\,\text{m}\Omega)^2 \times \frac{4}{3} = 240\,\text{pH} \quad (19)$$

where Q^2 is limited to $^4/_3$ to ensure a critically damped system.

In this example, L_X is approximately 240 pH for the ten A1-Polys capacitors, which satisfies this limitation. If the L_X of the chosen bulk capacitor bank is too large, the number of ceramic capacitors may need to be increased, or lower ESL bulks used if there is excessive undershoot during a load transient.

For this multimode control technique, all ceramic designs can be used providing the conditions of Equation 16, Equation 17, Equation 18, and Equation 19 are satisfied.

POWER MOSFETS

For this example, the N-channel power MOSFETs have been selected for one high-side switch and two low-side switches per phase. The main selection parameters for the power MOSFETs are $V_{GS(TH)}$, Q_G, C_{ISS}, C_{RSS}, and $R_{DS(ON)}$. The minimum gate drive voltage (the supply voltage to the ADP3120) dictates whether standard threshold or logic-level threshold MOSFETs must be used. With V_{GATE} ~10 V, logic-level threshold MOSFETs ($V_{GS(TH)}$ < 2.5 V) are recommended.

The maximum output current (I_O) determines the $R_{DS(ON)}$ requirement for the low-side (synchronous) MOSFETs. With the ADP3189, currents are balanced between phases, thus the current in each low-side MOSFET is the output current divided by the total number of MOSFETs (n_{SF}). With conduction losses being dominant, the following expression shows the total power being dissipated in each synchronous MOSFET in terms of the ripple current per phase (I_R) and average total output current (I_O):

$$P_{SF} = (1-D) \times \left[\left(\frac{I_O}{n_{SF}} \right)^2 + \frac{1}{12} \times \left(\frac{n\,I_R}{n_{SF}} \right)^2 \right] \times R_{DS(SF)} \quad (20)$$

Knowing the maximum output current being designed for and the maximum allowed power dissipation, the user can find the required $R_{DS(ON)}$ for the MOSFET. For D-PAK MOSFETs up to an ambient temperature of 50°C, a safe limit for P_{SF} is 1 W to 1.5 W at 120°C junction temperature. Thus, for this example (119 A maximum), $R_{DS(SF)}$ (per MOSFET) < 7.5 mΩ. This $R_{DS(SF)}$ is also at a junction temperature of about 120°C, so be certain to account for this when making this selection. This example uses two lower-side MOSFETs at 4.8 mΩ, each at 120°C.

Another important factor for the synchronous MOSFET is the input capacitance and feedback capacitance. The ratio of the feedback to input needs to be small (less than 10% is recommended) to prevent accidental turn-on of the synchronous MOSFETs when the switch node goes high.

Also, the time to switch the synchronous MOSFETs off should not exceed the nonoverlap dead time of the MOSFET driver (40 ns typical for the ADP3120). The output impedance of the driver is approximately 2 Ω, and the typical MOSFET input gate resistances are about 1 Ω to 2 Ω, so a total gate capacitance of less than 6000 pF should be adhered to. Since there are two MOSFETs in parallel, the input capacitance for each synchronous MOSFET should be limited to 3000 pF.

The high-side (main) MOSFET has to be able to handle two main power dissipation components: conduction and switching losses. The switching loss is related to the amount of time it takes for the main MOSFET to turn on and off, and to the current and voltage that are being switched. Basing the switching speed on the rise and fall time of the gate driver impedance and MOSFET input capacitance, the following expression provides an approximate value for the switching loss per main MOSFET, where n_{MF} is the total number of main MOSFETs:

$$P_{S(MF)} = 2 \times f_{SW} \times \frac{V_{CC} \times I_O}{n_{MF}} \times R_G \times \frac{n_{MF}}{n} \times C_{ISS} \quad (21)$$

where R_G is the total gate resistance (2 Ω for the ADP3120 and about 1 Ω for typical high speed switching MOSFETs, making R_G = 3 Ω), and C_{ISS} is the input capacitance of the main MOSFET. Adding more main MOSFETs (n_{MF}) does not help the switching loss per MOSFET, since the additional gate capacitance slows switching. Use lower gate capacitance devices to reduce switching loss.

The conduction loss of the main MOSFET is given by the following, where $R_{DS(MF)}$ is the on resistance of the MOSFET:

$$P_{C(MF)} = D \times \left[\left(\frac{I_O}{n_{MF}} \right)^2 + \frac{1}{12} \times \left(\frac{n \times I_R}{n_{MF}} \right)^2 \right] \times R_{DS(MF)} \quad (22)$$

Typically, for main MOSFETs, the highest speed (low C_{ISS}) device is preferred, but these usually have higher on resistance. Select a device that meets the total power dissipation (about 1.5 W for a single D-PAK) when combining the switching and conduction losses.

For this example, an NTD40N03L was selected as the main MOSFET (eight total; n_{MF} = 8), with C_{ISS} = 584 pF (max) and $R_{DS(MF)}$ = 19 mΩ (max at T_J = 120°C), and an NTD110N02L was selected as the synchronous MOSFET (eight total; n_{SF} = 8), with C_{ISS} = 2710 pF (max) and $R_{DS(SF)}$ = 4.8 mΩ (max at T_J = 120°C). The synchronous MOSFET C_{ISS} is less than 3000 pF, satisfying this requirement. Solving for the power dissipation per MOSFET at IO = 119 A and IR = 11 A yields 958 mW for each synchronous MOSFET and 872 mW for each main MOSFET. The guideline is to limit the MOSFET power dissipation to 1 W. The values calculated in Equation 21 and Equation 22 comply with this guideline.

Finally, consider the power dissipation in the driver for each phase. This is best expressed as Q_G for the MOSFETs and is given by the following equation, where Q_{GMF} is the total gate charge for each main MOSFET and Q_{GSF} is the total gate charge for each synchronous MOSFET.

$$P_{DRV} = \left[\frac{f_{SW}}{2 \times n} \times \left(n_{MF} \times Q_{GMF} + n_{SF} \times Q_{GSF}\right) + I_{CC}\right] \times V_{CC} \quad (23)$$

Also shown is the driver's standby dissipation factor ($I_{CC} \times V_{CC}$). For the ADP3120, the maximum dissipation should be less than 400 mW. In this example, with I_{CC} = 7 mA, Q_{GMF} = 5.8 nC, and Q_{GSF} = 48 nC, one finds 297 mW in each driver, which is below the 400 mW dissipation limit. See the ADP3120 data sheet for more details.

RAMP RESISTOR SELECTION

The ramp resistor (R_R) is used for setting the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of thermal balance, stability, and transient response. The following expression is used for determining the optimum value:

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS} \times C_R} \quad (24)$$

$$R_R = \frac{0.2 \times 320\ \text{nH}}{3 \times 5 \times 2.4\ \text{m}\Omega \times 5\ \text{pF}} = 356\ \text{k}\Omega$$

where

A_R is the internal ramp amplifier gain.
A_D is the current balancing amplifier gain.
R_{DS} is the total low-side MOSFET on resistance.
C_R is the internal ramp capacitor value.

The internal ramp voltage magnitude can be calculated by using

$$V_R = \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} \quad (25)$$

$$V_R = \frac{0.2 \times (1 - 0.108) \times 1.3\ \text{V}}{357\ \text{k}\Omega \times 5\ \text{pF} \times 330\ \text{kHz}} = 394\ \text{mV}$$

The size of the internal ramp can be made larger or smaller. If it is made larger, stability and noise rejection improves, but transient degrades. Likewise, if the ramp is made smaller, transient response improves at the sacrifice of noise rejection and stability.

The factor of 3 in the denominator of Equation 24 sets a ramp size that gives an optimal balance for good stability, transient response, and thermal balance.

COMP PIN RAMP

A ramp signal on the COMP pin is due to the droop voltage and output voltage ramps. This ramp amplitude adds to the internal ramp to produce the following overall ramp signal at the PWM input:

$$V_{RT} = \frac{V_R}{\left(1 - \frac{2 \times (1 - n \times D)}{n \times f_{SW} \times C_X \times R_O}\right)} \quad (26)$$

In this example, the overall ramp signal is 0.46 V. However, if the ramp size is smaller than 0.5 V, increase the ramp size to be at least 0.5 V by decreasing the ramp resistor for noise immunity. As there is only 0.46 V initially, a ramp resistor value of 332 kΩ is chosen for this example, yielding an overall ramp of 0.51 V.

CURRENT LIMIT SETPOINT

To select the current limit setpoint, first find the resistor value for R_{LIM}. The current limit threshold for the ADP3189 is set with a 1.7 V source (V_{LIM}) across R_{LIM} with a gain of 10 mV/μA (A_{LIM}). R_{LIM} can be found using

$$R_{LIM} = \frac{A_{LIM} \times V_{LIM}}{I_{LIM} \times R_{CSA}} \quad (27)$$

For values of R_{LIM} greater than 500 kΩ, the current limit may be lower than expected, so some adjustment of R_{LIM} is needed. Here, I_{LIM} is the peak average current limit for the supply output. In this example, choosing a peak current limit of 170 A for I_{LIM}, results in R_{LIM} = 100 kΩ, and 100 kΩ is chosen as the nearest 1% value.

The per-phase initial duty cycle limit and peak current during a load step are determined by

$$D_{MAX} = D \times \frac{V_{COMP(MAX)} - V_{BIAS}}{V_{RT}} \quad (28)$$

$$I_{PHMAX} \cong \frac{D_{MAX}}{f_{SW}} \times \frac{(V_{IN} - V_{VID})}{L} \quad (29)$$

For the ADP3189, the maximum COMP voltage ($V_{COMP(MAX)}$) is 4.0 V and the COMP pin bias voltage (V_{BIAS}) is 1.1 V. In this example, the maximum duty cycle is 0.61 and the peak current is 62 A.

The limit of the peak per-phase current described earlier during the secondary current limit is determined by

$$I_{PHLIM} \cong \frac{V_{COMP(CLAMPED)} - V_{BIAS}}{A_D \times R_{DS(MAX)}} \quad (30)$$

For the ADP3189, the current balancing amplifier gain (A_D) is 5, and the clamped COMP pin voltage is 2 V. Using an $R_{DS(MAX)}$ of 2.8 mΩ (low-side on resistance at 150°C) results in a per-phase peak current limit of 64 A. This current level can be reached only with an absolute short at the output, and the current limit latch-off function shuts down the regulator before overheating can occur.

FEEDBACK LOOP COMPENSATION DESIGN

Optimized compensation of the ADP3189 allows the best possible response of the regulator's output to a load change. The basis for determining the optimum compensation is to make the regulator and output decoupling appear as an output impedance that is entirely resistive over the widest possible frequency range, including dc, and equal to the droop resistance (R_O). With the resistive output impedance, the output voltage droops in proportion to the load current at any load current slew rate. This ensures the optimal positioning and allows the minimization of the output decoupling.

With the multimode feedback structure of the ADP3189, the feedback compensation must be set to make the converter's output impedance, working in parallel with the output decoupling, to meet this goal. Several poles and zeros created by the output inductor and decoupling capacitors (output filter) need to be compensated for.

A type-three compensator on the voltage feedback is adequate for proper compensation of the output filter. Equation 31 to Equation 35 are intended to yield an optimal starting point for the design; some adjustments may be necessary to account for PCB and component parasitic effects (see the Tuning the ADP3189 section).

First, compute the time constants for all the poles and zeros in the system, using Equation 31 to Equation 35 on the next page.

The first step is to compute the time constants for all of the poles and zeros in the system:

$$R_E = n \times R_O + A_D \times R_{DS} + \frac{R_L \times V_{RT}}{V_{VID}} + \frac{2 \times L \times (1 - n \times D) \times V_{RT}}{n \times C_X \times R_O \times V_{VID}}$$

$$R_E = 4 \times 1\ \text{m}\Omega + 5 \times 2.4\ \text{m}\Omega + \frac{1.4\ \text{m}\Omega \times 0.51\ \text{V}}{1.3\ \text{V}} + \frac{2 \times 320\ \text{nH} \times (1 - 0.432) \times 0.51\ \text{V}}{4 \times 5.6\ \text{mF} \times 1\ \text{m}\Omega \times 1.3\ \text{V}} = 22.9\ \text{m}\Omega \quad (31)$$

$$T_A = C_X \times (R_O - R') + \frac{L_X}{R_O} \times \frac{R_O - R'}{R_X} = 5.6\ \text{mF} \times (1\ \text{m}\Omega - 0.5\ \text{m}\Omega) + \frac{240\ \text{pH}}{1\ \text{m}\Omega} \times \frac{1\ \text{m}\Omega - 0.5\ \text{m}\Omega}{0.6\ \text{m}\Omega} = 3.00\ \mu\text{s} \quad (32)$$

$$T_B = (R_X + R' - R_O) \times C_X = (0.6\ \text{m}\Omega + 0.5\ \text{m}\Omega - 1\ \text{m}\Omega) \times 5.6\ \text{mF} = 560\ \text{ns} \quad (33)$$

$$T_C = \frac{V_{RT} \times \left(L - \frac{A_D \times R_{DS}}{2 \times f_{SW}} \right)}{V_{VID} \times R_E} = \frac{0.51\ \text{V} \times \left(320\ \text{nH} - \frac{5 \times 2.4\ \text{m}\Omega}{2 \times 330\ \text{kHz}} \right)}{1.3\ \text{V} \times 22.9\ \text{m}\Omega} = 5.17\ \mu\text{s} \quad (34)$$

$$T_D = \frac{C_X \times C_Z \times R_O^2}{C_X \times (R_O - R') + C_Z \times R_O} = \frac{5.6\ \text{mF} \times 180\ \mu\text{F} \times (1\ \text{m}\Omega)^2}{5.6\ \text{mF} \times (1\ \text{m}\Omega - 0.5\ \text{m}\Omega) + 180\ \mu\text{F} \times 1\ \text{m}\Omega} = 338\ \text{ns} \quad (35)$$

where, for the ADP3189, R' is the PCB resistance from the bulk capacitors to the ceramics and where R_{DS} is the total low-side MOSFET on resistance per phase. In this example, A_D is 5, V_{RT} equals 0.51 V, R' is approximately 0.5 mΩ (assuming a 4-layer, 1 ounce motherboard), and L_X is 240 pH for the ten Al-Poly capacitors.

The compensation values can then be solved using

$$C_A = \frac{n \times R_O \times T_A}{R_E \times R_B} = \frac{4 \times 1\ \text{m}\Omega \times 3.00\ \mu\text{s}}{22.9\ \text{m}\Omega \times 1.00\ \text{k}\Omega} = 524\ \text{pF} \quad (36)$$

$$R_A = \frac{T_C}{C_A} = \frac{5.17\ \mu\text{s}}{524\ \text{pF}} = 9.87\ \text{k}\Omega \quad (37)$$

$$C_B = \frac{T_B}{R_B} = \frac{560\ \text{ns}}{1.00\ \text{k}\Omega} = 560\ \text{pF} \quad (38)$$

$$C_{FB} = \frac{T_D}{R_A} = \frac{338\ \text{ns}}{9.87\ \text{k}\Omega} = 34.2\ \text{pF} \quad (39)$$

These are the starting values prior to tuning the design to account for layout and other parasitic effects (see the Tuning the ADP3189 section). The final values selected after tuning are

C_A = 560 pF

R_A = 10.0 kΩ

C_B = 560 pF

C_{FB} = 27 pF

Figure 14 and Figure 15 show the typical transient response using these compensation values.

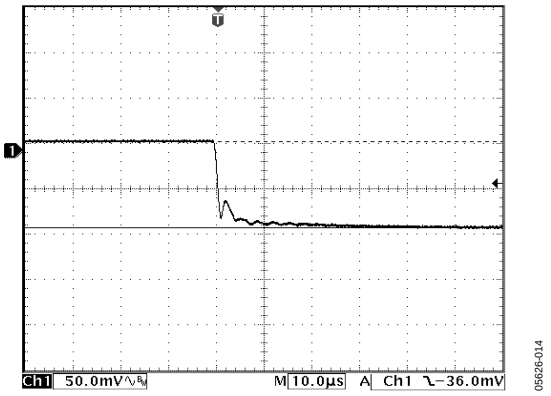

Figure 14. Typical Transient Response for Design Example Load Step

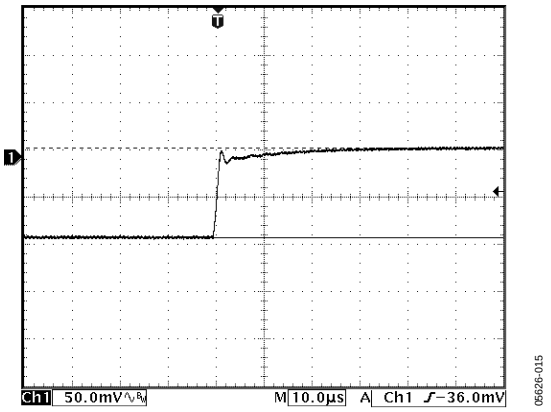

Figure 15. Typical Transient Response for Design Example Load Release

C_{IN} SELECTION AND INPUT CURRENT di/dt REDUCTION

In continuous inductor current mode, the source current of the high-side MOSFET is approximately a square wave with a duty ratio equal to n × V_{OUT}/V_{IN} and an amplitude of one-nth the maximum output current. To prevent large voltage transients, a low ESR input capacitor, sized for the maximum rms current, must be used. The maximum rms capacitor current is given by

$$I_{CRMS} = D \times I_O \times \sqrt{\frac{1}{\mathrm{N} \times \mathrm{D}} - 1} \tag{40}$$

$$I_{CRMS} = 0.108 \times 119\,\mathrm{A} \times \sqrt{\frac{1}{4 \times 0.108} - 1} = 14.7\,\mathrm{A}$$

The capacitor manufacturer's ripple current ratings are often based on only 2,000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may be placed in parallel to meet size or height requirements in the design. In this example, the input capacitor bank is formed by two 2,700 µF, 16 V aluminum electrolytic capacitors, and eight 4.7 µF ceramic capacitors.

To reduce the input current di/dt to a level below the recommended maximum of 0.1 A/µs, an additional small inductor (L > 370 nH at 18 A) should be inserted between the converter and the supply bus. This inductor also acts as a filter between the converter and the primary power source.

THERMAL MONITOR DESIGN

A thermistor is used on the TTSENSE input of the ADP3189 for monitoring the temperature of the VR. A constant current of 120 µA is sourced out of this pin and run through a thermistor network such as that shown in Figure 16.

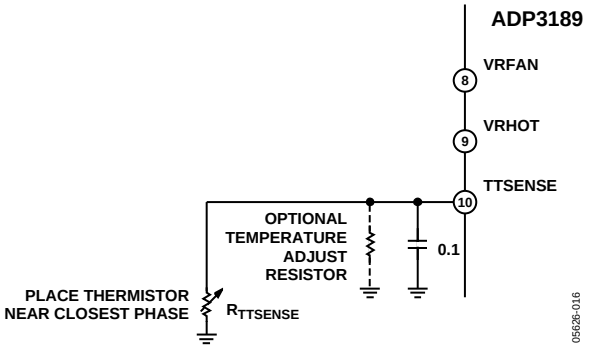

Figure 16. VR Thermal Monitor Circuit

A voltage is generated from this current through the thermistor and sensed inside the IC. When the voltage reaches 1.11 V, the VRFAN output gets set. When the voltage reaches 0.81 V, the VRHOT gets set. This corresponds to $R_{TTSENSE}$ values of 9.25 kΩ for VRFAN and 6.75 kΩ.

These values correspond to a thermistor temperature of ~100°C and ~110°C when using the same type of 100 kΩ NTC thermistor used in the current sense amplifier.

An additional fixed resistor in parallel with the thermistor provides tuning the trip point temperatures to match the hottest temperature in the VR, when the thermistor itself is directly sensing a proportionately lower temperature. Setting this resistor value is best accomplished with a variable resistor during thermal validation, and then fixing this value for the final design.

Additionally, a 0.1 µF should be used for filtering noise.

TUNING THE ADP3189

1. Build a circuit based on the compensation values computed from the design spreadsheet.
2. Hook up the dc load to circuit, turn it on, and verify its operation. Also, check for jitter at no load and full load.

DC Loadline Setting

3. Measure the output voltage at no load (V_{NL}). Verify that it is within tolerance.
4. Measure the output voltage at full load cold (V_{FLCOLD}). Let the board sit for ~10 minutes at full load, and then measure the output (V_{FLHOT}). If there is a change of more than a few millivolts, adjust R_{CS1} and R_{CS2} using Equation 41 and Equation 43.

$$R_{CS2(NEW)} = R_{CS2(OLD)} \times \frac{V_{NL} - V_{FLCOLD}}{V_{NL} - V_{FLHOT}} \quad (41)$$

5. Repeat Step 4 until the cold and hot voltage measurements remain the same.
6. Measure the output voltage from no load to full load using 5 A steps. Compute the loadline slope for each change, and then average to get overall loadline slope (R_{OMEAS}).
7. If R_{OMEAS} is off from R_O by more than 0.05 mΩ, use the following to adjust the R_{PH} values:

$$R_{PH(NEW)} = R_{PH(OLD)} \times \frac{R_{OMEAS}}{R_O} \quad (42)$$

8. Repeat Step 6 and Step 7 to check the loadline, and repeat adjustments if necessary.
9. Once dc loadline adjustment is complete, do not change R_{PH}, R_{CS1}, R_{CS2}, or R_{TH} for the remainder of the procedure.
10. Measure the output ripple at no load and full load with a scope, and make sure it is within specifications.

$$R_{CS1(NEW)} = \frac{1}{\frac{R_{CS1(OLD)} + R_{TH(25°C)}}{R_{CS1(OLD)} \times R_{TH(25°C)} + \left(R_{CS1(OLD)} - R_{CS2(NEW)}\right) \times \left(R_{CS1(OLD)} - R_{TH(25°C)}\right)} - \frac{1}{R_{TH(25°C)}}} \quad (43)$$

AC Loadline Setting

11. Remove the dc load from the circuit and hook up the dynamic load.

12. Hook up the scope to the output voltage and set it to dc coupling with the time scale at 100 µs/div.

13. Set the dynamic load for a transient step of about 40 A at 1 kHz with 50% duty cycle.

14. Measure the output waveform (use dc offset on scope to see the waveform). Try to use a vertical scale of 100 mV/div or finer. This waveform should look similar to Figure 17.

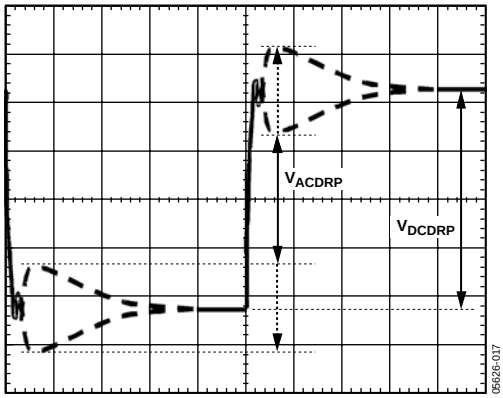

Figure 17. AC Loadline Waveform

15. Use the horizontal cursors to measure V_{ACDRP} and V_{DCDRP} as shown. Do not measure the undershoot or overshoot that happens immediately after this step.

16. If V_{ACDRP} and V_{DCDRP} are different by more than a few millivolts, use Equation 44 to adjust C_{CS}. You may need to parallel different values to get the right one since there are limited standard capacitor values available. (It is a good idea to have locations for two capacitors in the layout for this.)

$$C_{CS(NEW)} = C_{CS(OLD)} \times \frac{V_{ACDRP}}{V_{DCDRP}} \quad (44)$$

17. Repeat Step 11 to Step 13 and repeat the adjustments if necessary. Once complete, do not change C_{CS} for the remainder of the procedure.

    Set the dynamic load step to maximum step size (do not use a step size larger than needed) and verify that the output waveform is square, which means that V_{ACDRP} and V_{DCDRP} are equal.

Initial Transient Setting

18. With the dynamic load still set at the maximum step size, expand the scope time scale to see 2 µs/div to 5 µs/div. The waveform can have two overshoots and one minor undershoot (see Figure 18). Here, V_{DROOP} is the final desired value.

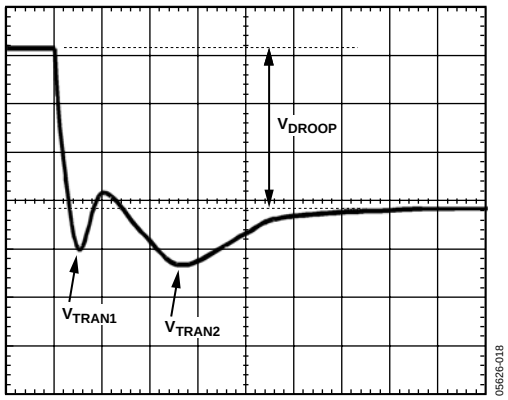

Figure 18. Transient Setting Waveform

19. If both overshoots are larger than desired, try making the adjustments described later in this step. If these adjustments do not change the response, you are limited by the output decoupling. Check the output response each time you make a change, and check the switching nodes to make ensure that the response is still stable.

    - Make the ramp resistor larger by 25% (R_{RAMP}).
    - For V_{TRAN1}, increase C_B or increase the switching frequency.
    - For V_{TRAN2}, increase R_A and decrease C_A by 25%.

20. For load release (see Figure 19), if $V_{TRANREL}$ is larger than the allowed overshoot, there is not enough output capacitance. Either more capacitance is needed, or the inductor values need to be made smaller. (When changing inductors, start the design again using a spreadsheet and this tuning procedure.)

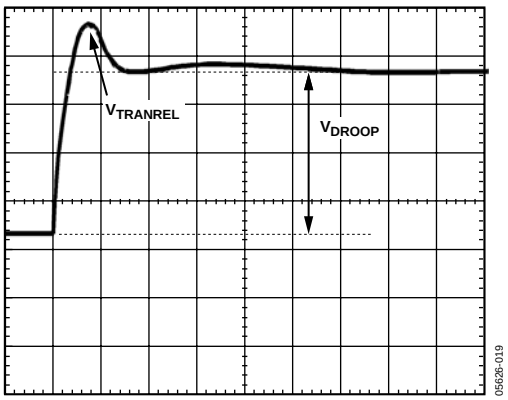

Figure 19. Transient Setting Waveform

Since the ADP3189 turns off all of the phases (switches inductors to ground), there is no ripple voltage present during load release. Therefore, the user does not have to add headroom for ripple, allowing load release VTRANREL to be larger than VTRAN1, by the amount of ripple, and still meet specifications.

If V_{TRAN1} and $V_{TRANREL}$ are less than the desired final droop, this implies that capacitors can be removed. When removing capacitors, check the output ripple voltage as well to make sure it is still within specifications.

LAYOUT AND COMPONENT PLACEMENT

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

General Recommendations

For good results, a PCB with at least four layers is recommended. This should allow the needed versatility for control circuitry interconnections with optimal placement, power planes for ground, input and output power, and wide interconnection traces in the remainder of the power delivery current paths. Keep in mind that each square unit of 1 ounce copper trace has a resistance of ~0.53 mΩ at room temperature.

Whenever high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths, so the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.

If critical signal lines (including the output voltage sense lines of the ADP3189) must cross through power circuitry, it is best if a signal ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.

An analog ground plane should be used around and under the ADP3189 as a reference for the components associated with the controller. This plane should be tied to the nearest output decoupling capacitor ground and should not be tied to any other power circuitry to prevent power currents from flowing in it.

The components around the ADP3189 should be located close to the controller with short traces. The most important traces to keep short and away from other traces are the FB pin and CSSUM pin. The output capacitors should be connected as close as possible to the load (or connector), for example, a microprocessor core, that receives the power. If the load is distributed, the capacitors should also be distributed and generally be in proportion to where the load tends to be more dynamic.

Avoid crossing any signal lines over the switching power path loop, described in the Power Circuitry Recommendations section.

Power Circuitry Recommendations

The switching power path should be routed on the PCB to encompass the shortest-possible length in order to minimize radiated switching noise energy (that is, EMI) and conduction losses in the board. Failure to take proper precautions often results in EMI problems for the entire PC system and noise-related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors and the power MOSFETs, including all interconnecting PCB traces and planes. Using short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high energy ringing, and it accommodates the high current demand with minimal voltage loss.

Whenever a power dissipating component, for example, a power MOSFET, is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are improved current rating through the vias and improved thermal performance from vias extended to the opposite side of the PCB, where a plane can more readily transfer the heat to the air. Make a mirror image of any pad being used to heatsink the MOSFETs on the opposite side of the PCB to achieve the best thermal dissipation to the air around the board. To further improve thermal performance, use the largest possible pad area.

The output power path should also be routed to encompass a short distance. The output power path is formed by the current path through the inductor, the output capacitors, and the load.

For best EMI containment, a solid power ground plane should be used as one of the inner layers extending fully under all the power components.

Signal Circuitry Recommendations

The output voltage is sensed and regulated between the FB pin and the FBRTN pin, which connect to the signal ground at the load. To avoid differential mode noise pickup in the sensed signal, the loop area should be small. Thus, the FB trace and FBRTN trace should be routed adjacent to each other on top of the power ground plane back to the controller.

The feedback traces from the switch nodes should be connected as close as possible to the inductor. The CSREF signal should be connected to the output voltage at the nearest inductor to the controller.

OUTLINE DIMENSIONS

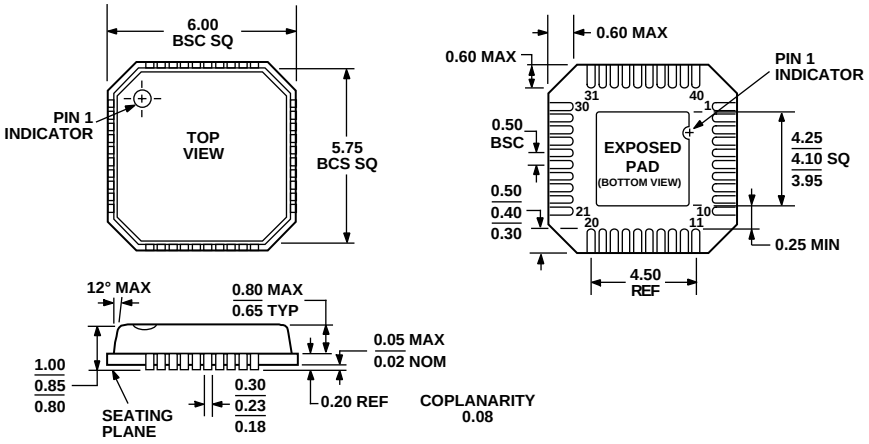

Figure 20. 40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
6 mm × 6 mm Body, Very Thin Quad
(CP-40)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADP3189JCPZ-RL[1]	0°C to 85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-40	2500

[1] Z = Pb-free part.

NOTES

D05626–0–7/05(0)