CYM1422

128K x 8 Static RAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 35 ns**
- **Low active power**
  - **1.1W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.65 in.**
- **Small PCB footprint**
  - **0.8 sq. in.**

Functional Description

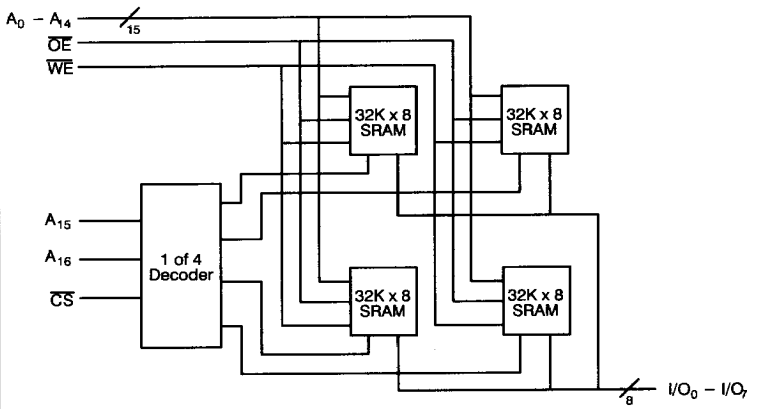
The CYM1422 is a high-performance 1-megabit static RAM module organized as 128K words by 8 bits. The module is constructed using four 32K x 8 static RAMs in SOICs mounted onto a single-sided multilayer epoxy laminate board with pins. A decoder is used to interpret the higher-order addresses (A_{15} and A_{16}) and to select one of the four RAMs.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{16}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



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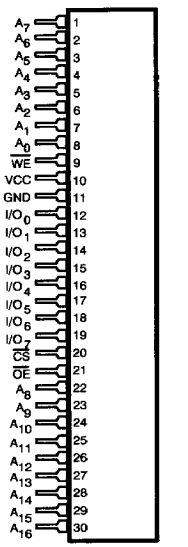
Pin Configuration

SIP
Component Side



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Selection Guide

	1422-35	1422-45	1422-55
Maximum Access Time (ns)	35	45	55
Maximum Operating Current (mA)	200	200	200
Maximum Standby Current (mA)	140	140	140

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... −10°C to +90°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to + 7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	1422 Min.	1422 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−15	+15	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−15	+15	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		200	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH} Min. Duty Cycle = 100%		140	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		80	mA

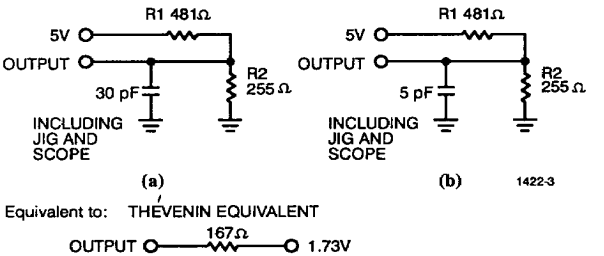
Capacitance[2]

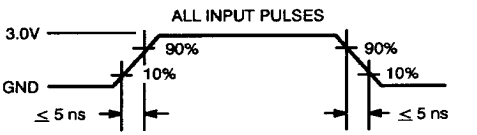
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	40	pF
C_{OUT}	Output Capacitance		35	pF

Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms





Switching Characteristics Over the Operating Range[3]

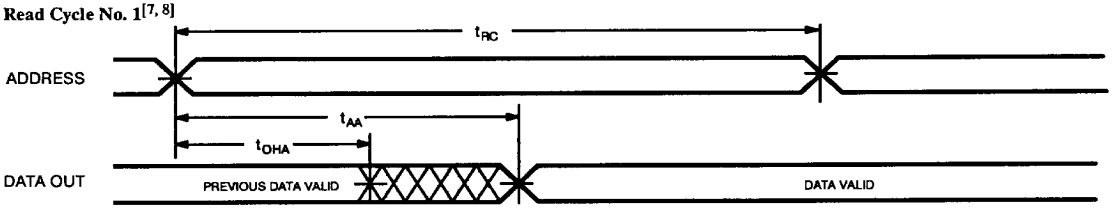
Parameters	Description	1422–35		1422–45		1422–55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		20		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		20		20		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		20		20		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		35		45		55	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	30		40		45		ns
t_{AW}	Address Set-Up to Write End	30		40		45		ns
t_{HA}	Address Hold from Write End	5		5		5		ns
t_{SA}	Address Set-Up to Write Start	5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	25		35		35		ns
t_{SD}	Data Set-Up to Write End	20		20		20		ns
t_{HD}	Data Hold from Write End	3		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[4]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4, 5]	0	20	0	25	0	25	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
5. t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
9. Data I/O will be high impedance if $\overline{OE}$ = V_{IH}.
10. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
11. If $\overline{CS}$ goes HIGH siumultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms[9]

Read Cycle No. 1[7, 8]



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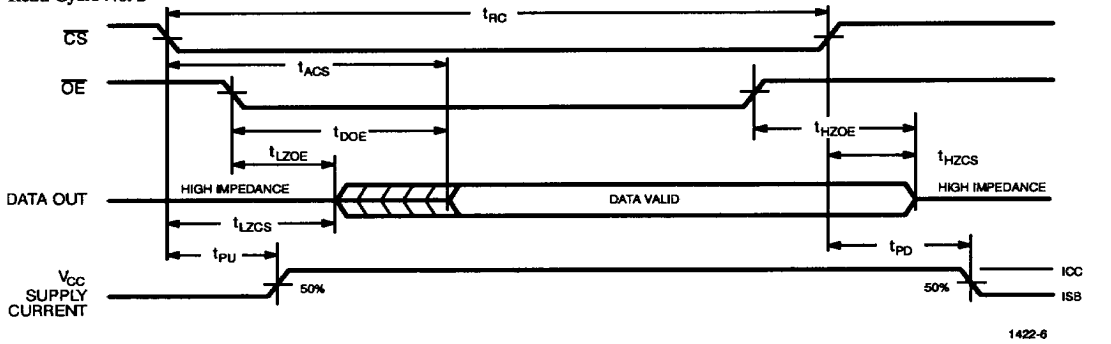
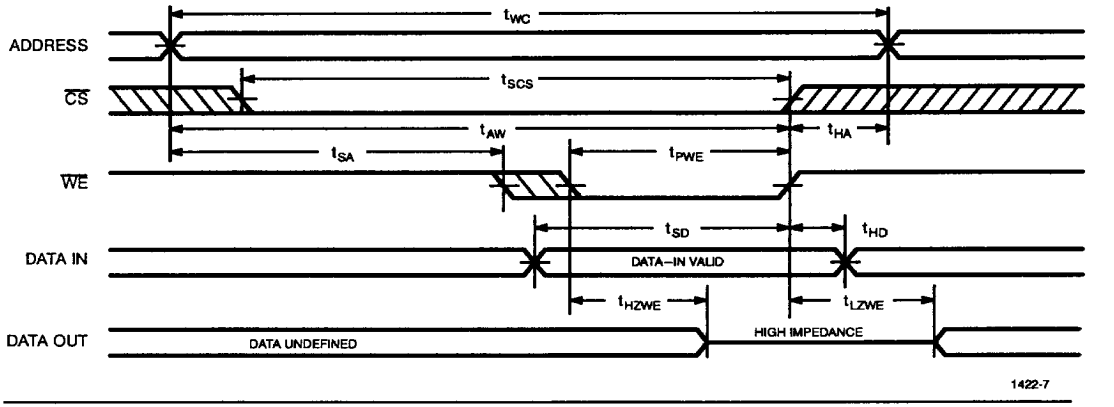
Switching Waveforms (continued)

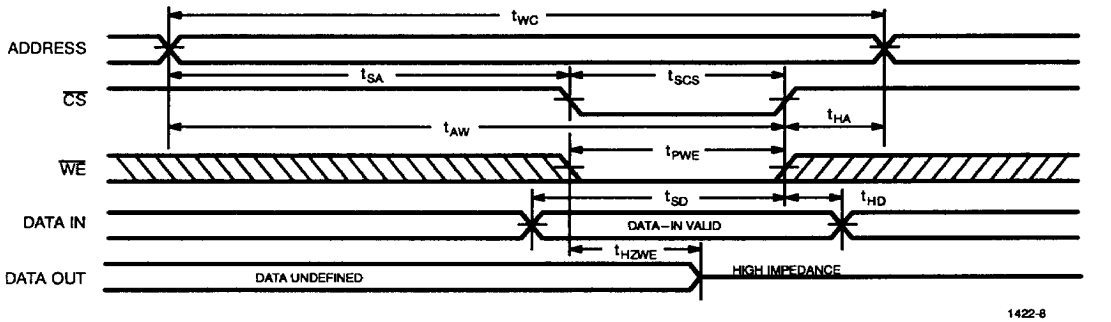
Read Cycle No. 2[7, 10]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[6]



Write Cycle No. 2 ($\overline{CS}$ Controlled) [6, 11]



Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	L	H	Data Out	Read
L	X	L	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CYM1422PS–35C	PS03	Commercial
45	CYM1422PS–45C	PS03	Commercial
55	CYM1422PS–55C	PS03	Commercial

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