

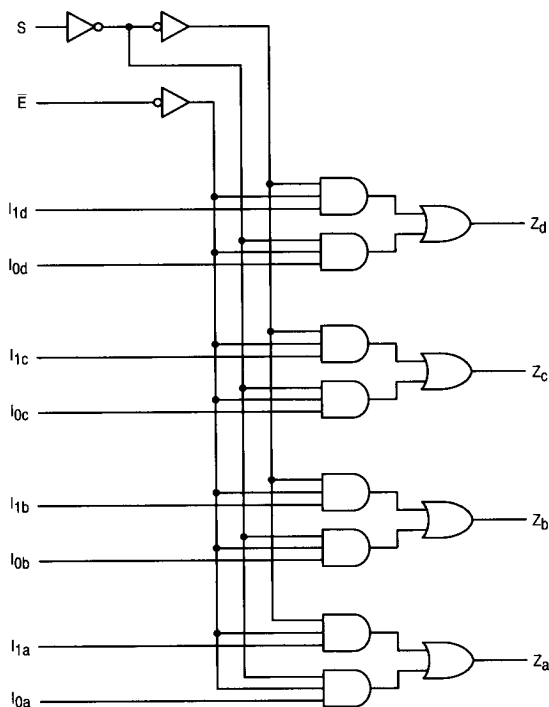


Quad 2-Input Data Selector/Multiplexer

ELECTRICALLY TESTED PER:
MIL-M-38510/33903

The 54F157A is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The 'F157A can also be used to generate any four of the 16 different functions of two variables.

LOGIC DIAGRAM



Military 54F157A



AVAILABLE AS:

- 1) JAN: JM38510/33903BXA
- 2) SMD: N/A
- 3) 883: 54F157A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS
BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
S	1	1	2	VCC
I0a	2	2	3	VCC
I1a	3	3	4	VCC
Za	4	4	5	OPEN
I0b	5	5	7	VCC
I1b	6	6	8	VCC
Zb	7	7	9	OPEN
GND	8	8	10	GND
Zd	9	9	12	OPEN
I1d	10	10	13	VCC
I0d	11	11	14	VCC
Zc	12	12	15	OPEN
I1c	13	13	17	VCC
I0c	14	14	18	VCC
E	15	15	19	VCC
VCC	16	16	20	VCC

BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

Inputs				Output
E-bar	S	I0n	I1n	Zn
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

MOTOROLA MILITARY FAST/LS/TTL DATA

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FUNCTIONAL DESCRIPTION

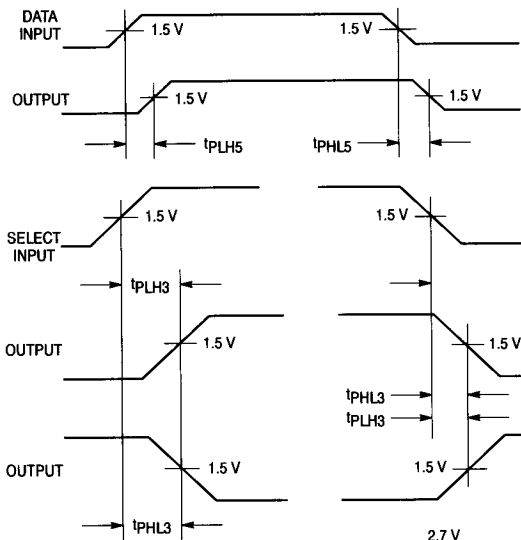
The F157A is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\bar{E}$) is active LOW. When $\bar{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The F157A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are Shown below:

$$Z_a = \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S}) \quad Z_b = \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$Z_c = \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S}) \quad Z_d = \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

A common use of the F157A is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The F157A can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

WAVEFORMS



NOTES:

1. Input pulse and has the following characteristics:
 $PRR \leq 1.0 \text{ MHz}$, $t_r = t_f \leq 2.5 \text{ ns}$, $Z_{OUT} \approx 50 \Omega$.
2. Terminal conditions (pins not designated may be high $\geq 2.0 \text{ V}$, low $\leq 0.8 \text{ V}$, or open).
3. $C_L = 50 \text{ pF} \pm 10\%$ including scope probe, wiring and stray capacitance, without package in test fixture.
4. $R_1 = R_2 = 499 \Omega \pm 5.0\%$.
5. Voltage measurements are to be made with respect to network ground terminal.

AC TEST CIRCUIT

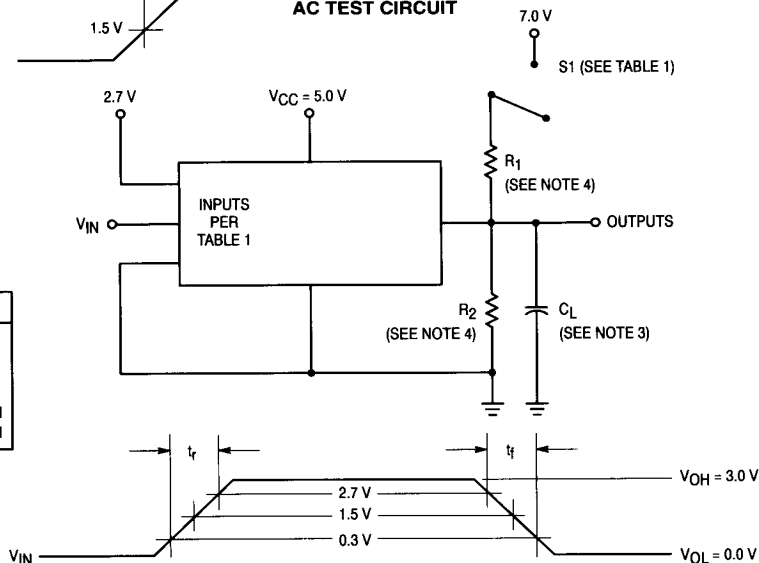


Table 1

Test Type	S1
t_{PLH}	open
t_{PHL}	open
t_{PHZ}	open
t_{PZH}	open
t_{PLZ}	closed
t_{PZL}	closed

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical “1” Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = –1.0 mA, V _{IH} = 2.0 V, S = 0.8 V or 2.0 V, V _{IL} = 0.8 V, $\bar{E}$ = 0.8 V or open.
V _{OL}	Logical “0” Output Voltage		0.5		0.5		0.5	V	V _{CC} = 4.5 V, I _{OL} = 20 mA, V _{IL} = 0.8 V, S = 0.8 V or 2.0 V, V _{IN} = 2.0 V, $\bar{E}$ = 0.8 V.
V _{IC}	Input Clamping Voltage		–1.2					V	V _{CC} = 4.5 V, I _{IN} = –18 mA, other inputs are open.
I _{IH}	Logical “1” Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are open, $\bar{E}$ = 2.7 V or 4.5 V, S = 2.7 V, 0 V or 4.5 V.
I _{IHH}	Logical “1” Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 7.0 V, other inputs are open, $\bar{E}$ = 7.0 V or 4.5 V, S = 7.0 V, 0 V or 4.5 V.
I _{IL}	Logical “0” Input Current	–0.03	–0.6	–0.03	–0.6	–0.03	–0.6	mA	V _{CC} = 5.5 V, V _{IN} = 0.5 V, other inputs are open, $\bar{E}$ = 0.5 V, S = 0.5 V, 4.5 V or 0 V.
I _{OD}	Diode Current	60		60		60		mA	V _{CC} = 4.5 V, all inputs are open, V _{OUT} = 2.5 V, $\bar{E}$ = 5.5 V or open.
I _{OS}	Output Short Circuit Current	–60	–150	–60	–150	–60	–150	mA	V _{CC} = 5.5 V, V _{IN} = 4.5 V, other inputs are open, V _{OUT} = 0 V, S = 0 V, $\bar{E}$ = 0 V.
I _{CC}	Power Supply Current Off		23		23		23	mA	V _{CC} = 5.5 V, V _{IN} = 4.5 V (all inputs).
V _{IH}	Logical “1” Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical “0” Input Voltage		0.8		0.8		0.8	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7	Subgroup 8A		Subgroup 8B				
									per Truth Table with V _{CC} = 4.5 V, (Repeat at) V _{CC} = 5.5 V, V _{INL} = 0.5 V, and V _{INH} = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL1}	Propagation Delay /Data-Output I _n to Z _n	2.5	5.5	1.5	7.5	1.5	7.5	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PLH1}	Propagation Delay /Data-Output I _n to Z _n	2.5	6.0	2.5	7.5	2.5	7.5	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PHL3}	Propagation Delay /Data-Output S to Z _n	3.0	7.0	3.0	9.0	3.0	9.0	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PLH3}	Propagation Delay /Data-Output S to Z _n	4.0	10	4.0	12	4.0	12	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PHL5}	Propagation Delay /Data-Output E to Z _n	2.5	6.5	2.5	7.5	2.5	7.5	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PLH5}	Propagation Delay /Data-Output E to Z _n	5.0	9.5	5.0	13	5.0	13	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.