

54 HSC & HST Series

Radiation Hard High Speed CMOS / SOS Logic

FEATURES

- Radiation Hard to 1 MRad (Si)
- High SEU immunity, latch up free
- Low power CMOS / SOS Technology
- Plug in replacement for 54/74 LS, HC and HCT
- Dual in Line, Leadless Chip Carrier or Flatpack Packages

GENERAL DESCRIPTION

The Marconi CMOS/SOS HSC/T octal interface gates offer the combined benefits of low power, high speed CMOS with the inherent latch up immunity, Single Event Upset (SEU) immunity and high level of radiation hardness of Marconi's Silicon on Sapphire technology. The family of latches offers transparent or clocked operation and has inverted or non-inverted three state output. The decoder family offers two; single 'one-of-eight' latched or unlatched or dual 'one-of-four' configurations. Bus buffering is catered for with symmetrical high current drivers with several configurations of chip select for single or bi-directional operation. The 54 HSC / T series of circuits are pin for pin compatible with the 54LS series octal range.

HSC and HST octal devices have CMOS and TTL compatible inputs / outputs respectively.

Further octal variants to those listed will be available shortly. Please contact Marconi for further information.

The information presented herein is to the best of our knowledge true and accurate. No warranty expressed or implied is made regarding the capacity, performance or suitability of any product. You are strongly urged to ensure that the information given has not been superseded by a more up to date version.

DECODERS / DEMULTIPLEXERS

- 54HSC/T137** One of eight with latched inputs, inverted outputs
- 54 HSC/T138** One of eight with unlatched inputs, inverted outputs
- 54 HSC/T237** One of eight with latched inputs, non-inverted outputs
- 54 HSC/T238** One of eight with unlatched inputs, non-inverted outputs
- 54 HSC/T139** One of four with unlatched inputs, inverted outputs
- 54 HSC/T239** One of four with unlatched inputs, non-inverted outputs

BUFFERS / LINE DRIVERS

- 54 HSC/T240** Bi-directional connections inverting
- 54 HSC/T244** Bi-directional connections non-inverting
- 54 HSC/T241** Bi-directional connections non-inverting, complementary enable
- 54 HSC/T540** Uni-directional connections, inverting
- ~~54 HSC/T540~~ Uni-directional connections, non-inverting

TRANSCEIVERS

- 54 HSC/T245** Non-inverting

TRANSPARENT LATCHES

- 54 HSC/T373** Non-inverting, 3 state outputs
- 54 HSC/T573** Functionally identical to 373 - different pin out
- 54 HSC/T533** Inverting, 3 state outputs
- 54 HSC/T563** Functionally identical to 533 - different pin out

EDGE TRIGGERED 'D' FLIP FLOPS

- 54 HSC/T374** Non-inverting, 3 state outputs
- 54 HSC/T574** Functionally identical to 374 - different pin out
- 54 HSC/T534** Inverting, 3 state
- 54 HSC/T564** Functionally identical to 534 - different pin out

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN	MAX	UNITS
SUPPLY VOLTAGE	-0.5	10	V
INPUT VOLTAGE	-0.3	$V_{DD} + 0.3$	V
CURRENT THROUGH ANY PIN	-20	20	mA
OPERATING TEMP.	-55	125	°C
STORAGE TEMP	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING DC ELECTRICAL CHARACTERISTICS

$V_{DD} = 5V \pm 10\%$. Over full operating temperature range.

SYMBOL	PARAMETER	TOTAL DOSE RADIATION NOT EXCEEDING 3×10^5 RAD (Si)			TOTAL DOSE ≤ 1 MRAD (Si)		UNITS	CONDITION
		MIN	TYP	MAX	MIN	MAX		
V_{DD}	SUPPLY VOLTAGE	4.5	5.0	5.5	4.5	5.5	V	
V_{IH1}	HST Input High Voltage	2.0			2.0		V	
V_{IL1}	HST Input Low Voltage			0.8		0.3	V	
V_{IH2}	HSC Input High Voltage	3.5			3.5		V	
V_{IL2}	HSC Input Low Voltage			1.5		1.0	V	
V_{OH}	Output High Voltage	$V_{DD} - 0.1$			$V_{DD} - 0.1$		V	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -20\mu A$ $I_{OH} = -6.0mA$ $I_{OH} = -11.0mA$
		3.7			3.7		V	
		2.5			2.5		V	
V_{OL}	Output low Voltage			0.1		0.1	V	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 20\mu A$ $I_{OL} = 6mA$ $I_{OL} = 9mA$
				0.2		0.2	V	
				0.4		0.4	V	
I_{II}	Input leakage current			± 10		± 10	μA	$V_{IN} = V_{DD}$ or V_{SS} All inputs
I_{LO}	Output leakage current			± 10		± 10	μA	Outputs disabled. $V_{OUT} = V_{DD}$ or V_{SS}
I_{DD}	Quiescent current		15	160		4000		$V_{IN} = V_{DD}$ Outputs unloaded

AC ELECTRICAL CHARACTERISTICS

$V_{DD} = 5V \pm 10\%$. $C_{CL} = 50pF$. Over full operating temperature range.

PARAMETER	SYM.	DEVICE	VALUE			VALUE			UNITS	CONDITIONS
			54HSC			54HST				
			MIN	TYP	MAX	MIN	TYP	MAX		
Address to Output	t _{PLH}	137		26	34		29	37	ns	
		138		17	25		20	28		
		237		21	29		24	32		
		238		16	24		19	27		
		139		16	24		19	27		
		239		13	21		16	24		
Address to Output	t _{PHL}	137		26	34		29	37	ns	
		138		19	27		22	30		
		237		22	30		25	33		
		238		17	25		20	28		
		139		17	25		20	28		
		239		14	22		17	25		
E to Output	t _{PLH}	137		22	30		25	33	ns	
		138		21	29		24	32		
		237		19	27		22	30		
		238		19	27		22	30		
		139		16	24		19	27		
		239		13	21		16	24		
E to Output	t _{PHL}	137		22	30		25	33	ns	
		138		21	29		24	32		
		237		21	29		24	32		
		238		19	27		22	30		
		139		17	25		20	28		
		239		14	22		17	25		
Set up time	t _{SU}	373 573 533 563	15			15			ns	
Hold time	t _{HOLD}	374 574 534 564 only	0			0			ns	
Rise Time	t _{TLH}	All	5		10	5		10	ns	C _L = 50pF
Fall Time	t _{THL}	All	5		10	5		10	ns	C _L = 50pF
Input Capacitance	C _I	All	3		8	3		8	ns	V _{IN} = 0V
Output Capacitance	C _O	All	3		8	3		8	ns	V _{OUT} = 0V

54 HSC & HST Series

Radiation Hard
High Speed
CMOS/SOS Logic

Marconi
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AC ELECTRICAL CHARACTERISTICS (continued)

$V_{DD} = 5V \pm 10\%$. $C_{CL} = 50pF$. Over full operating temperature range.

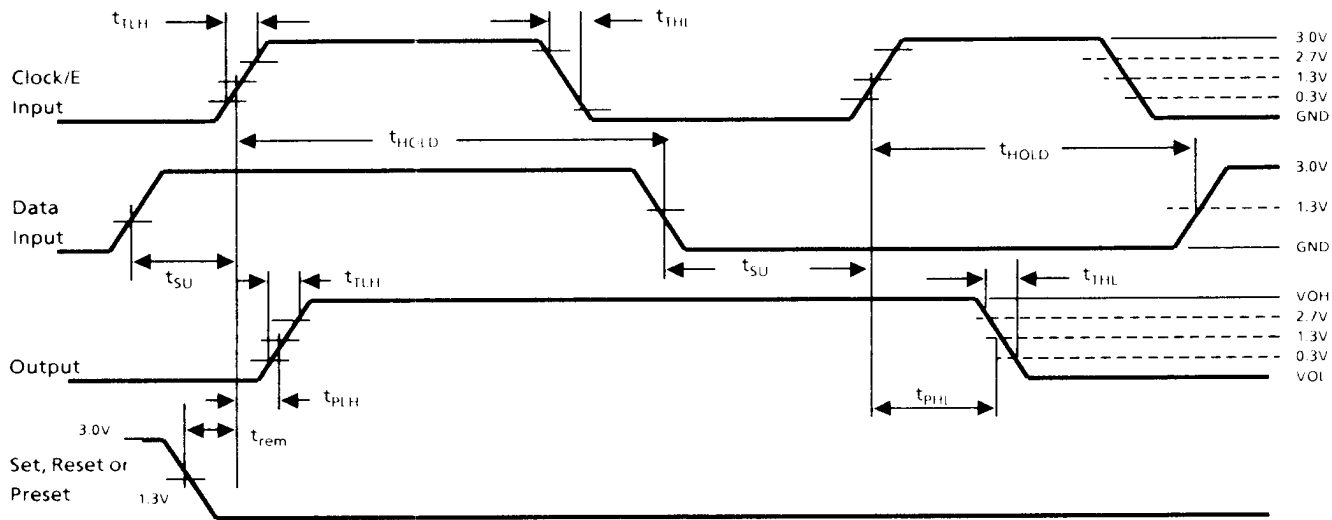
PARAMETER	SYM.	DEVICE	VALUE			VALUE			UNIT	TEST CONDITIONS
			54HSC			54HST				
			MIN	TYP	MAX	MIN	TYP	MAX		
Low to High Output	t_{PLH}	240		12	20		12	23	ns	$C_L = 50pF$
		244		11	29		11	22		
		241		11	29		11	22		
		540		13	21		13	24		
		542		11	29		11	22		
		245		10	28		10	21		
		373/573		19	27		19	30		
		533/563		16	24		16	27		
		374/574		16	24		16	27		
534/564		21	29		21	32				
High to Low Output	t_{PHL}	240		14	22		14	25	ns	$C_L = 50pF$
		244		13	21		13	24		
		241		13	21		13	24		
		540		14	22		14	25		
		542		13	21		13	24		
		245		11	19		11	22		
		373/573		19	27		19	30		
		533/563		16	24		16	27		
		374/574		19	27		19	30		
534/564		22	30		22	33				
Enable to Low	t_{PZL}	240		19	27		19	30	ns	
		244		19	27		19	30		
		241		19	27		19	30		
		540		21	29		21	32		
		542		21	29		21	32		
		245		21	29		21	32		
		373/573		13	21		13	24		
		533/563		13	21		13	24		
		374/574		13	21		13	24		
534/564		13	21		13	24				
Enable to High	t_{PZH}	240		14	22		14	25	ns	
		244		19	27		19	30		
		241		19	27		19	30		
		540		16	24		16	27		
		542		16	24		16	27		
		245		16	24		16	27		
		373/573		16	24		16	27		
		533/563		16	24		16	27		
		374/574		16	24		16	27		
534/564		16	24		16	27				

AC ELECTRICAL CHARACTERISTICS (continued)

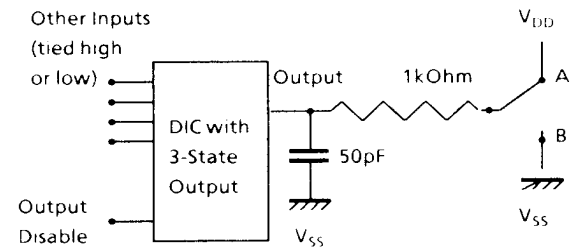
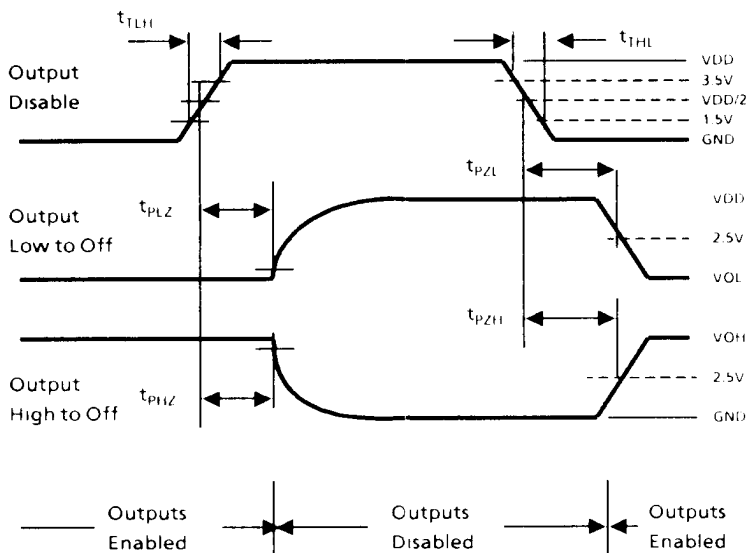
PARAMETER	SYM.	DEVICE	VALUE			VALUE			UNIT	TEST CONDITIONS
			54HSC			54HST				
			MIN	TYP	MAX	MIN	TYP	MAX		
Disable from Low	t _{PLZ}	240		22	30		25	33	ns	
		244		22	30		25	33		
		241		22	30		25	33		
		540		24	32		27	35		
		542		24	32		27	35		
		245		24	32		27	35		
		373/573		14	22		17	25		
		533/563		14	22		17	25		
		374/574		14	22		17	25		
534/564		14	22		17	25				
Set-up Time	t _{SU}	D	15			15			ns	
Hold Time	t _H	D	0			0			ns	
Minimum pulse width	t _W	D	15			15			ns	
LE to High Output	t _{PLHE}	373/573 533/563	19 26		27 34	22 29		30 37	ns	
Le to Low Output	t _{PHLE}	373/573 533/563	19 26		27 34	22 29		30 37	ns	
Rise time	t _{TLH}	All	5		10	5		10	ns	C _L = 50pF
Fall time	t _{THL}	All	5		10	5		10	ns	C _L = 50pF
Input capacitance	C _I	All	3		8	3		8	pF	V _{IN} = 0V
Output capacitance	C _O	All	3		8	3		8	pF	V _{OUT} = 0V

D - Device types 373, 573, 533, 563, 374, 574, 534 and 564 only

TIMING DIAGRAMS



Set-up times, hold times, removal time and propagation delay times

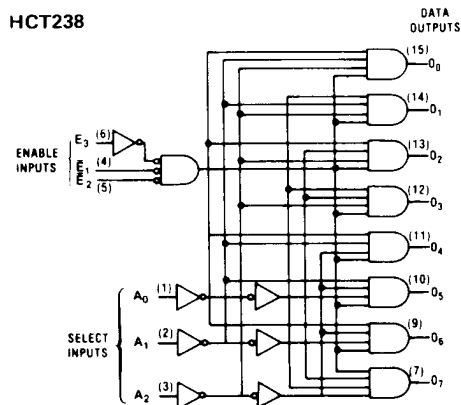
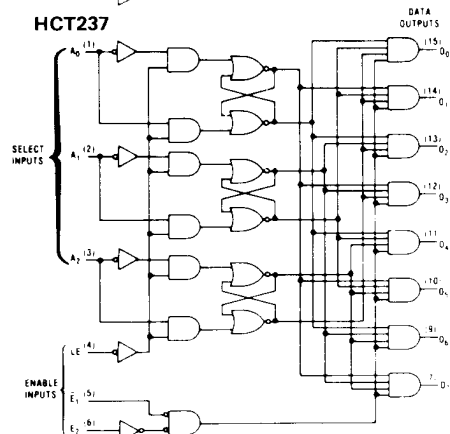
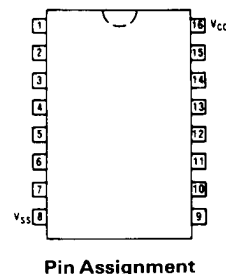
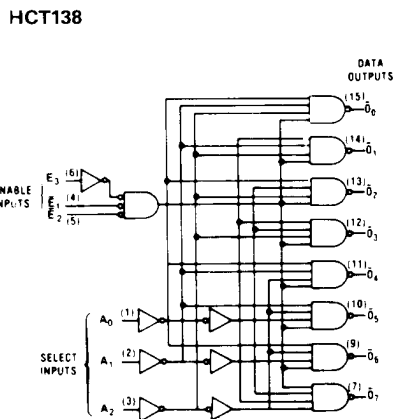
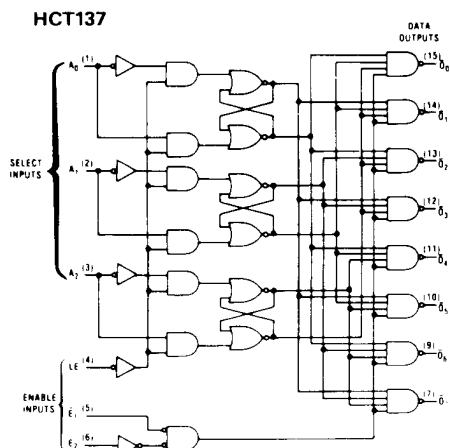


Switch in position A for t_{PLZ} and t_{pZL}
Switch in position B for t_{PHZ} and t_{pZH}

Three-state propagation delay wave shapes and test circuit

LOGIC DIAGRAMS

STANDARD OUTPUT FAMILY



FUNCTION TABLE

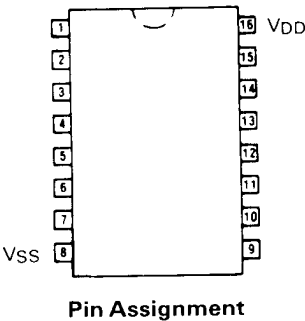
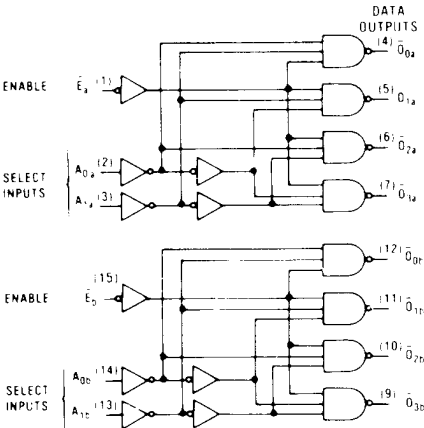
Inputs						Outputs																	
Enable				Select																			
137/237		138/238																					
LE	E ₂	E ₁	E ₃	E ₂ /E ₁	A ₂	A ₁	A ₀	137/8							237/8								
								O ₀	O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇	O ₀	O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇
X	X	H	X	H	X	X	X	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L
X	L	X	L	X	X	X	X	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L
L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L
L	H	L	H	L	L	L	H	L	H	H	H	H	H	H	H	L	H	L	L	L	L	L	L
L	H	L	H	L	L	L	H	L	H	L	H	H	H	H	H	L	L	H	L	L	L	L	L
L	H	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L
L	H	L	H	L	L	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L
L	H	L	H	L	L	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L
L	H	L	H	L	L	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L
H	H	L	—	—	X	X	X																

H = High Level; L = Low Level; X = irrelevant

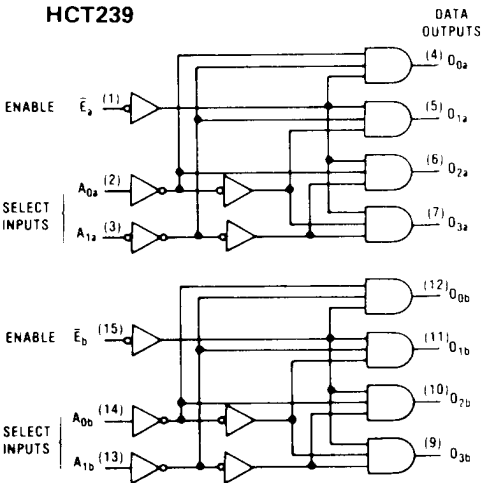
LOGIC DIAGRAMS (continued)

STANDARD OUTPUT FAMILY — continued

HCT139



HCT239



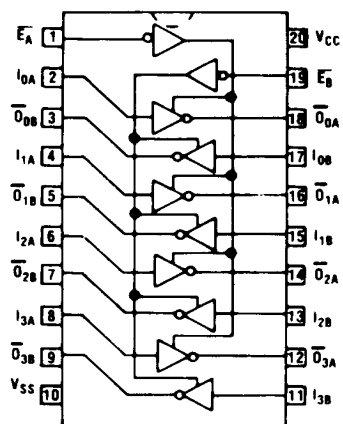
FUNCTION TABLE

Inputs			Outputs							
Enable	Select		139				239			
$\bar{E}$	A ₁	A ₀	O ₀	O ₁	O ₂	O ₃	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$
H	X	X	H	H	H	H	L	L	L	L
L	L	L	L	H	H	H	H	L	L	L
L	L	H	H	L	H	H	L	H	L	L
L	H	L	H	H	L	H	L	L	H	L
L	H	H	H	H	H	L	L	L	L	H

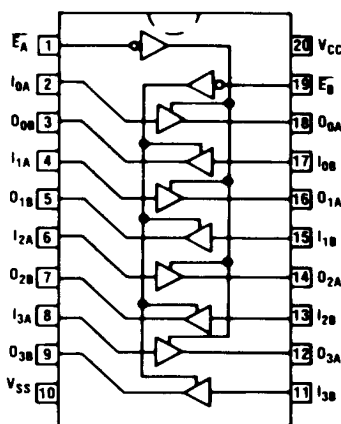
L = Low Level; H = High Level; X = irrelevant

LOGIC DIAGRAMS (continued)

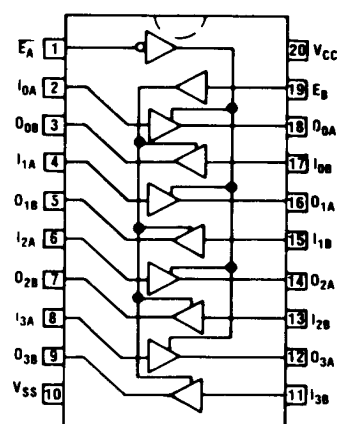
3-STATE OUTPUT FAMILY



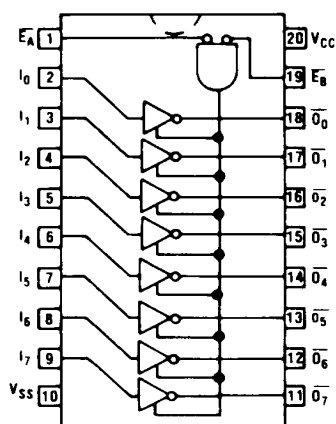
HCT240



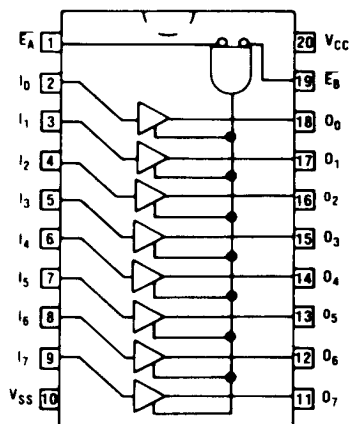
HCT244



HCT241



HCT540



HCT54

FUNCTION TABLE

Inputs				Outputs							
240/4		241		540/1				240	244/1	540	541
$\bar{E}$	IO-3	$\bar{E}A$	EB	IO-3	$\bar{E}A$	EB	IO-7	O0-3	O0-3	O0-7	O0-7
L	L	L	H	L	L	L	L	H	L	H	L
L	H	L	H	H	L	L	H	L	H	L	H
H	X	H	L	X	H	X	X	Z	Z	Z	Z
—	—	—	—	—	X	H	X	—	—	Z	Z

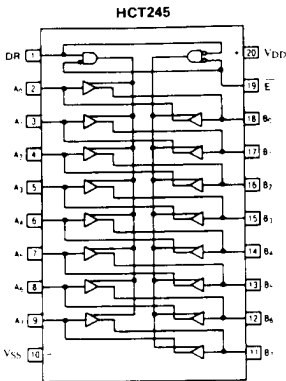
L = Low Level; H = High Level; X = irrelevant; Z = High Impedance

LOGIC DIAGRAMS (continued)

3-STATE OUTPUT FAMILY — continued

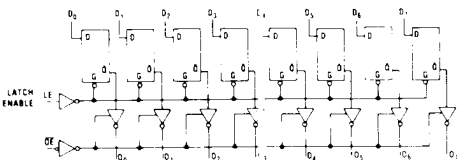
FUNCTION TABLE

Inputs		Output
$\overline{E}$	DR	245
L	L	Bus B data to Bus A
L	H	Bus A data to Bus B
H	X	Isolation



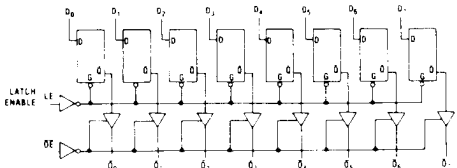
LOGIC DIAGRAMS

HCT373/573

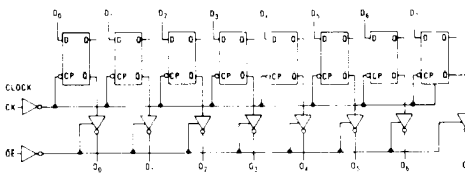


PIN NAMES
D₀ – D₇ Data Inputs
LE Latch Enable (Active HIGH) Input
 $\overline{OE}$ Output Enable (Active LOW) Input
O₀ – O₇ Outputs

HCT533/563

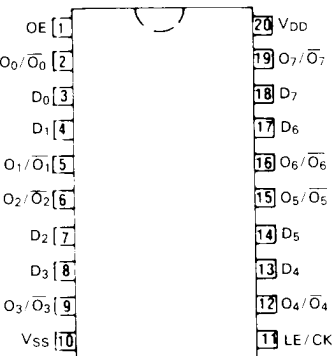
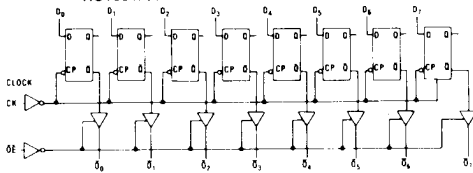


HCT374/574

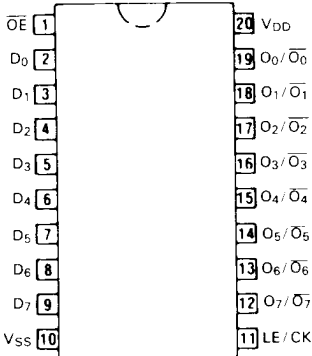


PIN NAMES
D₀ – D₇ Data Inputs
CK Clock (Active HIGH going edge) Input
 $\overline{OE}$ Output Enable (Active LOW) Input
O₀ – O₇ Outputs

HCT534/564



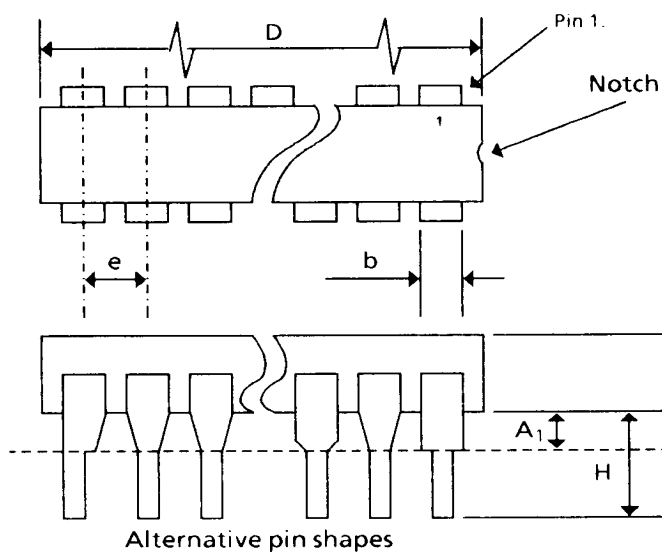
HCT373, HCT533
HCT374, HCT534



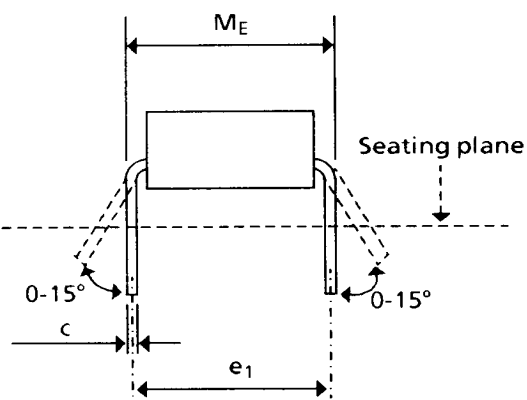
HCT573, HCT563
HCT574, HCT564

PACKAGE OUTLINES

20 Lead Ceramic DIL

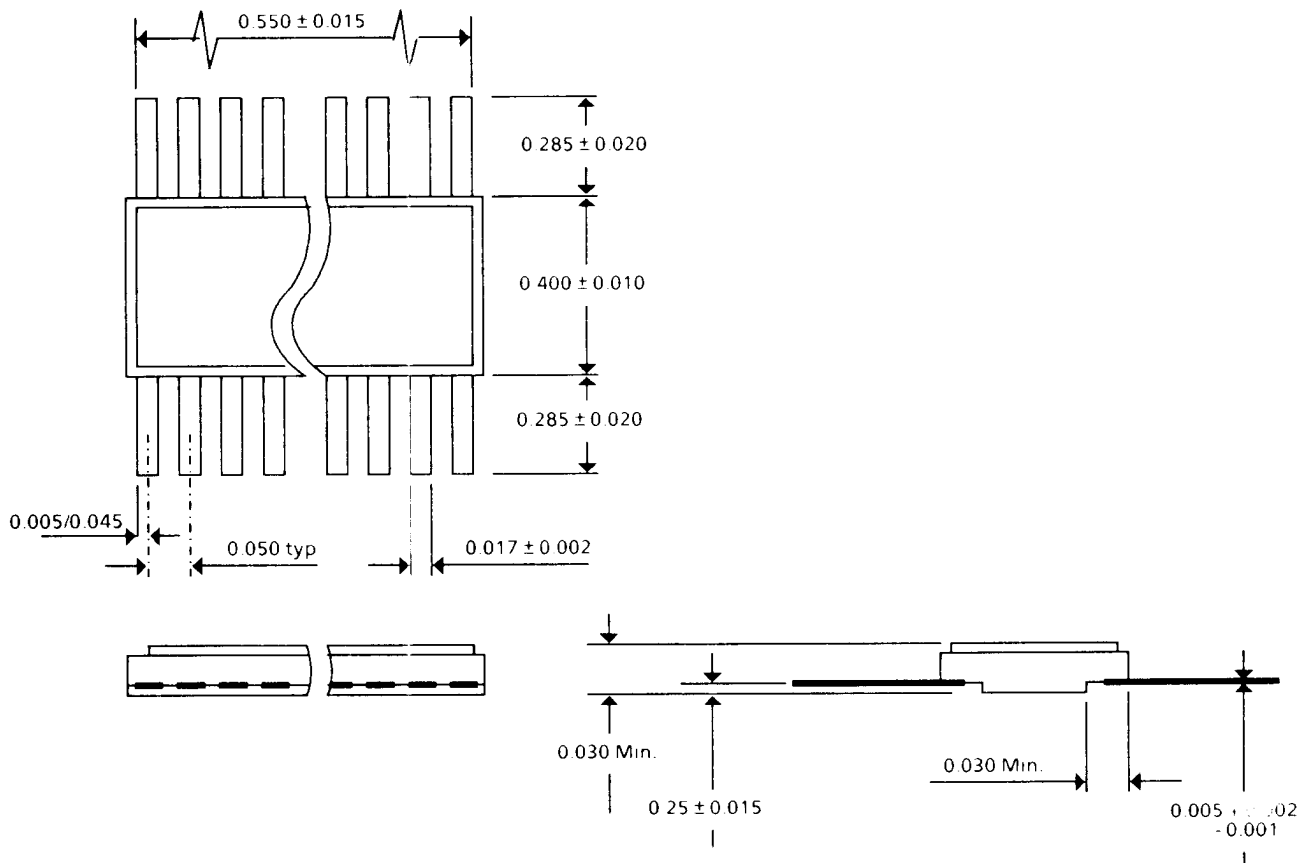


Ref.	Min.	Nom.	Max.
A	0.105		0.145
A ₁	0.025		0.045
b	0.047		0.053
c		0.01	
D	*****		*****
e		0.10 typ.	
e ₁		0.30 typ.	
H	0.175		0.212
M _L			0.32
DIMENSIONS IN INCHES			



PACKAGE OUTLINES (cont)

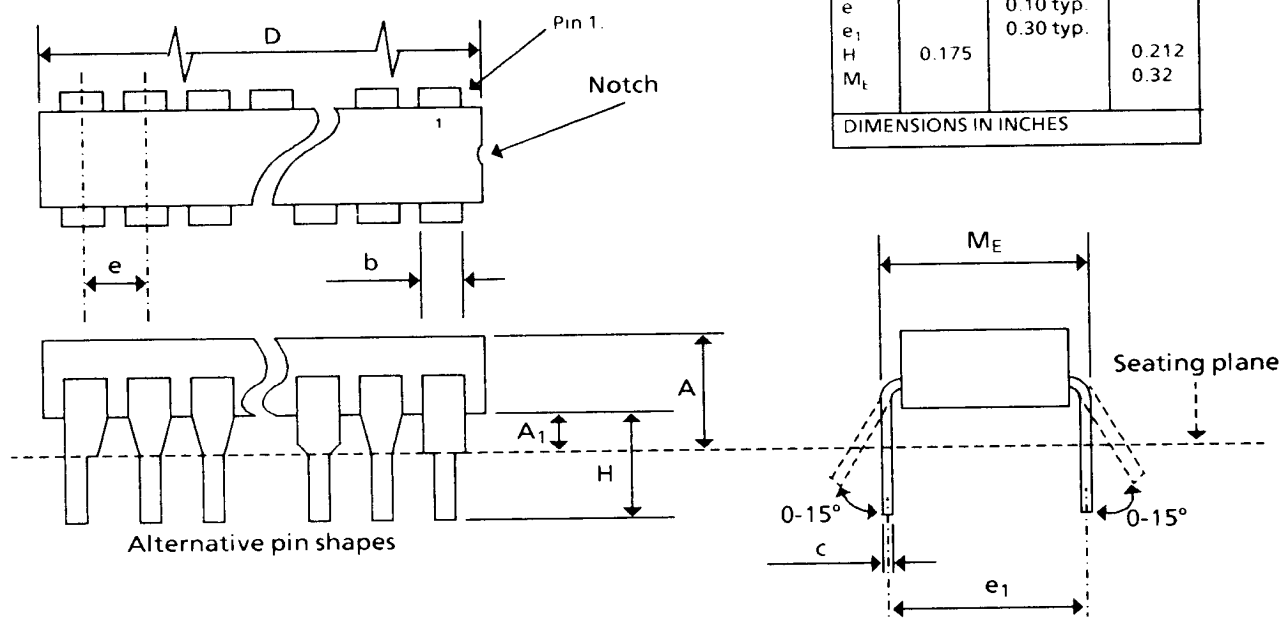
20 Lead Ceramic Flatpack



PACKAGE OUTLINES (cont)

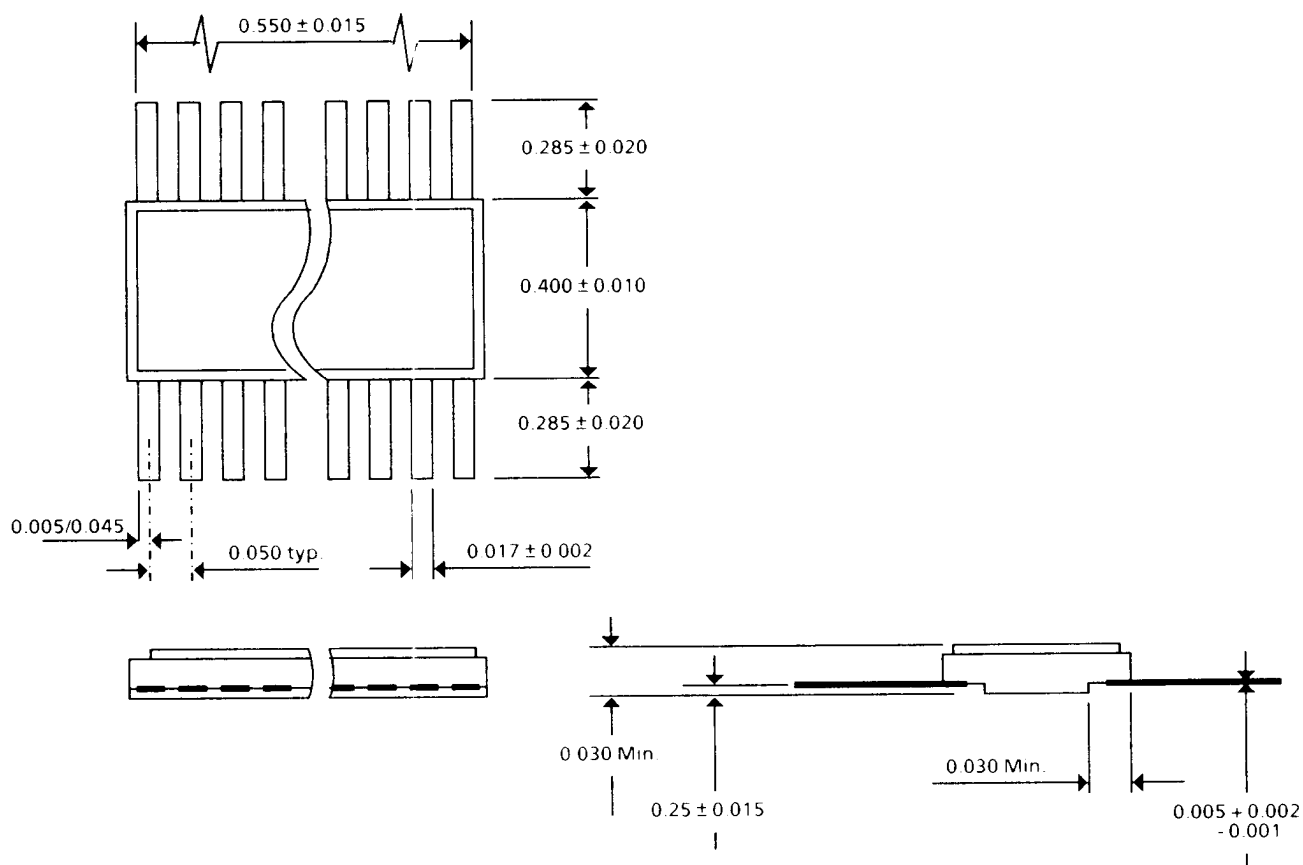
16 Lead Ceramic DIL

Ref.	Min.	Nom.	Max.
A	0.105		0.145
A ₁	0.025		0.045
b	0.047		0.053
c		0.01	
D	*****		*****
e		0.10 typ.	
e ₁		0.30 typ.	
H	0.175		0.212
M _E			0.32
DIMENSIONS IN INCHES			



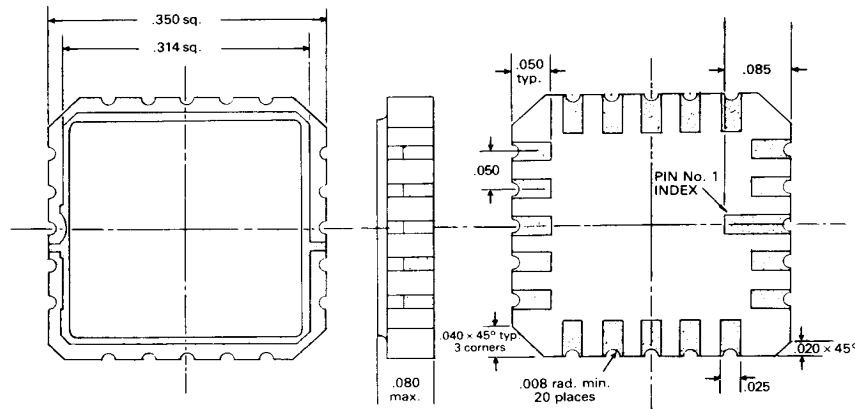
PACKAGE OUTLINES (cont.)

16 Lead Ceramic Flatpack



PACKAGE OUTLINES (cont.)

20 CONTACT LEADLESS CHIP CARRIER



TOTAL DOSE RADIATION TESTING

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

RADIATION PERFORMANCE

Total Dose (Function to specification)	3×10^5 Rad(Si)
Total Dose (Function to 1MRad (Si) specification)	1×10^6 Rad(Si)
Transient Upset (Stored data loss)	3×10^{10} Rad(Si)/s
Transient Upset (Survivability)	$> 1 \times 10^{12}$ Rad(Si)/s
Neutron Hardness (Function to specification)	1×10^{15} neutrons/cm ²
Latch-up	Not possible

54 HSC & HST Series

Radiation Hard
High Speed
CMOS/SOS Logic

Marconi
Electronic Devices

ORDERING INFORMATION

PACKAGE

Unique circuit
designator.

C Ceramic DIL
F Flatpack
L Leadless Chip Carrier
N Naked Die

54xHST139xxx
54xHSC139xxx

RADIATION TOLERANCE

QUALITY LEVEL

'Blank' No tolerance implied
S Radiation hard processing
R 100 kRads (Si) guaranteed
Q 300 kRads (Si) guaranteed
H 1000 kRads (Si) guaranteed

USA Standards (note 1)
B1 Class B
B9 Class B + SEM inspection and PIND screening
S0 Class S without internal visual inspection by customer
S2 Class S

ESA/SCC 9000 (note 2)
T1 level B, Lat 1
T2 level B, Lat 2
T3 level B, Lat 3
T4 level C, Lat 1
T5 level C, Lat 2
T6 level C, Lat 3

'Blank' No tolerance implied
S Radiation hard processing

GB Commercial 0 to 70°C
GC Commercial -55 to 125°C

1 Marconi Electronic Devices quality levels conform to MIL STD 883C class B/S, screening method 5004 and Quality Conformance Inspection method 5005. This does not imply DESC certification, however MIL-M-38510 qualified product listing is being sought.

2 Marconi's specifications for European Space manufacturing flows, including their associated screening procedures, conform to ESA/SCC Generic Specification No.9000. A Process Identification Document, describing the manufacture of these devices, has been approved by the European Space Agency.