HEWLETT® PACKARD

VDE 0884 Approved, High CMR, Wide V_{CC}, Logic Gate Optocoupler

Technical Data

CNW2201
CNW2211

Features

- **5000 V_{RMS}/1 Minute Insulation Withstand Capability**
- **Worldwide Safety Approval**
- **UL1577 (File No. E55361)**
- **CSA Certified-Component Acceptance Notice #5 (File CA88324)**
- **VDE 0884 Certification (VIORM = 1 kV_{RMS})**
- **SEMKO-NEMKO According to IEC 65/950/335 (Pending)**
- **DEMKO-FIMKO/SETI According to IEC 65/950/335**
- **BSI According to BS415/BS EN60950 (BS 7002)/BS EN41003**
- **Very High Common Mode Rejection, 10 kV/μs at 1000 V Specified (CNW2211)**
- **Wide V_{CC} Range (4.5 to 20 Volts)**
- **300 ns Propagation Delay Specified Over The Full Temperature Range**
- **5 MBd Typical Signal Rate**
- **Low Input Current (1.6 mA)**
- **Totem Pole Output (No Pullup Resistor Required)**
- **Performance Specified From -40°C to +85°C**
- **Function Compatible with HCPL-2201/2211**
- **Surface Mount Option Available (Option #300)**

Applications

- **Isolation of High Speed Logic Systems**
- **Computer-Peripheral Interfaces**
- **Microprocessor System Interfaces**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**
- **High Speed Line Receiver**

Description

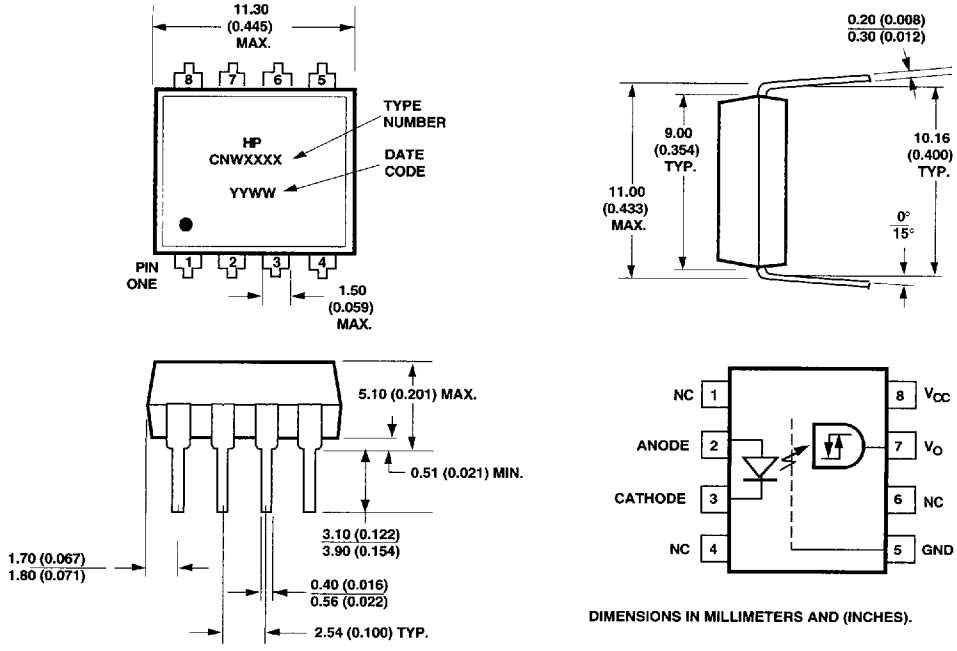
The CNW2201/2211 are single-channel, optically-coupled logic gates. The detectors have totem pole output stages and optical receiver input stages with built-in Schmitt triggers to provide logic-compatible wave-forms, eliminating the need for additional waveshaping.

A superior internal shield on the CNW2211 specifies common mode transient immunity of 10,000 V/μs at a common mode voltage of 1000 volts.

The electrical and switching characteristics of the CNW2201/2211 are specified from -40°C to +85°C and a V_{CC} from 4.5 volts to 20 volts. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS logic and result in lower power consumption compared to other high speed couplers. Logic signals are transmitted with a typical propagation delay of 150 ns.

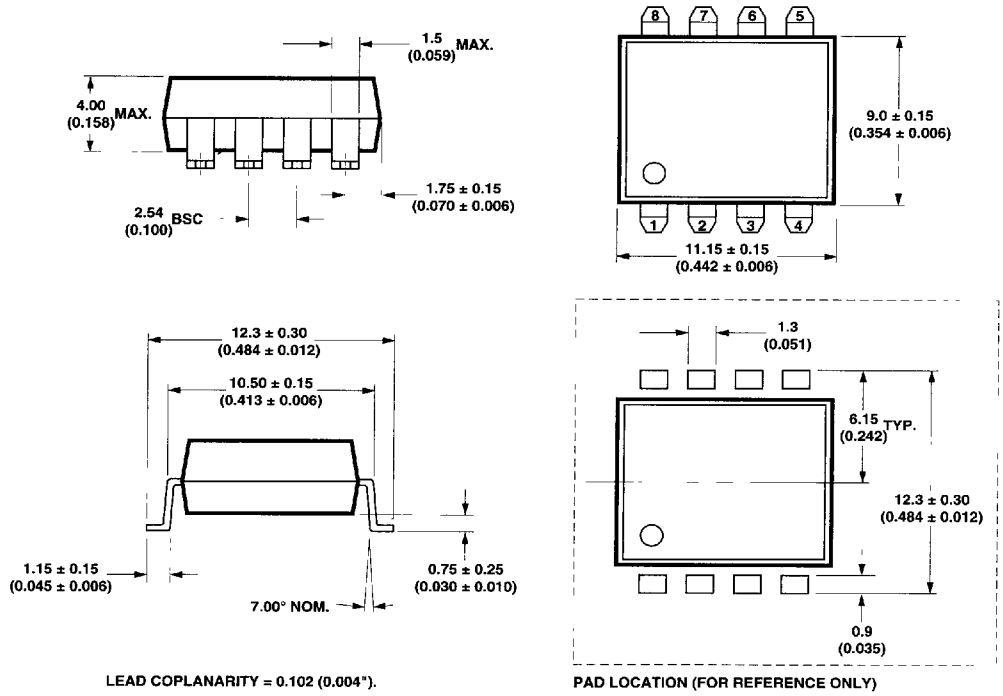
CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Outline Drawing



DIMENSIONS IN MILLIMETERS AND (INCHES).

Gull Wing Surface Mount Option #300

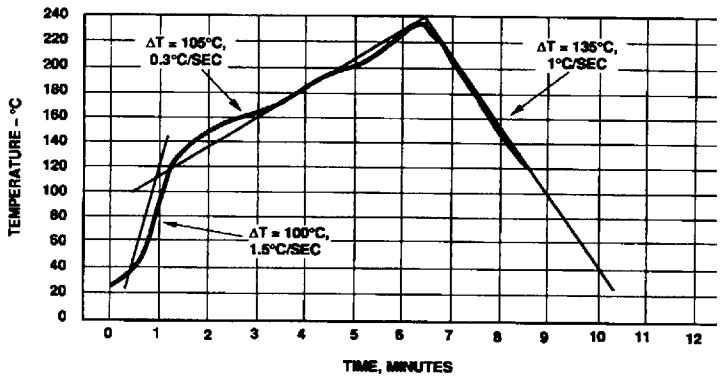


LEAD COPLANARITY = 0.102 (0.004").

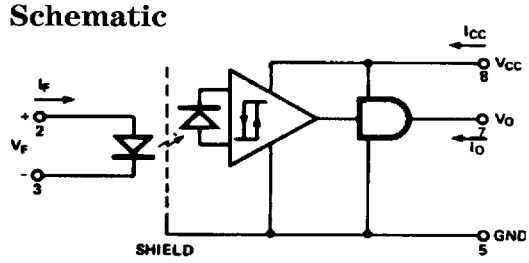
DIMENSIONS IN MILLIMETERS (INCHES).

PAD LOCATION (FOR REFERENCE ONLY)

Temperature Profile



Schematic



TRUTH TABLE (POSITIVE LOGIC)

INPUT	OUTPUT
H	H
L	L

Recommended Circuit Design

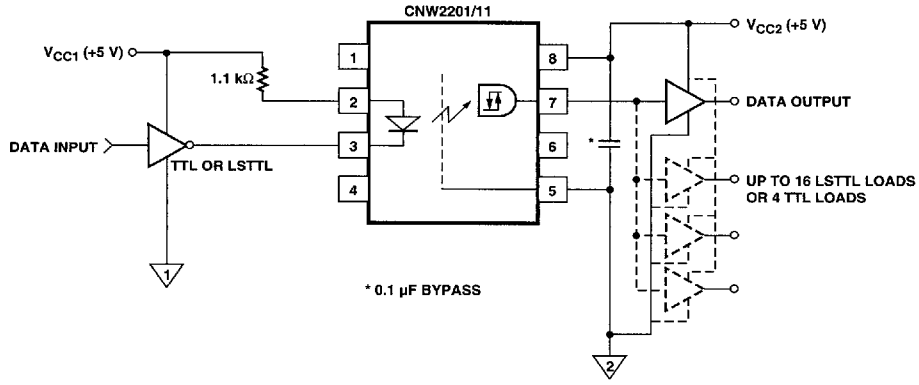


Figure 1a. Recommended LSTTL to LSTTL Circuit Where 500 ns Propagation Delay is Sufficient.

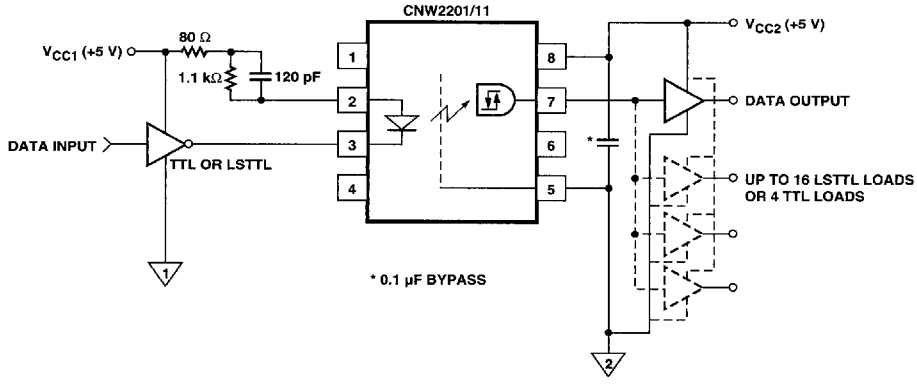


Figure 1b. Recommended LSTTL to LSTTL Circuit for Applications Requiring a Maximum Allowable Propagation Delay of 300 ns.

Regulatory Information

The CNW2201/2211 optocouplers feature 10.16 mm (0.400 inch) wide, eight pin DIP packages. This package was specifically designed to meet worldwide regulatory requirements. The CNW2201/2211 is approved by the following organizations:

UL	Covered under UL 1577, component recognition, FILE E55361
CSA	Certified according to Component Acceptance Notice #5 (File CA88324)
VDE	Approved according to VDE 0884/06.92
NORDIC	Tested for application (reinforced insulation) - Class II applications for plugable apparatus in normal tight execution. FIMKO/SETI-SEMKO-NEMKO-DEMKO according to IEC65/IEC950/IEC335. (SEMKO-NEMKO pending)
BSI	Certification according to BS415:1990, BS EN60950: 1992 (BS 7002: 1992), and EN41003: 1993 for Class II applications.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min External Clearance (External Air Gap)	L(IO1)	9.6	mm	Measured from input terminals to output terminals, through air, shortest distance
Min. External Creepage (External Tracking Path)	L(IO2)	10.0	mm	Measured from input terminals to output terminals, along body of optocoupler, shortest distance
Min. Internal Clearance (Internal Plastic Gap)		1.0	mm	Through insulation distance conductor to conductor, emitter to detector
Min. Internal Creepage (Internal Tracking Path)		4.0	mm	Measured from emitter to detector, along internal cavity wall.
Comparative Tracking Index	CTI	200	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material group (DIN VDE 0110)

VDE 0884 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 Part 1/1.89, Table 1 For Rated Mains Voltage 600 V_{rms} For Rated Mains Voltage 1000 k V_{rms}		 I-IV I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110 Part 1/1.89)		2	
Maximum Working Insulation Voltage	V_{IOWM}	1414	V_{PEAK}
	V_{IORM}	1000	V_{rms}
Input to Output Test Voltage, Method b* V_{PR} = 1.875 x V_{IORM}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2652 1875	V_{PEAK} V_{rms}
Input to Output Test Voltage, Method a* V_{PR} = 1.5 x V_{IORM}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	2121 1500	V_{PEAK} V_{rms}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{tm} = 10 sec)	V_{IOTM}	8000	V_{PEAK}
Safety-Limiting Values (Maximum values allowed in the event of a failure, also see Figure 15) Case Temperature	 T_S	 150	 °C
Current (Input Current I_F, P_S = 0)	I_S	400	mA
Output Power (obtained by setting pin 8 = 5.5 V, pins 7,6,5 = ground)	P_S, output	700	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_{IO}	$>10^9$	

*Refer to the front of the Optocoupler section in the current Optoelectronics Designer's Catalog for a more detailed description of VDE 0884 and other product safety regulations.
Note: Optocouplers providing safe electrical separation per VDE0884 do so only within the safety-limiting values to which they are qualified. Protective cut-out switches must be used to ensure that the safety limits are not exceeded.

Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Ambient Operating Temperature ..... -40°C to +85°C
Reflow Temperature Profile ..... See Outline Drawing
Lead Solder Temperature (up to seating plane) ..... 260°C for 10 s
Peak Transient Input Current ..... 40 mA
(pulse width 200 μs, duty cycle 1%)
Average Input Current - I_F ..... 10 mA
Average Output Current - I_O ..... 25 mA
Reverse Input Voltage - V_R ..... 3 V
Supply Voltage - V_{CC} ..... 20 V
Output Voltage V_O ..... -0.5 to 20V
Total Package Power Dissipation P_O ..... 210 mW[1]

Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Forward Input Current	$I_{F(ON)}$	1.6	5	mA
Forward Input Voltage (LED Off)	$V_{F(OFF)}$	-	0.8	Volts
Operating Temperature	T_A	-40	85	°C
Junction Temperature	T_J	-40	125	°C
Fan Out	N		4	TTL Loads

Electrical Specifications

-40°C T_A 85°C, 4.5 V V_{CC} 20 V, 1.6 mA $I_{F(ON)}$ 5 mA, 0 V $V_{F(OFF)}$ 0.8 V.
All Typicals at T_A = 25°C, V_{CC} = 5 V, $I_{F(ON)}$ = 3 mA, unless otherwise specified.
See Note 6.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 6.4 mA (4 TTL Loads)		2,4	
Logic High Output Voltage	V_{OH}	2.4	*		Volts	I_{OH} = -2.6 mA		3,4,8	
		2.7				I_{OH} = -0.4 mA			
Output Leakage Current ($V_{OUT} > V_{CC}$)	I_{OHH}			100	μA	V_O = 5.5 V	I_F = 5 mA		
				500		V_O = 20 V			
Logic Low Supply Current	I_{CCL}		3.7	6.0	mA	V_{CC} = 5.5 V	V_F = 0 V, I_O = Open		
			4.3	7.0		V_{CC} = 20 V			
Logic High Supply Current	I_{CCH}		2.4	4.0	mA	V_{CC} = 5.5 V	I_F = 5 mA, I_O = Open		
			2.7	5.0		V_{CC} = 20 V			
Logic Low Short Circuit Output Current	I_{OSL}	15			mA	$V_O = V_{CC}$ = 5.5 V	V_F = 0 V		2
		20				$V_O = V_{CC}$ = 20 V			
Logic High Short Circuit Output Current	I_{OSH}	-10			mA	V_{CC} = 5.5 V	I_F = 5 mA, V_O = GND		2
		-20				V_{CC} = 20 V			
Input Forward Voltage	V_F		1.5	1.82	Volts	T_A = 25°C	I_F = 5 mA	5	
				1.95					
Input Reverse Breakdown Voltage	BV_R	3				I_R = 100 μA			
Input Capacitance	C_{IN}		70		pF	V_F = 0, f = 1 MHz, Pins 2 and 3			
Input Diode Temperature Coefficient	V_F/T_A		-1.4		mV/°C	I_F = 5 mA			
Input-Output Insulation	V_{ISO}	5000			V_{RMS}	RH < 50%, t = 1 min., T_A = 25°C			3,7
Resistance (Input-Output)	R_{I-O}	10^{12}	10^{13}			T_A = 25°C; V_{I-O} = 500 V			3
		10^{11}				T_A = 100°C; V_{I-O} = 500 V			
Capacitance (Input-Output)	C_{I-O}		0.5	0.6	pF	f = 1 MHz, T_A = 25°C			3

*Typical $V_{OH} = V_{CC}$ - 2.1 V.

Switching Specifications

-40°C T_A 85°C, 4.5 V V_{CC} 20 V, 1.6 mA $I_{F(ON)}$ 5 mA, 0 V $V_{F(OFF)}$ 0.8 V.
All typicals at T_A = 25°C, V_{CC} = 5 V, $I_{F(ON)}$ = 3 mA unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		160		ns	Without Peaking Capacitor	6, 7	4
			150	300		With Peaking Capacitor		
Propagation Delay Time to Logic High Output Level	t_{PLH}		180		ns	Without Peaking Capacitor	6, 7	4
			90	300		With Peaking Capacitor		
Output Rise Time (10-90%)	t_r		30		ns		6, 9	
Output Fall Time (90-10%)	t_f		7		ns		6, 9	

Parameter	Symbol	Device	Min.	Units	Test Conditions		Fig.	Note
Logic High Common Mode Transient Immunity	$\|CM_H\|$	CNW2201	1,000	V/μs	$\|V_{CM}\|$ = 50 V I_F = 1.6 mA	V_{CC} = 5 V T_A = 25°C	10	5
		CNW2211	10,000	V/μs	$\|V_{CM}\|$ = 1000 V I_F = 5.0 mA			
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	CNW2201	1,000	V/μs	$\|V_{CM}\|$ = 50 V	V_F = 0 V $_{CC}$ = 5 V T_A = 25°C	10	5
		CNW2211	10,000	V/μs	$\|V_{CM}\|$ = 1000 V			

1. Derate total package power dissipation, P, linearly above 70°C free air temperature at a rate of 4.5 mW/°C.
2. Duration of output short circuit time should not exceed 10 ms.
3. Device considered a two terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
5. CM_L is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic low state V_O < 0.8 V. CM_H is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state V_O > 2.0 V.
6. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
7. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage 6000 V_{rms} for one second (leakage detection current limit, I_{I-O} 5 μA). This test is performed before the 100% production test for partial discharge (Method b) shown in the VDE 0884 Insulation Characteristics Table.

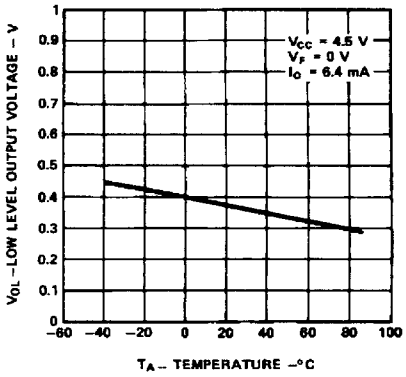


Figure 2. Typical Logic Low Output Voltage vs. Temperature.

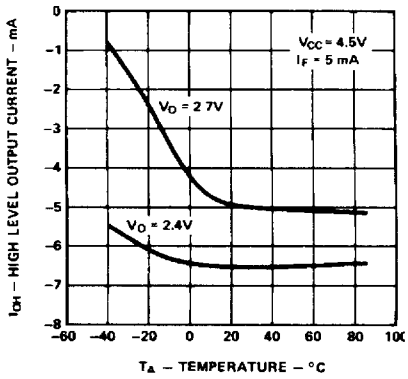


Figure 3. Typical Logic High Output Current vs. Temperature.

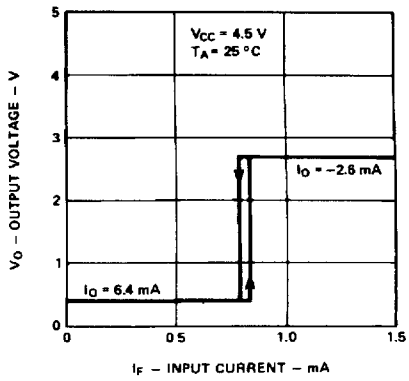


Figure 4. Output Voltage vs. Forward Input Current.

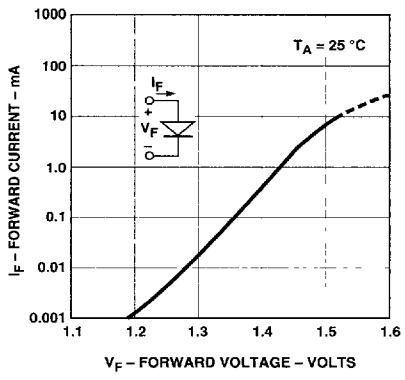
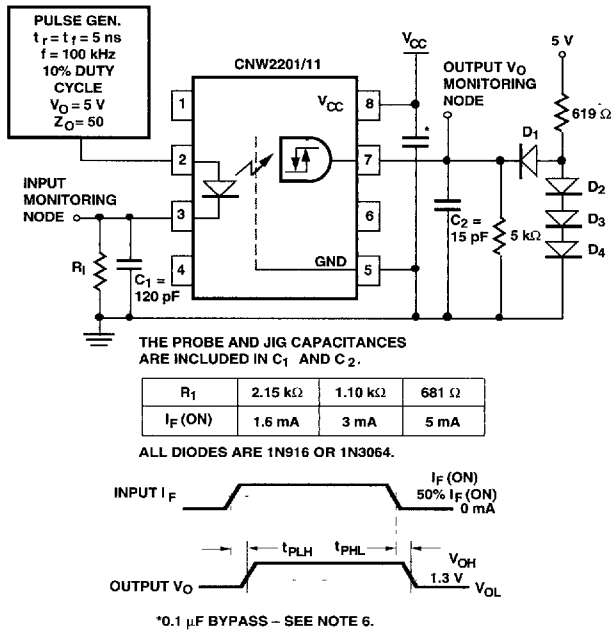


Figure 5. Typical Input Diode Forward Characteristic.



R_1	2.15 kΩ	1.10 kΩ	681 Ω
I_F (ON)	1.6 mA	3 mA	5 mA

Figure 6. Circuit for t_{plh}, t_{phl}, t_r, t_f.

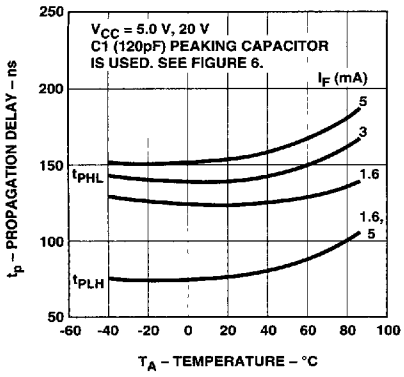


Figure 7. Typical Propagation Delays vs. Temperature.

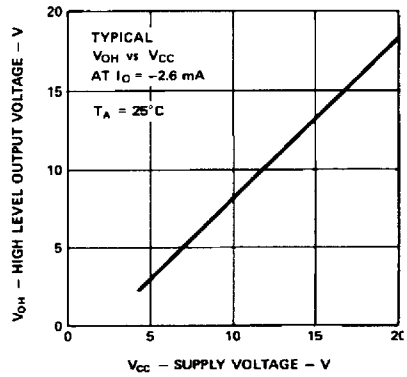


Figure 8. Typical Logic High Output Voltage vs. Supply Voltage.

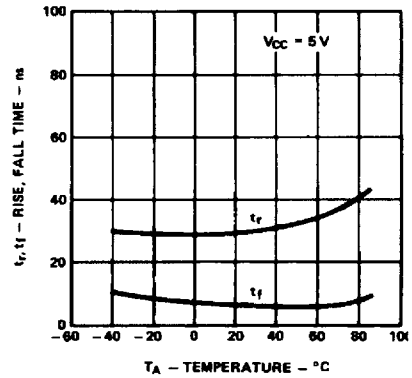


Figure 9. Typical Rise, Fall Time vs. Temperature.

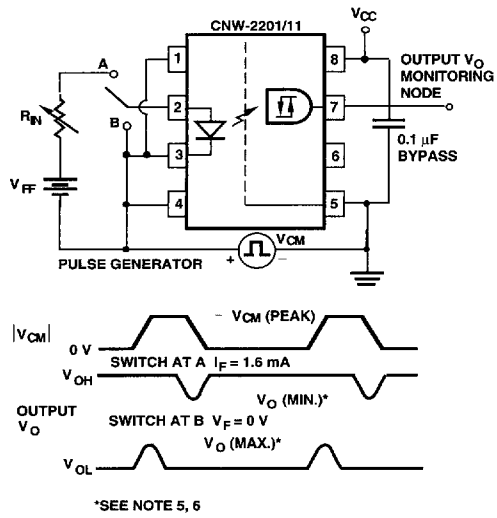


Figure 10. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

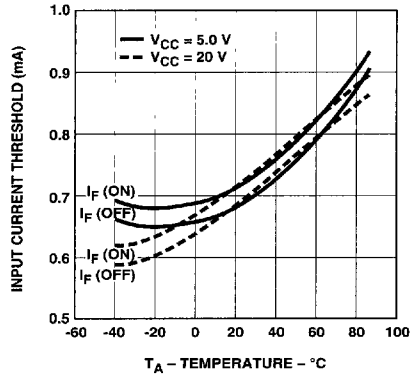


Figure 11. Typical Input Threshold Current vs. Temperature.

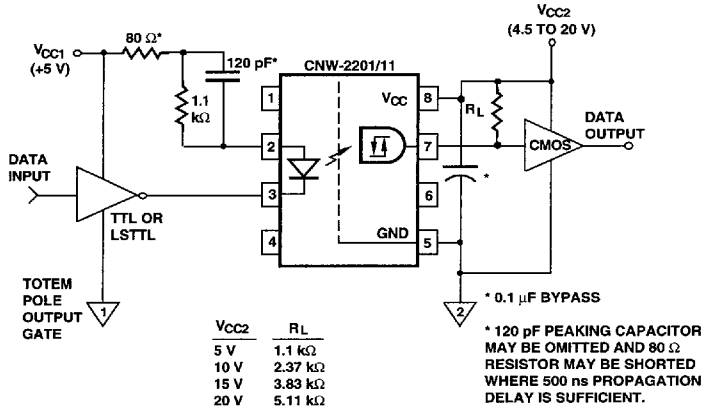


Figure 12. LSTTL to CMOS Interface Circuit.

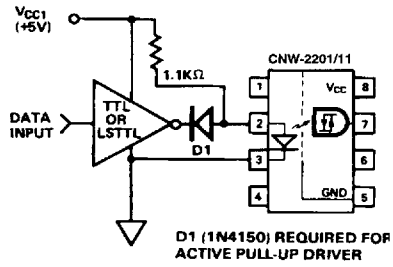


Figure 13. Alternative LED Drive Circuit.

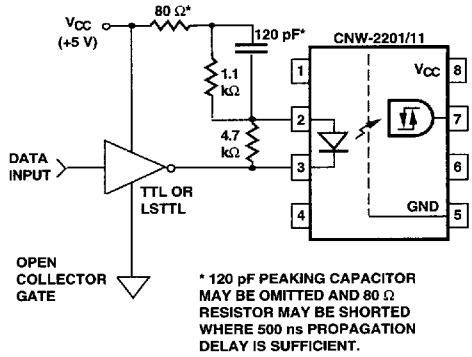


Figure 14. Series LED Drive with Open Collector Gate (4.7 k Resistor Shunts I_{OH} form the LED).

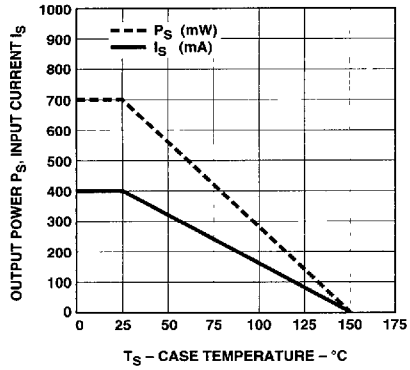


Figure 15. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per VDE 0884.

For more information:

United States*

Europe*

Far East/Australasia: (65) 290-6305

Canada: (416) 206-4725

Japan: (81) 3 3331-6111

*Call your local HP sales office listed in your telephone directory. Ask for a Components representative.

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