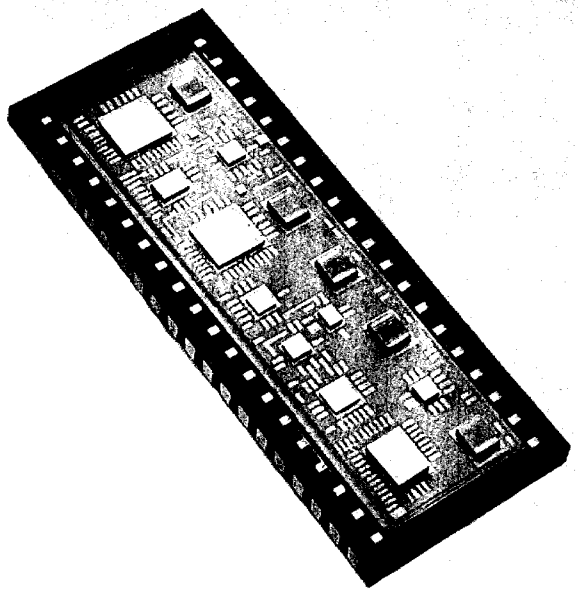
DUAL SERIAL/ DUAL PARALLEL PORT INTERFACE MODULE DHC8-DPDS SERIES

Advance Information

White Technology, Inc.

001609



FEATURES

- **200°C Operating Temperature**
- **Two Separate Serial Ports**
- **Two Separate Parallel Ports**
- **Single 5 Volt Power Supply**
- **Microprocessor Bus Oriented Interface**
- **Separate Internal Baud Rate Generator For Each Serial Port—72 Selectable Baud Rates**
- **16 Programmable I/O Pins**
- **Bus-Hold Circuitry on I/O Ports—Eliminates Pull-Up Resistors**
- **2.5 mA Drive Capability On All I/O Ports**

DESCRIPTION

The White Technology, Inc. DPDS module is designed for hostile environments and will operate at +200°C. It is designed to interface directly to the White Technology, Inc. DHC8-P85 and all future DHC Series microcomputer modules. It is ideal for data acquisition or any control application which requires specific bit control. The DPDS also allows direct connection to printer or host computer when developing software for the White Technology, Inc. DHC series microcomputers.

The DHC8-DPDS-X contains two serial ports and two 8-bit parallel ports in a single 40-pin DIP.

Each serial port has its own baud rate generator, and accepts Standard RS232 input levels.

Each parallel port is 8 bits wide with bus-hold circuitry to eliminate pull-up resistors. Each port can be programmed for either input or output.

The entire module is 3-state design for easy interface to microprocessor bus.

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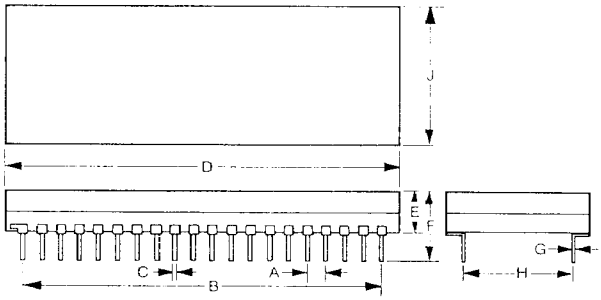
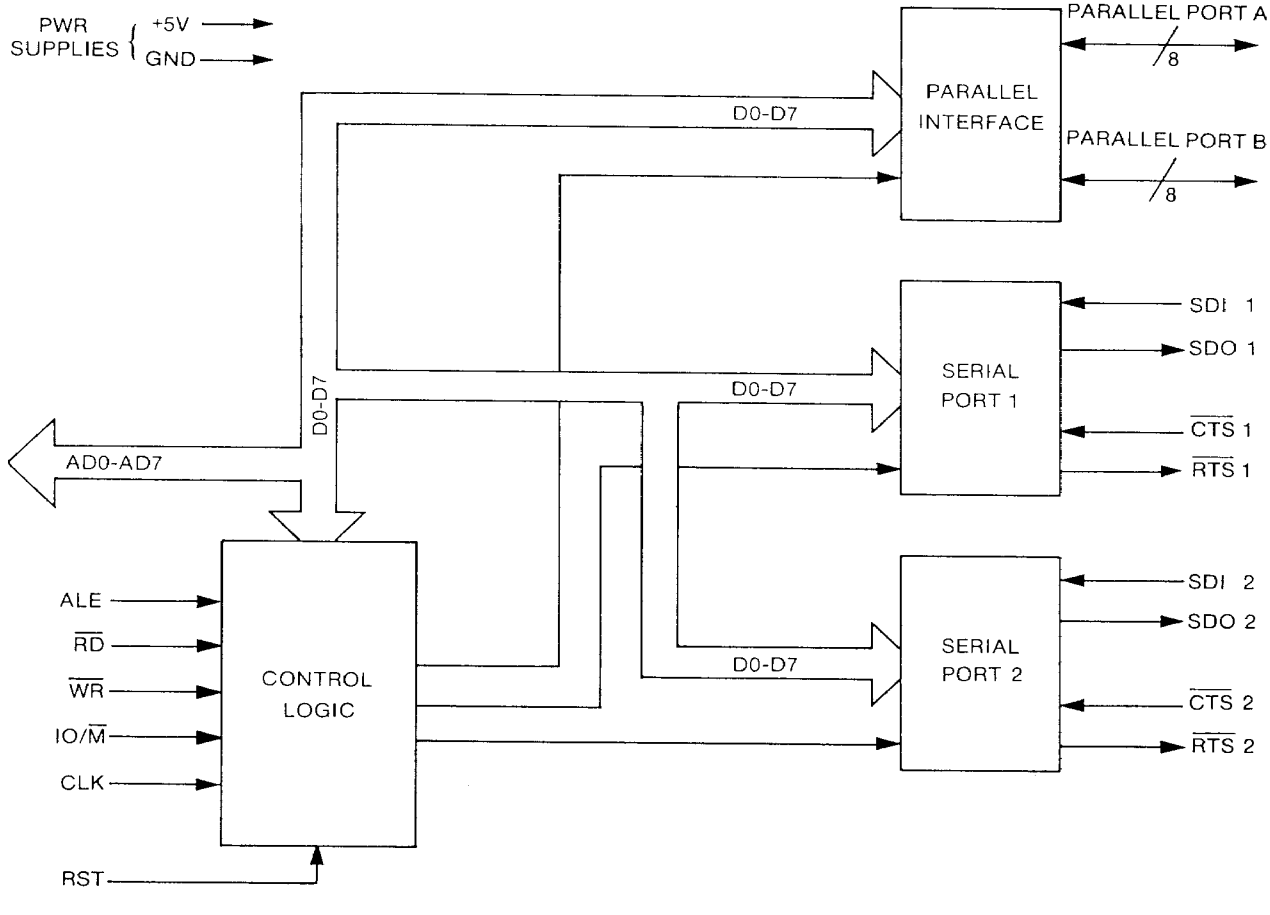
CASE OUTLINE



DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.095	.105	2.4	2.7
B	1.802	1.908	45.8	48.5
C	.016	.020	0.4	0.5
D	2.074	2.116	52.7	53.7
E	.226	.284	5.7	7.2
F	.395	.480	10	12.2
G	.008	.012	.2	.3
H	.590	.610	15	15.5
J	.780	.805	19.8	20.4

BLOCK DIAGRAM



PIN DESCRIPTION

I/O	Pin	Symbol	Active Level	Description
O	1, 29	SDO	Low	Serial Data Output: A mark (0) is low and a space (1) is high.
I	2, 35	$\overline{CTS}$	Low	Clear To Send.
O	3, 38	$\overline{RTS}$	Low	Request To Send: the $\overline{RTS}$ signal can be set (Low) by writing a logic 1 to the appropriate bit in the MCR. This signal is cleared (High) by writing a logic 0 to the the same bit in the MCR or wherever a $\overline{RST}$ (High) is applied to the DPDS.
I/O	4-11	PA0-PA7	High	Parallel Port A—Bits 0-7.
I/O	12-19	AD0-AD7	High	Address/Data Bits 0-7: multiplexed Address/Data bus provides eight 3-state Input/Output lines for the transfer of Data, Control, and status information between the DPDS and CPU.
	20	GND	Low	Ground: power supply ground connection.
I/O	21-28	PB0-PB7	High	Parallel Port B, bits 0-7.
I	30	ALE	High	Address Latch Enable: ALE true enables the internal transparent address latches for A0-A7 inputs. The address is latched when ALE goes false (Low).
I	31	$\overline{WR}$	Low	Write: The $\overline{WR}$ input causes data from the data bus (D0-D7) to be input to the DPDS.
I	32	$\overline{RD}$	Low	Read: the $\overline{RD}$ input causes data to be output to the data bus (D0-D7).
	33, 39	SDI	Low	Serial Data Input (1), (2): serial data input to the DPDS receiver circuits. A mark (0) is Low and a space (1) is High.
I	34	IO/M		Input/Output $\overline{MEMORY}$: input from CPU signaling if a Read or Write is to Memory or to an input/output device. A High (1) is to a I/O device, a Low (0) is to Memory.
I	36	RST	High	Reset In: a high will reset both serial and both parallel ports internally pulled low.
I	37	CLK		Clock Input: is used for internal baud rate generation.
I	40	Vcc	High	+5 Volt Supply: positive power supply connection.

DPDS SERIAL PORTS (SP)

UART STATUS REGISTER (USR)

The USR provides a single register that the controlling system can examine status of the SP.

Bits 5, 6, 7 of USR are the only ones used and are as follows:

Bit 5— CTS: Clear To Send is an inverted signal of the CTS input pins. This is used to check if the device has issued a Clear To Send signal.

Bit 6— TBRE: Transmit Buffer Register Empty. Is used to check if SP has finished transmitting the last character.

1 = TBRE empty, transmission complete.

0 = TBRE not empty, transmitting.

Bit 7— DR: Data Ready is used to check if data is ready to be read by CPU.

1 = data ready.

0 = data not ready.

PROGRAMMING THE DPDS SERIAL PORTS (SP)

The complete functional definition of the SP is programmed by the systems software. A set of control words (UCR, BRSR and MCR) must be sent out by the CPU to initialize the SP to support the desired communication format. These control words will program the character length, number of stop bits, baud rate etc. Once programmed, the SP is ready to perform its communication functions.

The control registers can be written to in any order, however the MCR should be written to last because it controls the modem control outputs and the receiver enable bit. Once the SP is programmed and operational these registers can be updated any time that the SP is not immediately transmitting or receiving data.

Table 1 shows the required control signals to access the SP internal registers.

ALE	$\overline{CS0}$	CS1	A1	A0	$\overline{WR}$	$\overline{RD}$	OPERATION
1 or ↓	0	1	0	0	↑	1	Data bus → TBR
1 or ↓	0	1	0	0	1	↓	RBR → Data Bus
1 or ↓	0	1	0	1	↑	1	Data bus → UCR
1 or ↓	0	1	1	0	↑	1	Data bus → MCR
1 or ↓	0	1	1	0	1	↓	MCR → Data bus
1 or ↓	0	1	1	1	↑	1	Data bus → BRSR

TABLE 1

The Address Latch Enable (ALE) input acts as an address latch control signal. For multiplexed bus applications, the address inputs A0, A1 are latched when ALE goes low. In this case A0 and A1 are not required to be held true for the entire bus cycle.

The following descriptions discuss the control registers in detail.

UART CONTROL REGISTER (UCR)

The UCR is a write only register which configures the UART transmitter and receiver circuits. Data bits D7 and D6 are not used but should always be set to a zero in order to insure software compatability with future product upgrades. During the Echo Mode, the transmitter always repeats the received word and parity, even when the UCR is programmed with different or no parity.

UCR

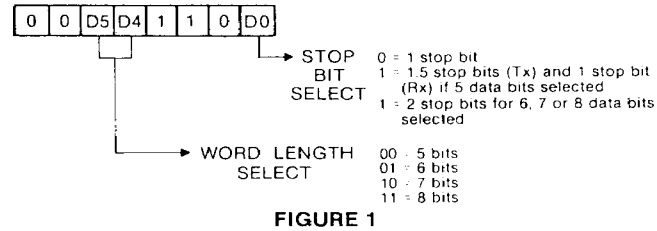


FIGURE 1

BAUD RATE SELECT REGISTER (BRSR)

The SP is designed to operate with a single external clock. The Baud Rate Select Register is used to select which divide ratio (one of 72) the internal Baud Rate Generator circuitry will use. The internal circuitry is separated into two separate counters, a Prescaler and a Divisor Select. The Prescaler can be set to any one of four division rates, ÷1, ÷3, ÷4, or ÷5. This Prescaler design has been optimized to provide standard baud rates using any one of three popular crystal frequencies. By using one of these common system clock frequencies, 1.8432 MHz, 2.4576 MHz or 3.072 MHz and a Prescaler of ÷3, ÷4 or ÷5 respectively, the Prescaler output will provide a constant 614,400 Hz. When this frequency is further divided by the Divisor Select counter, any of the standard baud rates from 50 to 38.4 Kbaud can be selected (see Table 2). Non-standard baud rates up to 1 Mbaud can be selected by using different input frequencies (up to 16 MHz) and/or different Prescaler and Divisor Select ratios. The baud rate generator provides a clock which is 16 times the desired baud rate. For example, in order to operate at a 1 Mbaud data rate a 16 MHz crystal, a Prescale rate of ÷1, and a Divisor Select rate of "external" would be used to provide a 16 MHz clock as the output of the Baud Rate Generator to the Transmitter and Receiver Circuits.

BRSR

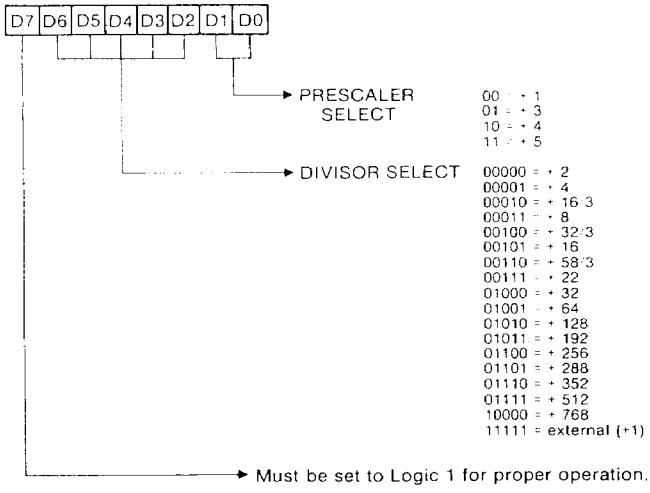


FIGURE 2

BAUD RATE	DIVISOR	BAUD RATE	DIVISOR
38.4K	external	1200	32
19.2	2	600	64
9600	4	300	128
7200	16/3	200	192
4800	8	150	256
3600	32/3	134.5*	288
2400	16	110*	352
2000*	58/3	75	512
1800	22	50	768

TABLE 2

Note: These baud rates are based upon the following input frequency/Prescale divisor combinations.
1.8432 MHz and Prescale = ÷3
2.4576 MHz and Prescale = ÷4
3.072 MHz and Prescale = ÷5

*All baud rates are exact except for:

BAUD RATE	ACTUAL	PERCENT ERROR
2000	1986.2	0.69%
134.5	133.33	0.87%
110	109.71	0.26%

MODEM CONTROL REGISTER (MCR)

The MCR is a general purpose control register which can be written to and read from. The $\overline{RTS}$ output is directly controlled by its associated bit in this register. Note that a logic one asserts a true logic level (low) at these output pins. The Operating Mode bits configure the SP into one of four possible modes. "Normal" configures the SP for normal full or half duplex communications. "Transmit Break" enables the transmitter to only transmit break characters (Start, Data and Stop bits all are logic zero). The Echo Mode causes any data that is received on the SDI input pin to be re-transmitted on the SD0 output pin. Note that this ouput is a buffered version of the data seen on the SDI input and is not a re-synchronized output. The Loop Test Mode internally routes transmitted data to the receiver circuitry for the purpose of self test. The transmit data is disabled from the SD0 output pin. The Receiver Enable bit gates off the input to the receiver circuitry when in the false state. Bit D7 must always be written to with a logic zero to insure correct SP operation.

MCR

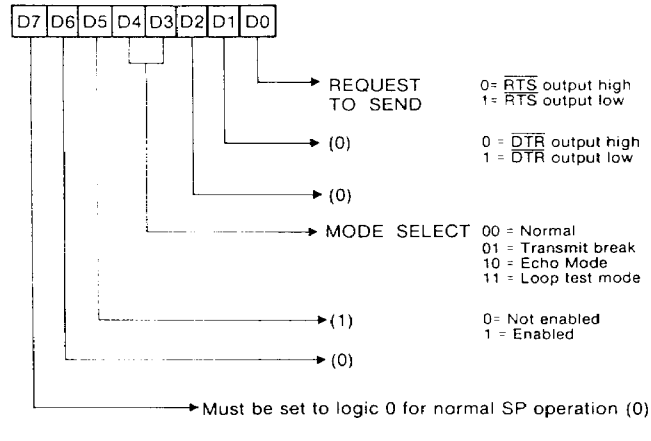
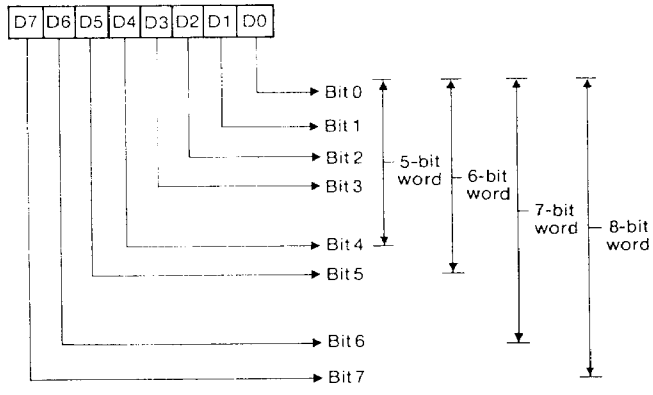


FIGURE 3

RECEIVER BUFFER REGISTER (RBR)

The receiver circuitry in the SP is programmable for 5, 6, 7 or 8 data bits per character. For words of less than 8 bits, the data is right justified to the LSB (D0). Bit D0 of a data word is always the first data bit received. The unused bits in a less than 8 bit word, at the parallel interface, are set to 0 by the SP. Received data at the SDI input pin is shifted into the Receiver Register by an internal 1X clock which has been synchronized to the incoming data based on the position of the start bit. When a complete character has been shifted into the Receiver Register, the assembled data bits are parallel loaded into the Receiver Buffer Register, and the DR flag in the USR register is set. This double buffering of the received data permits continuous reception of data without losing any of the received data. While the Receiver Register is shifting a new character into the SP, the Receiver Buffer Register is holding a previously received character for the system CPU to read. Failure to read the data in the RBR before complete reception of the next character can result in the loss of the data in the Receiver Register.

RBR



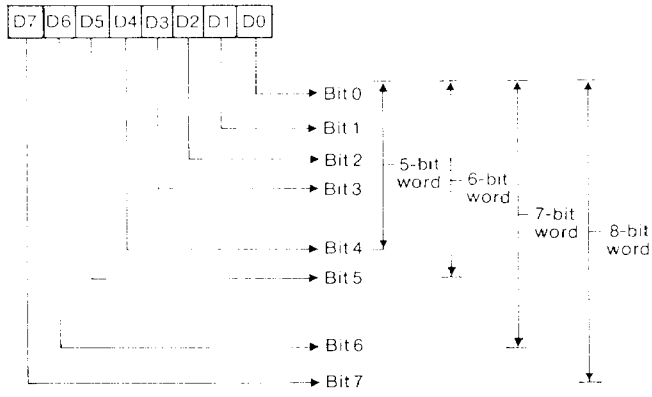
Note: The LSB, Bit 0 is the first serial data bit received.

FIGURE 4

TRANSMITTER BUFFER REGISTER (TBR)

The Transmitter Buffer Register (TBR) accepts parallel data from the microprocessor data bus (D0-D7) and holds it until the Transmitter Register is empty and ready to accept a new character for transmission. The transmitter always has the same word length and number of stop bits as the receiver. For words of less than 8 bits the unused bits at the microprocessor data bus are ignored by the transmitter. Bit 0, which corresponds to D0 at the data bus, is always the first serial data bit transmitted. Provision is made for the transmitter parity to be the same or different from the receiver. The TBRE and flag USR register reflect the status of the TBR.

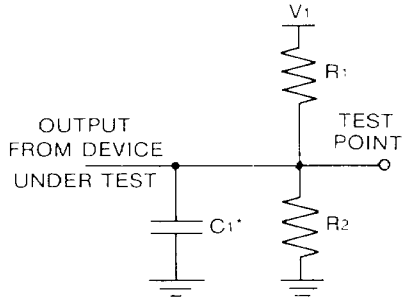
TBR



Note: The LSB, Bit 0 is the first serial data bit transmitted.

FIGURE 5

AC TEST CIRCUIT



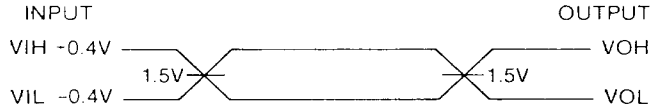
*Includes stray and jig capacitance

TEST CONDITION DEFINITION TABLE

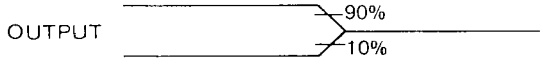
TEST CONDITION	V1	R1	R2	C1
1. Propagation Delay	1.7V	520	∞	100pF
2. Disable Delay	Vcc	5K	5K	50pF

AC TESTING OUTPUT WAVEFORM

PROPAGATION DELAY



ENABLE/DISABLE DELAY



AC Testing: all input signals must switch between VIL -0.4V and VIH +0.4V. TR and TF must be less than or equal to 15ns.

REGISTER BIT ASSIGNMENT SUMMARY

REGISTER NAME	MNEMONIC	LSB 0	1	2	3	4	5	6	MSB 7
Receiver Buffer	RBR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Transmitter Buffer	TBR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
UART Status	USR						$\overline{CTS}$	Transmitter Buffer Reg. empty (TBRE)	Data Ready (DR)
UART Control	UCR	Stop Bit Select	0	1	1	Word Length 0	Word Length 1	0	0
Modem Control	MCR	Request To Send (RTS)	0	0	Mode Select 0	Mode Select 1	1	0	0
Baud Rate Select	BRSR	Prescaler Select 0	Prescaler Select 1	Divisor Select 0	Divisor Select 1	Divisor Select 2	Divisor Select 3	Divisor Select 4	1

*Reserved for future use. Always set to zero (0) to maintain future software compatibility.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage: +8.0 Volts
Operating Voltage Range: +4V to +7V
Input Voltage Applied: GND -5V to +6.5V
Output Voltage Applied: GND -0.5V to V_{CC} +0.5V
Storage Temperature Range: -65°C to +250°C
Operating Temperature Range: -55°C to +200°C
Maximum Power Dissipation: 1 Watt
Serial Ports Input: ±10 Volts
Serial Ports Output: +5V, 0V
Parallel Ports Input: +5V, 0V
Parallel Ports Output: +5V, 0V

CAUTION: Stresses above those listed in the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC CHARACTERISTICS

V_{CC} = 5.0V ±10%; T_A = -55°C to +200°C

SYMBOL	PARAMETER	MIN	TYP	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0	—	Volts	
VIL	Logical Zero Input Voltage	—	0.8	Volts	
VTH	Schmidt Trigger Logical One Input Voltage	V_{CC} -0.5	—	Volts	Reset Input
VTL	Schmidt Trigger Logical One Input Voltage	—	GND +0.5	Volts	Reset Input
VIH (CLK)	Logical One Clock Voltage	V_{CC} -0.5	—	Volts	External Clock
VIL (CLK)	Logical Zero Clock Voltage	—	GND +0.5	Volts	External Clock
VOH	Output High Voltage	3.0 V_{CC} -0.4	—	Volts	IOH = -2.5mA IOH = -400μA
VOL	Output Low Voltage	—	0.4	Volts	IOL = +2.5mA
IIL	Input Leakage Current	-1.0	+1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
IOL	Output Leakage Current	-10.0	+10.0	μA	$0V \leq V_{IN} \leq V_{CC}$
ICCOP*	Operating Power Supply Current	—	40	mA	External Clock F = 921.6 KHz V_{CC} = 5.5 Volts V_{IN} = V_{CC} or GND Outputs Open

*Guaranteed and sampled, but not 100% tested.

CAPACITANCE

$T_A = 25°C$; V_{CC} = GND = 0V; V_{IN} = +5V or GND

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
C_{IN}*	Input Capacitance	—	10	pF	FREQ = 1 MHz Unmeasured returned to GND
C_{OUT}*	Ouput Capacitance	—	15	pF	
$C_{I/O}$*	I/O Capacitance	—	20	pF	

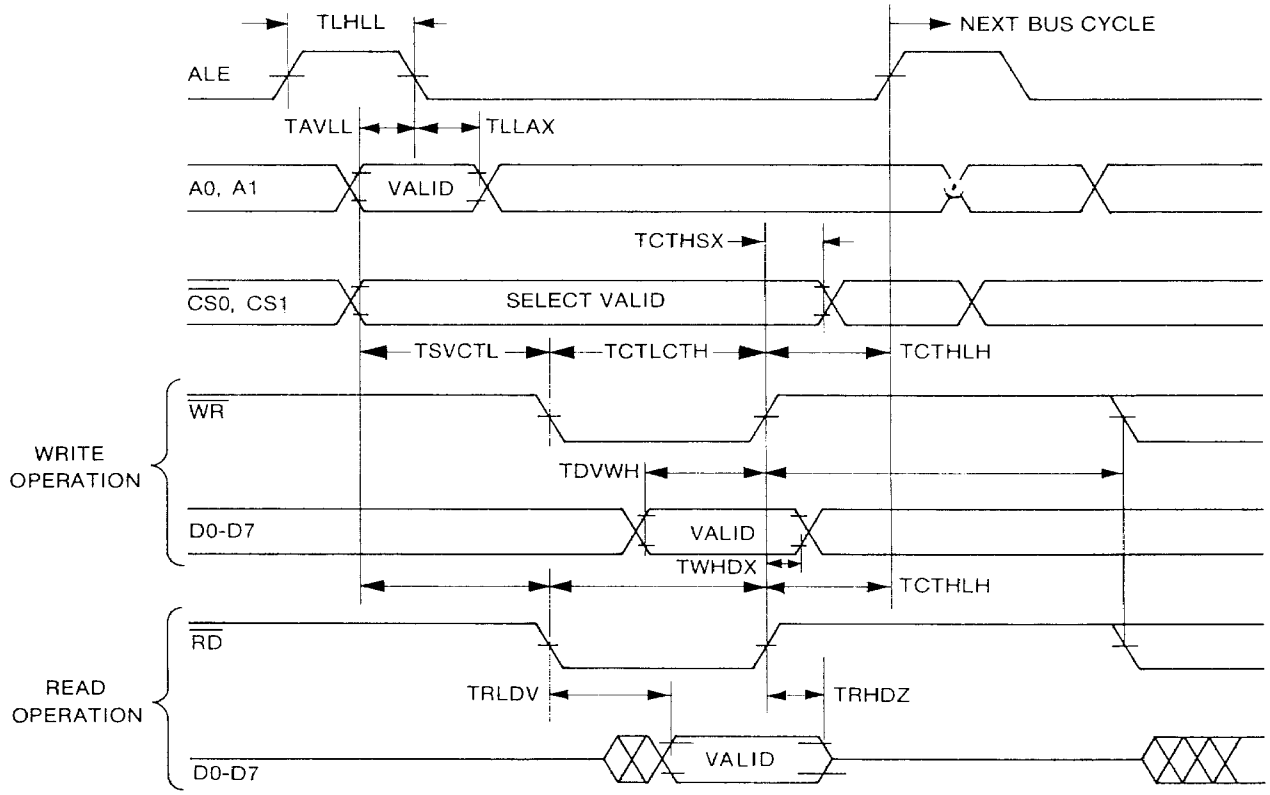
*Guaranteed and sampled, but not 100% tested.

AC CHARACTERISTICS—TIMING REQUIREMENTS

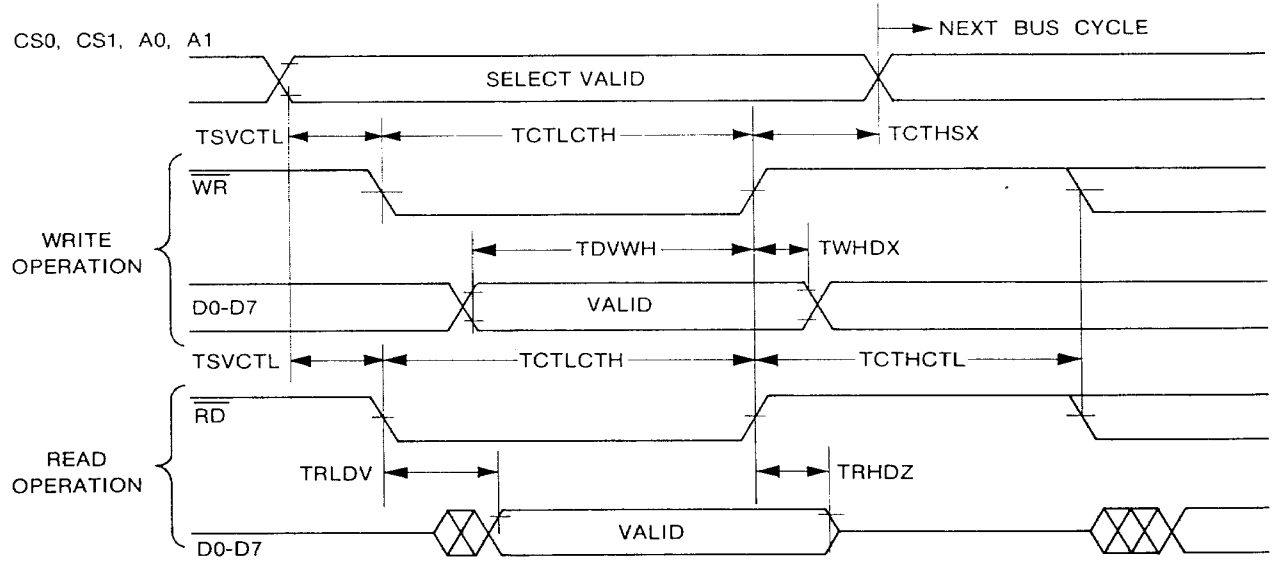
V_{CC} = +5V ±10%; GND = 0V; T_A = -55°C to +200°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TLHLL	ALE Pulse Width	50	—	ns	
TAVLL	Address Setup	20	—	ns	
TLLAX	Address Hold	20	—	ns	
TSVCTL	Select Setup to Control leading edge	30	—	ns	
TCTHSX	Select Hold from Control Trailing Edge	50	—	ns	
TCTLCTH	Control Pulse Width	150	—	ns	Control Consist of $\overline{RD}$ or $\overline{WR}$
TCTHCTL	Control Disable to Control Enable	100	—	ns	
TRLDV	Read low to Data Valid	—	120	ns	1
TRHDZ	Read Disable	0	60	ns	2
TCTHLH	Control Inactive to ALE High	20	—	ns	
TDVWH	Data Setup Time	50	—	ns	
TWHDX	Data Hold Time	20	—	ns	
FC	Clock Frequency	0	16	MHz	TCHCL + TCLCH must be ≥62.5ns
TCHCL	Clock High Time	25	—	ns	
TCLCH	Clock Low Time	25	—	ns	
TR/TF	Clock Input Rise/Fall Time (10% - 90%) (External Clock)	—	tx	ns	tx 1/(6FC) 05 50ns whichever is smaller
TFCO	Clock Output Fall Time	—	15	ns	C1 = 50 pF
TRCO	Clock Output Rise Time	—	15	ns	C1 = 50 pF

TIMING DIAGRAMS



MULTIPLEXED BUS OPERATION



DEMULTIPLEXED BUS OPERATION (ALE)

DPDS PARALLEL PORT (PP)

OPERATIONAL DESCRIPTION

When the reset input goes "high", all ports will be set to the input mode with all 16 port lines held at a logic "one" level by internal bus hold devices. After the reset is removed, the PP can remain in the input mode with no additional initialization required. This eliminates the need for pull-up or pull-down resistors in all CMOS designs. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single PP to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance: Group B can be programmed to monitor simple switch closings or display computational results. Group A could be programmed to monitor a keyboard or tape reader on an interrupt-driven basis.

	CONTROL WORD	PORT A	PORT B
89H	1000 1001	Output	Output
8BH	1000 1011	Output	Input
99H	1001 1001	Input	Output
9BH	1001 1011	Input	Input

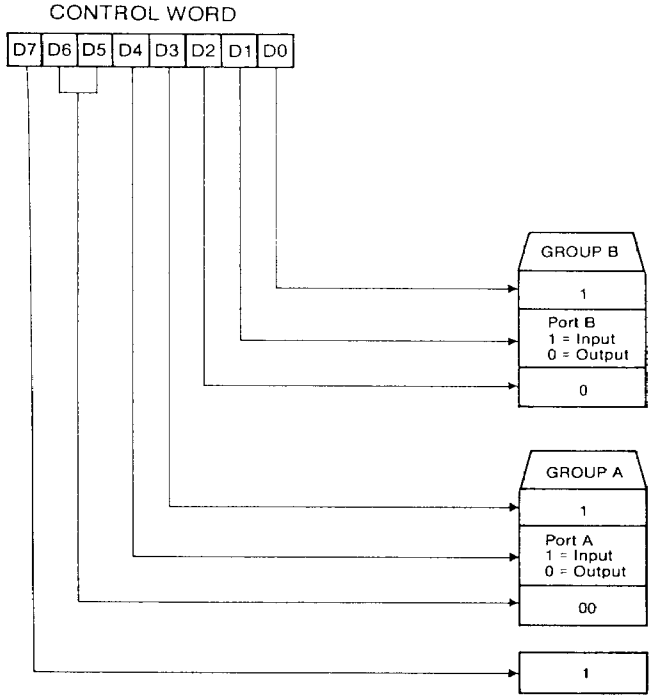


FIGURE 6

FUNCTIONAL DESCRIPTION

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the PP to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

A1	A0	RD	WR	INPUT OPERATION (READ)
0	0	0	1	Port A → Data Bus
0	1	0	1	Port B → Data Bus
1	1	0	1	Control Word → Data Bus
				OUTPUT OPERATION (WRITE)
0	0	1	0	Data Bus → Port A
0	1	1	0	Data Bus → Port B
1	1	1	0	Data Bus → Control
				DISABLE FUNCTION
X	X	1	1	Data Bus → 3-State

RESET

Reset. A "high" on this input clears the control register and all ports (A, B) are set to the input mode. Internal "bus hold" devices will hold the I/O port inputs to a logic "1" state with a maximum hold current of 300 μA.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the PP. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the PP.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A — Port A
Control Group B — Port B

The control word register can be both written and read as shown in the "Basic Operation" table. Figure 4 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic "1", as this implies control word mode information.

Port A, and Port B Controls

The DPDS contains two 8-bit ports (A and B). Both can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the DPDS.

Port A One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus-hold devices are present on Port A.

Port B One 8-bit input/output latch/buffer and one 8-bit data input buffer.

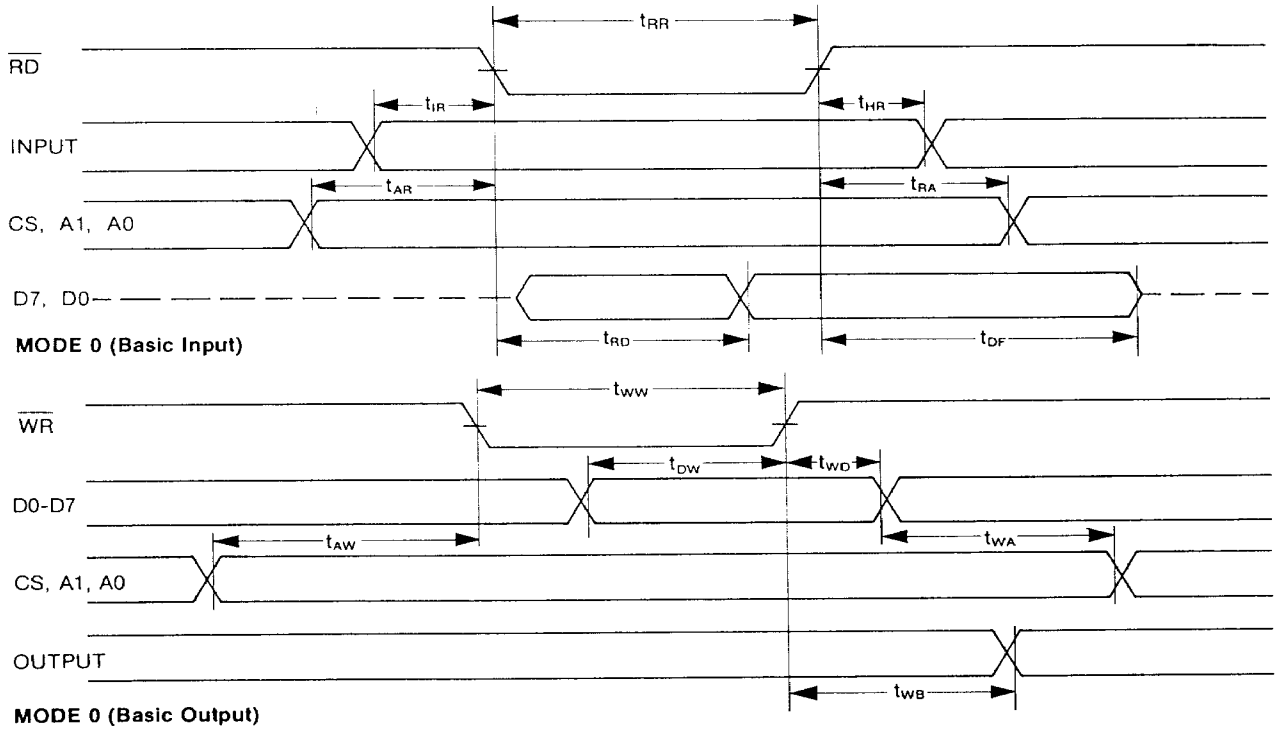
OPERATING MODE

This functional configuration provides simple input and output operations for each of the two ports. No handshaking is required, data is simply written to or read from a specific port.

Basic Functional Definitions.

- Two 8-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched
- Different Input/Output configurations possible

WAVEFORMS



MODE 0 (Basic Input)

MODE 0 (Basic Output)

AC CHARACTERISTICS

V_{CC} = 5V ±10%, GND = 0V; T_A = 0°C to +70°C (C82C55A)
V_{CC} = 5V ±10%, GND = 0V; T_A = -40°C to +85°C (I82C55A)
V_{CC} = 5V ±10%, GND = 0V; T_A = -55°C to +125°C (M82C55A)

BUS PARAMETERS READ SYMBOL	PARAMETER	PARALLEL PORT MIN	MAX	UNITS	TEST CONDITION
tAR	Address Stable Before READ	0	—	ns	
tRA	Address Stable After READ	0	—	ns	
tRR	READ Pulse Width	150	—	ns	
tRD	Data Valid From READ	—	100	ns	1
tDF	Date Float After READ	10	75	ns	2
tRV	Time Between READs and/or WRITEs	300	—	ns	
WRITE SYMBOL	**PARAMETER**	**MIN**	**MAX**	**UNITS**	**TEST CONDITION**
tAW	Address Stable Before WRITE	0	—	ns	
tWA	Address Stable After WRITE	20	—	ns	Ports A & B
tWW	WRITE Pulse Width	100	—	ns	
tDW	Data Valid to WRITE High	100	—	ns	
tWD	Data Valid After WRITE High	30	—	ns	Ports A & B
OTHER TIMINGS SYMBOL	**PARAMETER**	**MIN**	**MAX**	**UNITS**	**TEST CONDITION**
tWB	WR = 1 to Output	—	350	ns	1
tIR	Peripheral Data Before RD	0	—	ns	
tHR	Peripheral Data After RD	0	—	ns	
tRES	Reset Pulse Width	500	—	ns	See note 1

DC ELECTRICAL CHARACTERISTICS

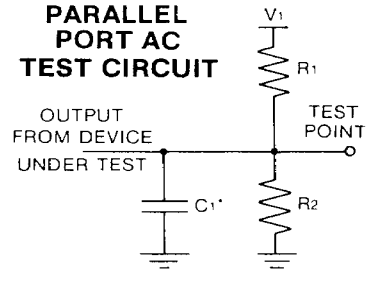
SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITION
IBHH	Bus Hold High Current	- 50	- 300	µA	VO = 3.0V; Ports A & B
IBHL	Bus Hold Low Current	+50	+300	µA	VO = 1.0V; Port A Only
IDAR	Darlington Drive Current	- 2.0	—	mA	Ports A & B Test Condition 3

Note 1: Period of initial Reset pulse after power-on must be at least 50µsec. Subsequent Reset pulses may be 500ns minimum.

TEST CONDITIONS DEFINITIONS TABLE

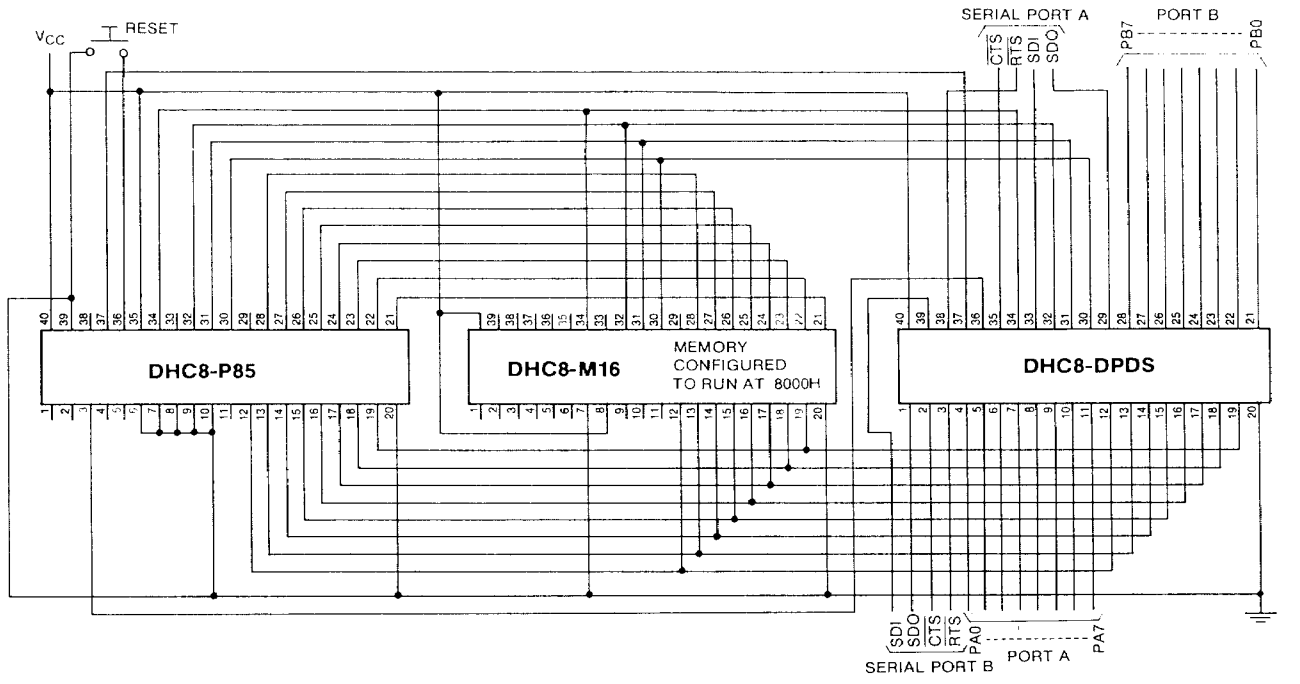
TEST CONDITION	V1	R1	R2	C1
1	1.7V	523Ω	OPEN	150 pF
2	5.0V	2KΩ	1.7KΩ	50 pF
3	1.5V	750Ω	OPEN	OPEN

PARALLEL PORT AC TEST CIRCUIT



*Includes stray and jig capacitance

Typical 20K System Hookup with Multi Port I/O



ORDERING INFORMATION

DHC8-DPDS-X

ADDRESS OFFSET	
2	2XH
4	4XH
6	6XH

ADDRESSING INFORMATION

	Serial Port 1	Serial Port 2
Data (TBR, RBR)	20H (X0H)	24H (X4H)
Control (UCR)	21H (X1H)	25H (X5H)
Handshake (MCR)	22H (X2H)	26H (X6H)
Baud Rate (BRSR)	23H (X3H)	27H (X7H)
Status (USR)	28H (X8H)	29H (X9H)

	Parallel Ports
Control Word	2CH (XCH)
Data Port A	2FH (XFH)
Data Port B	2EH (XEH)

Where X = Part Dash Number. i.e. DHC8-DPDS-**X**.

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