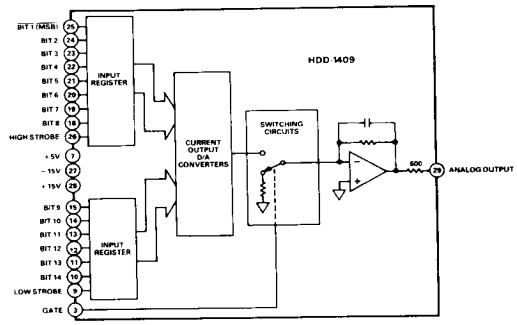
14-Bit, 200kHz Digital-to-Analog Converter

HDD-1409

FEATURES
- 14-Bit Resolution
- 200kHz Word Rates
- RZ Gated Output
- 32-Pin DIP

APPLICATIONS
- FDM/TDM Transmultiplexers
- Digital Signal Processing
- PCM Systems
- Digital Audio

HDD-1409 FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

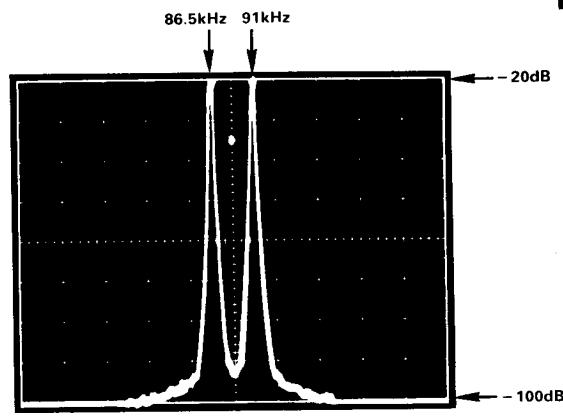
The HDD-1409KM D A converter is a voltage-output, 32-pin hybrid digital-to-analog converter complete with input registers, current-output D A, switching circuits, and output amplifier. The unit is capable of converting 14-bit digital inputs into gated analog output voltages at update rates from dc through 200kHz.

Monolithic ICs and hybrid microelectronic packaging have been combined in a grounded metal case hybrid which provides cost, space, and power savings for the system designer. The HDD-1409 is a complete solution for converting high-resolution digital data into "clean" analog voltages and accomplishes it with maximum power dissipation of only 600 milliwatts.

The HDD-1409 D A has been characterized with a companion A D converter, the HAS-1409KM, to emphasize the superior ac performance which makes the A/D – D/A combination especially attractive for use in Frequency Division Multiplex/Time Division Multiplex (FDM/TDM) transmultiplexer systems. But the design concepts and versatility which are incorporated into it also make the HDD-1409 useful in Pulse Code Modulation (PCM) and other digital signal processing applications.

The analog output voltage range is ± 5V; output impedance is 600 ohms, ideal for filter matching. The D/A output operates in a return-to-zero (RZ) mode, which provides deglitching and allows selecting the optimum duty cycle for FDM/TDM and PCM applications.

Small size, low power, and multiple functions in a single package make the HDD-1409 D/A converter attractive for a wide range of data processing uses.



10dB/div Vertical; 5kHz/div Horizontal
Spectrum analyzer shows extremely low intermodulation (IM) products of back-to-back HAS-1409 A/D and HDD-1408 D/A
(See Page 9–308 for details)

SPECIFICATIONS (typical @ + 25°C with nominal power supplies unless otherwise noted)

Model	Units	HDD-1409KM
RESOLUTION (FS = Full Scale)	Bits	14
LSB WEIGHT (FS = 10V; no load)	μV	610
ACCURACY (Linearity)	%FS	0.006
Differential Nonlinearity	LSB	1/2
Zero Offset (Initial)	mV	2
Monotonicity		Guaranteed
Gain Accuracy (−3dB)	dB	±0.01
TEMPERATURE COEFFICIENTS		
Linearity	ppm/°C	10
Gain	ppm/°C	20
Offset	ppm/°C	10
DYNAMIC CHARACTERISTICS[1]		
Settling Time to 1/2LSB		
±5V FS Change	μs	5
1LSB Change	μs	1
Slew Rate	V/μs	5
Update Rate	kHz, max	200
Harmonics[2]	dB	−100
Intermodulation Products[2]	dB	−100
Noise Power Ratio (NPR)[3]	dB	68
Idle Noise kHz[4]	dB	−104
Frequency Response[5]	dB	±0.2
DIGITAL DATA INPUTS		
Logic Compatability		TTL; CMOS
Logic Levels		
"0"	V	0 to +2.0
"1"	V	+3 to +5
Loading		
Each Bit	CMOS Load	5
STROBE (HIGH/LOW)	CMOS Load	5
GATE	TTL	1 Standard
Coding		Two's Complement (2SC)
		Offset Binary (OBN)
OUTPUT[6]		
Bipolar Voltage (No Load)	V	±5
Current	mA	4.2
Output Impedance	Ω (max %)	600 (±2)
Residual Glitch		(See Note 7)
POWER REQUIREMENTS		
+15V ±5%	mA	8
−15V ±5%	mA	20
+5V ±5%	mA	20
Power Supply Rejection Ratio	mV/V	1
Power Dissipation	W, max	0.6
TEMPERATURE RANGE[8]		
Operating	°C	−25 to +85
Storage	°C	−55 to +150
THERMAL RESISTANCE[9]		
Junction to Air, θja		
(Free Air)	°C/W	38
Junction to Case, θjc	°C/W	18
MEAN TIME BETWEEN FAILURES[10]		
(MTBF)	Hours	4×10^6
PACKAGE OPTION[11]		HY32C

NOTES
[1]AC performance characteristics are based on back-to-back performance with HAS-1409 D/A converter. All signals are referenced to rms value of full-scale sinewave.
[2]Harmonics and intermodulation products measured at 112kHz encode rate, with input frequencies of 86.5kHz and 91kHz at −21dB (see Figure 4).
[3]60kHz to 108kHz white noise bandwidth with slot frequency of 70kHz; and encode rate of 112kHz (see Figure 5).
[4]Idle noise measured at 112kHz encode rate, with input frequency of 84kHz at −41dB (see Figure 6).
[5]Indicates flatness of response over frequency range of 60kHz to 108kHz.
[6]Output is 25% duty cycle high; Return-to-Zero (RZ) between samples.
[7]Not deglitched; designed for gated operation.
[8]Case Temperature.
[9]Maximum junction temperature = 150°C.
[10]Calculated per MIL-HDBK 217; Ground; Benign; Case Temperature = 60°C.
[11]See Section 19 for package outline information.

Specifications subject to change without notice.

HDD-1409 PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	SIGNAL	17	DIGITAL GROUND
2	SIGNAL	18	BIT 8
3	GATE	19	BIT 7
4	DIGITAL GROUND	20	BIT 6
5	ANALOG GROUND	21	BIT 5
6	N/C	22	BIT 4
7	+5V	23	BIT 3
8	DIGITAL GROUND	24	BIT 2
9	LOW STROBE	25	BIT 1 (MSB)
10	BIT 14 (LSB)	26	HIGH STROBE
11	BIT 13	27	−15V
12	BIT 12	28	+15V
13	BIT 11	29	ANALOG OUTPUT
14	BIT 10	30	ANALOG GROUND
15	BIT 9	31	ANALOG GROUND
16	DIGITAL GROUND	32	ANALOG GROUND

NOTES:
WHEN USING WITH HAS-1409 A/D, CONNECT BIT 1 (MSB) OF A/D (PIN 22) to BIT 1 (MSB) OF HDD-1409 D/A (PIN 25).

TO USE HDD-1409 D/A AS STAND-ALONE DEVICE WITH OFFSET BINARY INPUT, APPLY BIT 1 DIGITAL INPUT SIGNAL TO SIGNAL (PIN 1) AND CONNECT SIGNAL (PIN 2) TO BIT 1 (MSB) (PIN 25).

TO LOAD 14-BIT DATA FULLY PARALLEL, CONNECT HIGH STROBE (PIN 26) AND LOW STROBE (PIN 9) TOGETHER EXTERNALLY.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

THEORY OF OPERATION

Refer to the block diagram of the HDD-1409 D/A converter.

When the HDD-1409 D/A converter is operated with its companion HAS-1409 A/D converter, the 3-state digital logic inputs supplied by the HAS-1409 are applied to internal input registers.

For full 14-bit parallel operation, HIGH STROBE and LOW STROBE are operated simultaneously from an external STROBE signal and cause the outputs of the registers to be applied to the internal current output D/A converter.

The output of the converter, in turn, is applied to the output amplifier through switching circuits controlled by an external GATE signal. The timing of this GATE signal establishes the percentage of duty cycle during which the analog output will be at the voltage level indicative of the value of the digital inputs. During the time the GATE signal is at a digital "0" level, the voltage output of the HDD-1409 will be at ground.

The glitch from the internal D/A converter subsides during that period of time the analog output is connected to ground and never appears as a discontinuity in its voltage level. In effect, this technique accomplishes "deglitching" of the HDD-1409 D/A converter output by gating the output to be available only after internal settling times have been completed.

APPLICATIONS/TESTING

The testing and calibration of the HDD-1409 D/A converter are done in a back-to-back hookup with its companion HAS-1409 A/D converter. See Figure 1.

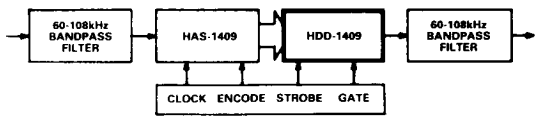


Figure 1. Basic Test Setup

The ac parameters of both converters have been optimized for operation at a word rate of 112kHz for reasons outlined in the detailed explanation of FDM/TDM Transmultiplexers included in the HAS-1409 A/D converter data sheet. This word rate is the one used in test and calibration of the units.

Analog signals in the frequency band of 60-108kHz are applied through a bandpass filter to the input of the HAS-1409 A/D converter. The output of the A/D is a digital representation of this signal and is applied to the HDD-1409 D/A converter as 3-state TTL-compatible digital inputs. After reconstruction, the analog output of the D/A is filtered through the same type of filter used ahead of the A/D and is applied to the test and measurement circuits.

CLOCK and $\overline{\text{ENCODE}}$ signals generated by the test setup are synchronized to one another and are timed for correct interaction with the STROBE and GATE signals applied to the HDD-1409.

The timing relationships among the digital inputs, STROBE, GATE, and analog output signals are shown in Figure 2.

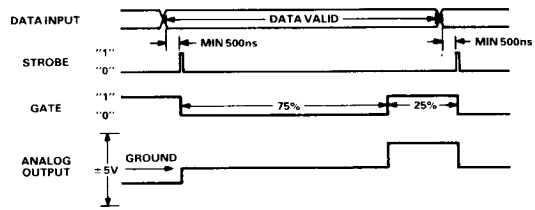


Figure 2. HAS-1409 Timing Diagram

The STROBE signal is shown as a single pulse for illustrative purposes to highlight that its positive-trigger leading edge establishes timing. In actual use, both LOW STROBE (pin 9) and HIGH STROBE (pin 26) signals are simultaneously applied to the HDD-1409 to latch the digital inputs into internal registers. This is easily accomplished through the simple expedient of connecting pins 9 and 26 together externally.

The GATE input shown in Figure 2 causes the analog output of the converter to be "on" for 25% of the duty cycle and "off" (connected to ground) for 75% of the duty cycle. This ratio makes the sin X/X compensation simpler when reconstructing

the digital inputs. If desired, the user could alter the timing of the GATE signal to allow the output to be "on" and/or "off" up to 50% of the duty cycle.

The type of testing which is done checks performance parameters for both the A/D and the D/A; as a result, it establishes the baseline performance for *both* units.

Refer to Figure 3 Intermodulation/Total Harmonic Distortion Test Circuit.

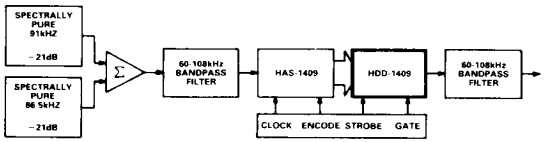


Figure 3. Intermodulation/Total Harmonic Distortion Test

To assure optimum performance in FDM/TDM transmultiplexer applications, the levels of harmonics and intermodulation (IM) products are both measured in the same way. The purpose of testing these parameters is to insure that "beat" frequencies which result from the interaction of two signals are far enough below those signals to avoid interfering with the carrier frequencies.

Spectrally pure sinewaves at frequencies of 91kHz and 86.5kHz are used because their interactions with one another will generate second and third-order harmonics which are easy to distinguish and measure. As in any sampling scheme, the generated frequencies are "folded" back into the passband of interest and their levels are a measure of converter performance.

Each test frequency is applied to a summation amplifier at a precise level 21dB below the rms value of a full-scale sinewave. After being digitized, reconstructed by the HDD-1409 D/A converter, and filtered, the amplitudes of the residual harmonics and IM products have typical levels of −100dB.

Refer to Figure 4 Noise Power Ratio Test Circuit.

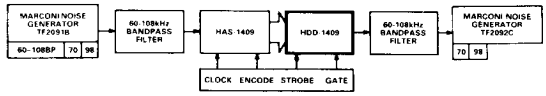


Figure 4. Noise Power Ratio Test Circuit

The measurement of noise power ratio (NPR) is a critical indicator of converter performance in telecommunications systems, and the test conditions must replicate the system environment to the maximum possible extent.

White noise in the frequency range of 60 to 108kHz is applied through the input filter, and the total power present in a narrow "slot" centered at 70kHz is computed. A bandstop filter 1kHz wide, also centered at 70kHz, is switched in and the total power still present in the "slot" is computed. The NPR is the ratio of these two readings and acceptable performance is typically 68dB.

Refer to Figure 5 Idle Noise Test Circuit.

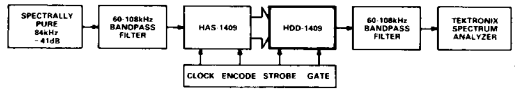


Figure 5. Idle Noise Test Circuit

As shown in Figure 5, a sinewave of 84kHz and good spectral purity is applied through the input filter to the A/D and D/A combination under test. As it is in the harmonics and IM distortion tests, the input level of the test signal is critical; for this measurement, it is at −41dB, referenced to the rms value of a full-scale sinewave.

The combination of input frequency and encode rate cancels all harmonics, leaving only the fundamental 84kHz frequency and the idle noise components. The specification for acceptable performance requires that these components typically be at −104dB when using a 1kHz-bandwidth filter.

FDM/TDM TRANSMULTIPLEXERS

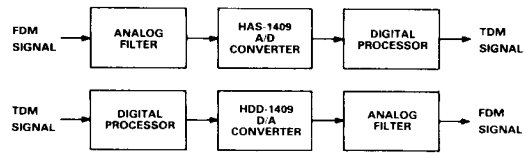
Two standard formats are used in telephony for multiplexing voice signals. The older of the two, frequency division multiplex (FDM), is used throughout the world for transmitting long distance telephone calls. In this scheme, voiceband signals are "stacked" into adjacent 4kHz channels in their assigned frequency domain by using single sideband (SSB) amplitude modulation.

In the newer time division multiplex, or TDM, each voice signal is digitized using pulse code modulation (PCM), at an 8kHz sample rate. As the name suggests, the resulting pulse streams are then interleaved in time and transmitted.

Digital toll switching offices, first installed in the United States in the latter part of the 1970s, continue to proliferate at a high rate. One of their major characteristics is that they switch signals exclusively in the TDM format within the office. But the need to operate also with the older FDM format means all incoming and outgoing signals must be converted to and from digital form.

The interface between the two standard signl multiplexing formats which is used to make this conversion is the FDM/TDM transmultiplexer system.

The application of digital signal processing (DSP) to the interface, as shown above, is extremely attractive since the frequency ranges of the signals which are involved make efficient use of available technology. In addition, the stringent interface specifications benefit from the precision which is inherent in a digital approach to the problem.



Digital FDM/TDM Translation

The analog filter shown in the upper portion of the diagram is used to remove undesirable out-of-band components from the FDM signal. The output of the filter is then applied to the HAS-1409 A/D converter whose output is a digital word stream. The individual channels within this stream are separated via a real-time processing algorithm in the block labeled Digital Processor. The resulting signal is now in the TDM format for switching and/or transmitting.

The lower portion of the diagram depicts the process of going from TDM to FDM, using the HDD-1409 D/A converter, in a procedure which is basically an inverse operation. The exception to that is the analog filter, which performs essentially the same function in both directions.

The reader is urged to consult the data sheet for the HAS-1409 A/D converter, which contains considerably more detail on the theory and application of FDM/TDM transmultiplexers.