Dual Voltage Video/Memory Clock Generator

Features

- Specified for dual voltage operation (V_{DD} = 3.3V or 5V) but operates continuously from 3.0V to 5.25V
- Power-down input for extended battery life in portable applications
- Guaranteed performance up to 110 MHz (at 3.3V) or 135 MHz (at 5V)
- Advanced PLL for low phase-jitter
- Low power CMOS device technology
- Excellent power supply rejection
- Integral Loop Filter components
- Mask-programmable frequencies
- Small footprint - 16-pin DIP or SOIC
- Generates 16 video clock frequencies derived from a 14.318 MHz system clock reference frequency
- Provision for external frequency input
- Video clock is selectable among the 16 internally generated clocks, one external clock, or the buffered crystal oscillator
- Internal clock remains locked when the external frequency input is selected
- On-chip generation of four memory clock frequencies
- Patented technique eliminates cross-interference between video and memory clocks
- Fast acquisition of selected frequencies, strobed or non-strobed

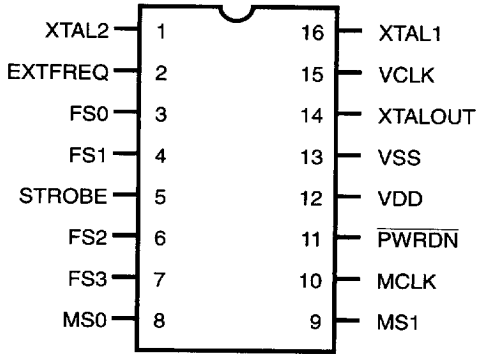
Description

The **ICS2496** has been specifically designed to serve the portable PC market with operation at either 3.3V or 5V with a comprehensive power-saving shut down mode.

The **ICS2496** Clock Generator is a dual phase-locked loop frequency synthesizer capable of generating 16 video frequencies and four memory clock frequencies for use with high performance video display systems. Utilizing CMOS technology to implement all linear, digital and memory functions, the **ICS2496** provides a low power, small footprint, low cost solution to the generation of video dot clocks. Provision is made via a single level custom mask to implement customer specific frequency sets. Phase-locked loop circuitry permits rapid glitch-free transitions between clock frequencies.

In addition to providing 16 clock rates, the **ICS2496** has provisions to multiplex an externally-generated signal source into the **VCLK** signal path. Internal phase-locked frequencies continue to remain locked at their preset values when this mode is selected. This feature permits instantaneous transition from an external frequency to an internally-generated frequency. Printed circuit board testing is simplified by the use of these modes, as an external clock generated by the ATE tester can be fed through, permitting synchronous testing of the entire system.

Pin Configuration



16-Pin DIP or SOIC
K-4, K-6

Notes:
1. ICS2496M(SOIC) pinout is identical to ICS2496N(DIP).

Circuit Function and Application

"Power-down"

The **ICS2496** has been optimized for use in battery operated portables. It can be placed in a power-down mode which drops its supply current requirement below 1 microamp. When placed in this mode, the digital inputs FS0-3, STROBE, MS0-1, and EXTFREQ may be either high or low or floating without causing an increase in the **ICS2496** supply current.

The PWRDN pin must be low (It has an internal pull-down.) in order to place the device in its low power state. The output pins (VCLK and MCLK) are driven high and XTALOUT is driven low by the **ICS2496** when it is in its low power state.

If a crystal is being used, nothing needs to be done to achieve low power. If XTAL1 is being driven by an external source, it may be driven low or high without a power penalty. If XTAL1 is at an intermediate voltage (V_{SS} +0.5V < V_{IN} < V_{DD} -0.5), there will be a small increase in supply current. If XTAL1 is driven at 14.318 MHz while the chip is in power-down, the **ICS2496** supply current will increase to approximately 1.2 mA.

The STROBE (pin 5) may be used to guard against inadvertent frequency changes during power-down/power-up sequences. By holding the STROBE low during power-down and power-up sequences, the **ICS2496** will retain the most recent video frequency selection.

Reference Oscillator and Crystal Selection

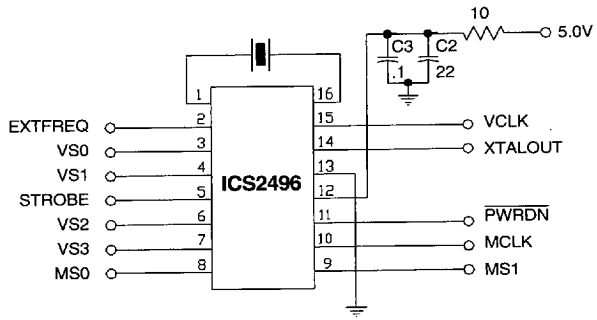
In cases where the on-chip crystal oscillator is used to generate the reference frequency, the accuracy of the crystal oscillation frequency will have a very small effect on output accuracy.

The external crystal and the on-chip circuit implement a Pierce oscillator. In a Pierce oscillator, the crystal is operated in its parallel-resonant (also called anti-resonant) mode. This means that its actual frequency of oscillation depends on the effective capacitance that appears across the terminals of the quartz crystal. Use of a crystal that is characterized for use in a series-resonant circuit is fine, although the actual oscillation frequency will be slightly higher than the value stamped on the crystal can (typically 0.025%-0.05% or so). Normally, this error is not significant in video graphics applications, which is why the **ICS2496** will typically derive its frequency reference from a series-resonant crystal connected between pins 1 and 16.

As the entire operation of the phase-locked loop depends on having a stable reference frequency, the crystal should be mounted as close as possible to the package. Avoid routing digital signals or the **ICS2496** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

Power Supply Conditioning

The **ICS2496** is a member of the second generation of dot clock products. By incorporating the loop filter on chip and upgrading the VCO, the ease of application has been substantially improved over earlier products. If a stable and noise-free power supply is available, no external components are required. However, in most applications it is judicious to decouple the power supply as shown in Figure 1.



NOTES: FS3-FS0, MS1-MS0, EXTFREQ, and STROBE inputs are all equipped with pull-ups and need not be tied high.
PWRDN input has an internal pull-down and must be driven or tied high for full device function.
Mount decoupling capacitors as close as possible to the device and connect device ground to the ground plane where available.
Mount crystal and its circuit traces away from switching digital lines and the VCLK, MCLK, and XTALOUT lines.

Figure 1

Layout Considerations

Utilizing the **ICS2496** in video graphics adapter cards or on PS2 motherboards is simple, but does require precautions in board layout if satisfactory jitter-free performance is to be realized. Care should be exercised in ensuring that components not related to the **ICS2496** do not share its ground. In applications utilizing a multi-layer board, V_{SS} should be connected directly to the ground plane.

Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate crystal should be connected between **XTAL1 (16)** and **XTAL2 (1)**. In IBM-compatible applications this will typically be a 14.31818 MHz crystal, but fundamental mode crystals between 10 MHz and 25 MHz have been tested. Maintain short lead lengths between the crystal and the **ICS2496**. In some applications, it may be desirable to utilize the bus clock. If the signal amplitude is equal to or greater than 3.5 volts, it may be connected directly to **XTAL1 (16)**. If the signal amplitude is less than 3.5 volts, connect the clock through a .047 microfarad capacitor to **XTAL1 (16)**, and keep the lead length of the capacitor to **XTAL1 (16)** to a minimum to reduce noise susceptibility. This input is internally biased at $V_{DD}/2$. Since TTL compatible clocks typically guarantee a V_{OH} of only 2.8V, capacitively coupling the input restores noise immunity. The **ICS2496** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of this signal is typically outside of the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. **XTAL2 (1)** must be left open in this configuration.

Buffered XTALOUT

In motherboard applications it may be desirable to have the **ICS2496** provide the bus clock for the rest of the system. This eliminates the need for an additional 14.31818 MHz crystal oscillator in the system, saving money as well as board space. Depending on the load, it may be judicious to buffer XTALOUT when using it to provide the system clock.

Output Circuit Considerations

As the dot clock is usually the highest frequency present in a video graphics system, consideration should be given to EMI. To minimize problems with meeting FCC EMI requirements, the trace which connects **VCLK** or **MCLK** and other components in the system should be kept as short as possible. The **ICS2496** outputs have been designed to minimize overshoot. In addition, it may be helpful to place a ferrite bead in these signal paths to limit the propagation of high order harmonics of this signal. A suitable device would be a Ferroxcube 56-590-65/4B or equivalent. This device should be placed physically close to the **ICS2496**. A 33 to 47 Ohm series resistor, sometimes called source termination, in this path may be necessary to reduce ringing and reflection of the signal and may thereby reduce phase-jitter as well as EMI.

External Frequency Sources

EXTFREQ on versions so equipped by the programming, is an input to a digital multiplexer. When this input is enabled by the FS0-3 selection, the signal driving pin 2 will appear at **VCLK (15)** instead of the PLL output. Internally, the PLL will remain in lock at the frequency selected by the ROM code.

The programming option also exists to output the crystal oscillator output on VCLK. In the case where XTAL1 is being driven by an external oscillator, then this frequency would appear on VCLK if so programmed.

Digital Inputs

FS0 (3), **FS1 (4)**, **FS2 (6)**, and **FS3 (7)**, are the TTL compatible frequency select inputs for the binary code corresponding to the frequency desired. **STROBE (5)**, when high, allows new data into the frequency select latches; and when low, prevents address changes per Figure 2. The internal power-on-clear signal will force an initial frequency code corresponding to an all-zeros input state. **MS0 (8)** and **MS1 (9)** are the corresponding memory select inputs and are not strobed.

Pin Descriptions

The following table provides the pin description for the 16-pin **ICS2496** packages:

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	XTAL2	OUT	Crystal interface
2	EXTFREQ	IN	External clock input (if so programmed)
3	FS0	IN	Control input for VCLK selection
4	FS1	IN	Control input for VCLK selection
5	STROBE	IN	Strobe for latching FS (0-3) (*High enable*)
6	FS2	IN	Control input for VCLK selection
7	FS3	IN	Control input for VCLK selection
8	MS0	IN	Select input for MCLK selection
9	MS1	IN	Select input for MCLK selection
10	MCLK	OUT	Memory Clock Output
11	$\overline{\text{PWRDN}}$	IN	Power-down Control (low for power-down)
12	VDD	-	Power
13	VSS	-	Ground
14	XTALOUT	OUT	Buffered Crystal Output
15	VCLK	OUT	Video Clock Output
16	XTAL1	IN	Reference input clock from system

Absolute Maximum Ratings

Ambient Temperature under bias	0 °C to 70 °C
Storage temperature	-40 °C to 125 °C
Voltage on all inputs and outputs with respect to VSS	0.3 to 7 Volts

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin.

Operating Temperature range	0 °C to 70 °C
Power supply voltage	3.0 to 5.25 Volts

DC Characteristics at 5 Volts V_{DD}

SYMBOL	PARAMETER		MIN	MAX	UNITS	CONDITIONS
V_{DD}	Operating Voltage Range		4.75	5.25	V	
V_{IL}	Input Low Voltage		V_{SS}	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage		2.0	V_{DD}	V	V_{DD} = 5V
I_{IH}	Input Leakage Current		-	10	µA	$V_{in} = V_{CC}$
V_{OL}	Output Low Voltage:	VCLK, MCLK	-	0.4	V	I_{OL} = 8.0 mA
		XTALOUT	-	0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage:	VCLK, MCLK	2.4	-	V	I_{OH} = 8.0 mA
		XTALOUT	2.4	-	V	I_{OH} = 4.0 mA
I_{DD}	Supply Current		-	30	mA	VDD = 5V
R_{UP}	Internal Pull-up Resistors		50	-	K ohms	V_{IN} = 0.0V
C_{in}	Input Pin Capacitance		-	8	pF	F_C = 1 MHz
C_{out}	Output Pin Capacitance		-	12	pF	F_C = 1 MHz
I_{PN}	Power-down Supply Current		-	1.0	µA	V_{DD}=3.3V
R_{DN}	Internal Pull-down Equivalent		20	-	K ohms	$V_{IN}=V_{DD}$=5V

DC Characteristics at 3.3 Volts V_{DD}

SYMBOL	PARAMETER		MIN	MAX	UNITS	CONDITIONS
V_{DD}	Operating Voltage Range		3.0	3.6	V	
V_{IL}	Input Low Voltage		V_{SS}	0.8	V	V_{DD} = 3.3V
V_{IH}	Input High Voltage		2.0	V_{DD}	V	V_{DD} = 3.3V
I_{IH}	Input Leakage Current		-	10	µA	$V_{in} = V_{DD}$
V_{OL}	Output Low Voltage:	VCLK, MCLK	-	0.4	V	I_{OL} = 3.0 mA
		XTALOUT	-	0.4	V	I_{OL} = 1.5 mA
V_{OH}	Output High Voltage:	VCLK, MCLK	2.4	-	V	I_{OH} = 3.0 mA
		XTALOUT	2.4	-	V	I_{OL} = 1.5 mA
I_{DD}	Supply Current		-	20	mA	V_{DD} = 3.3V
R_{UP}	Internal Pull-up Resistors		100	-	K ohms	V_{IN} = 0.0V
C_{in}	Input Pin Capacitance		-	8	pF	F_C = 1 MHz
C_{out}	Output Pin Capacitance		-	12	pF	F_C = 1 MHz
I_{PN}	Power-down Supply Current		-	1.0	µA	V_{DD} =3.3V
R_{DN}	Internal Pulled-down Equivalent		50	-	K ohms	$V_{IN}=V_{DD}$ =3.3V

AC Timing Characteristics

The following notes apply to all of the parameters presented in this section:

1. REFCLK = 14.318 MHz
2. $T_C = 1/F_C$
3. All units are in nanoseconds (ns).
4. Maximum jitter is within a range of 30 µs after triggering on a 400 MHz scope.
5. Rise and fall time is between 0.8 and 2.0 VDC unless otherwise stated.
6. Output pin loading = 15pF
7. Duty cycle is measured at $V_{DD}/2$ unless otherwise stated.

SYMBOL	PARAMETER	MIN	MAX	NOTES
	STROBE TIMING			
Tpw	Strobe Pulse Width	10	-	
Tsu	Setup Time Data to Strobe	10	-	
Thd	Hold Time Data to Strobe	2	-	
	MCLK and VCLK TIMINGS @ **5.0V**			
Tr	Rise Time	-	2	Duty Cycle 40% min. to
Tf	Fall Time	-	2	60% max.
-	Frequency Error		0.5	%
-	Maximum Frequency		135	MHz
-	Propagation Delay for Pass Through Frequency	-	20	ns
-	Output Enable to Tristate (into and out of) time		15	ns
	MCLK and VCLK TIMINGS @ **3.3V**			
Tr	Rise Time	-	3	Duty Cycle 40% min. to
Tf	Fall Time	-	3	60% max.
-	Frequency Error		.5	%
-	Maximum Frequency		110	MHz
-	Propagation Delay for Pass Through Frequency	-	30	ns
-	Output Enable to Tristate (into and out of) time		20	ns

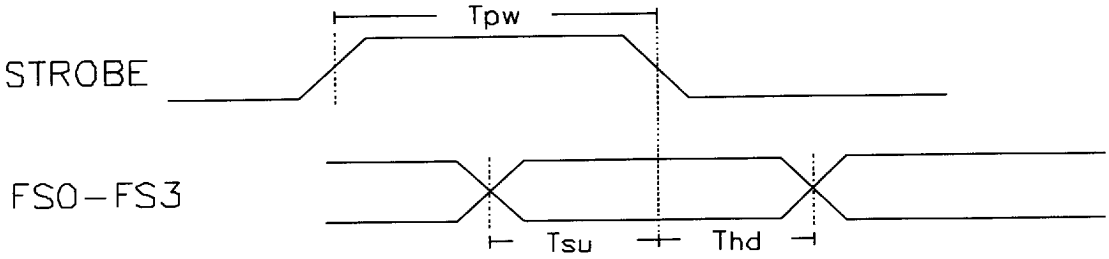


Figure 2

Ordering Information

ICS2496N-XXX or ICS2496M-XXX

Example:

ICS XXXX M -XXX

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  - N=DIP (Plastic)
  - M=SOIC
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  - ICS, AV=Standard Device; GSP=Genlock Device

ICS2496 Pattern Request Form

ICS produces a selection of standard pattern **ICS2496**'s pre-programmed for compatibility with many popular VGA chipsets. Custom patterns are also available, although a significant volume commitment and/or one-time mask charge will apply. Contact ICS sales for details.

ICS Part Number	ICS2496-452	ICS2496-454	ICS2496-456
Compatible VGA Chipsets	Cirrus Logic GD6410	Cirrus Logic GD6412	Motherboard Applications (CPU Clocks)
Video Clock Address(HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	XTAL	XTAL	20.000
1	65.000	65.000	24.000
2	EXTFREQ	EXTFREQ	32.000
3	36.000	36.000	40.000
4	25.175	25.175	50.000
5	28.322	28.322	66.667
6	24.000	24.000	80.000
7	40.000	40.000	100.000
8	44.900	44.900	54.000
9	50.350	50.350	70.000
A	16.257	16.257	90.000
B	32.514	32.514	110.000
C	56.644	56.444	25.000
D	20.000	20.000	33.333
E	41.539	41.539	40.000
F	80.000	80.000	50.000
Memory Clock Address(HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	32.900	32.900	16.000
1	35.600	35.600	24.000
2	43.900	43.900	50.000
3	49.100	39.900	66.667

Standard frequencies shown have been specified by and are supported by the respective VGA manufacturer.
All standard patterns shown above use 14.31818 MHz as the input reference frequency.
Order info: ICS2496M-XXX or ICS2496N-XXX (M= SOIC pkg., N= DIP pkg., XXX= Pattern number)