Contents

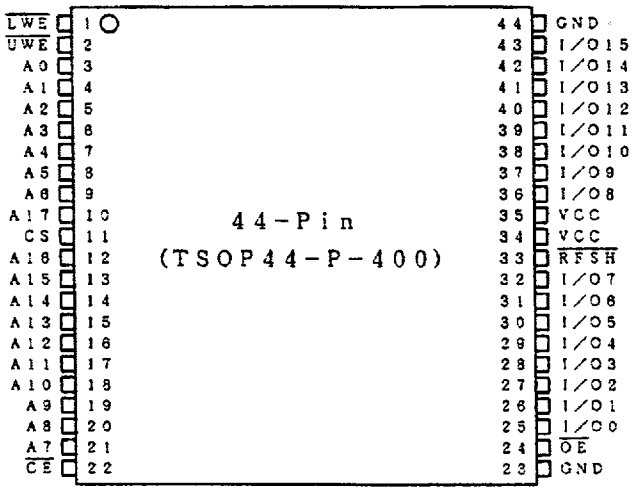
1. General

The LH5PV16256S-12LL is a 4M bit PSEUDO-SRAM with a 262,144-word by 16-bit configuration.

2. Features

- 262,144 x 16 bit organization
- Power supply: +3.0±0.15V
- Access time: 120ns (MAX.)
- Cycle time: 190ns (MIN.)
- Power consumption
  - Operating: 126mW (MAX.)
  - Standby: 94.5µW (MAX.)(CMOS input level)
  - Self-refresh: 220.5µW (MAX.)(CMOS input level)
- LVTTL compatible I/O
- Available for address refresh, auto-refresh and self-refresh modes
- 2,048 refresh cycles/32ms
- Address non-multiplex
- Available for byte write mode using $\overline{UWE}$ and $\overline{LWE}$ pins
- Package: 44-pin, TSOP Type II (TSOP44-P-400)
- Process: Silicon-gate CMOS
- Operating Temperature: 0 to 70 °C
- Not designed or rated as radiation hardened

3. Pin Configuration and Pin Description



TOP VIEW

Signal	Pin Name
A_7-A_{17}	Row address input
A_0-A_6	Column address input
$\overline{UWE}$, $\overline{LWE}$	Upper/Lower write enable input
$\overline{OE}$	Output enable input
$\overline{RFSH}$	Refresh input
$\overline{CE}$	Chip enable input
CS	Chip select input
I/O_8-I/O_{15}	Upper byte data input/output
I/O_0-I/O_7	Lower byte data input/output
Vcc	Power supply
GND	Ground

4. Truth Table

$\overline{CE}$	CS	$\overline{RFSH}$	$\overline{OE}$	$\overline{UWE}$	$\overline{LWE}$	Mode		I/O 0~7	I/O 8~15
L	H	H	L	H	H	Word Read		Output data	Output data
L	H	H	X	H	L	Write	Lower byte write	Input data	Don't care
				L	H		Upper byte write	Don't care	Input data
				L	L		Word write	Input data	Input data
				H	H		Invalid	High-Z	High-Z
H	X	L	X	X	X	Auto Refresh		High-Z	High-Z
L	L	H	X	X	X	CS Standby		High-Z	High-Z
H	X	H	X	X	X	Standby		High-Z	High-Z

H=High, L=Low, X=Don't Care

5. Requirements

<2$\overline{WE}$ control>

Please do not separate the $\overline{UWE}$ and $\overline{LWE}$ operation timing intentionally in the same write cycles. Each of the $\overline{UWE}$/$\overline{LWE}$ should satisfy the timing specifications individually.

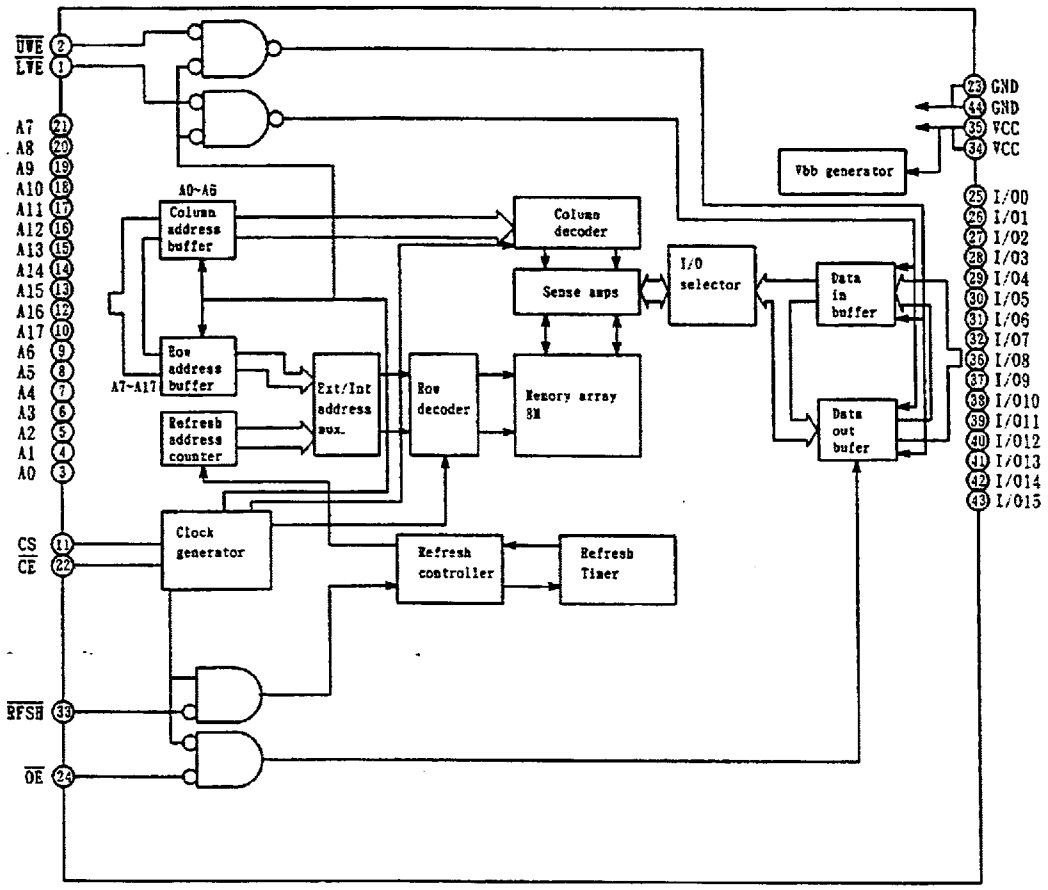
<Refresh after self-refresh or data retention mode>

- If address refresh is used during normal read/write cycles, the first address refresh must be executed within 15μs after self-refresh or data retention mode ends and the address refresh must be executed continuously for 2048 refresh cycles.
- If distributed auto-refresh is used during normal read/write cycles, the first auto-refresh must be executed within 15μs after self-refresh or data retention mode ends.
- If burst auto-refresh is used during normal read/write cycles, the first auto-refresh must be executed within 15μs after self-refresh or data retention mode ends, and the auto-refresh must be executed continuously for 2048 refresh cycles.

<Bypass capacitor for power supply noise reduction>

Because a PSRAM operates dynamically like a DRAM, it is recommended to put bypass capacitors between Vcc and GND to absorb power supply noise due to the peak current.

6. Block Diagram



7. Absolute Maximum Ratings

Parameter	symbol	Rating	Unit	Note
Supply voltage	V_T	-0.5 to +4.6	V	1
Output short circuit current	I_O	50	mA	
Power dissipation	P_D	600	mW	
Operating temperature	T_{opr}	0 to +70	℃	
Storage temperature	T_{stg}	-65 to +150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.

8. Recommended Operating Conditions

(Ta = 0 to 70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	Vcc	2.85	3.0	3.15	V	2
	GND	0	0	0	V	2
Input voltage	V_{IH}	2.0	-	Vcc+0.3	V	
	V_{IL}	-0.3	-	0.8	V	

Note 2: The supply voltage with all Vcc pins must be on the same level.
The supply voltage with all GND pins must be on the same level.

9. Pin Capacitances

(Ta = 0 to 70℃, f = 1MHz, Vcc = 3.0V ± 0.15V)

Parameter		Symbol	MIN.	MAX.	Unit
Input capacitance	A_0-A_{17}	C_{IN1}	-	8	pF
	$\overline{UWE}$,$\overline{LWE}$,$\overline{OE}$,$\overline{RFSH}$	C_{IN2}	-	8	pF
	$\overline{CE}$,CS	C_{IN3}	-	8	pF
Input/Output capacitance	I/O_0-I/O_{15}	C_{OUT1}	-	10	pF

10. DC Electrical Characteristics

(Ta = 0 to 70℃, Vcc = 3.0V ± 0.15V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit	Note
Operating current in normal operation	I_{CC1}	$t_{RC}=t_{RC}$(MIN.)	-	40	mA	3,4
Standby current	I_{CC2}	$\overline{CE}$,$\overline{RFSH}=V_{IH}$(MIN.)	-	1	mA	3
		$\overline{CE}$,$\overline{RFSH}=V_{CC}-0.2V$	-	30	μA	3
Self-refresh average current	I_{CC3}	$\overline{CE}=V_{IH}$(MIN.), $\overline{RFSH}=V_{IL}$(MAX.)	-	1	mA	3
		$\overline{CE}=V_{CC}-0.2V$, $\overline{RFSH}=0.2V$	-	70	μA	3
Input leakage current	I_{LI}	$0V\leq V_{IN}\leq 6.5V$, 0V on all other pins	-10	10	μA	
Output leakage current	I_{LO}	$0V\leq V_{OUT}\leq Vcc+0.3V$, Input/output pins in High-Z state	-10	10	μA	
Output High voltage	V_{OH}	$I_{OUT}=-1mA$	2.4	-	V	
		$I_{OUT}=-100\mu A$	$V_{CC}-0.2$	-		
Output Low voltage	V_{OL}	$I_{OUT}=1mA$	-	0.4	V	
		$I_{OUT}=100\mu A$	-	0.2		
Data retention voltage	V_R		2.2	3.15	V	

Note 3: The input/output pins are in high impedance state.

Note 4: I_{CC1} depends on the cycle time.

11. AC Electrical Characteristics (Note.5,6,11) (Ta= 0 to 70℃, Vcc= 3.0V ± 0.15V)

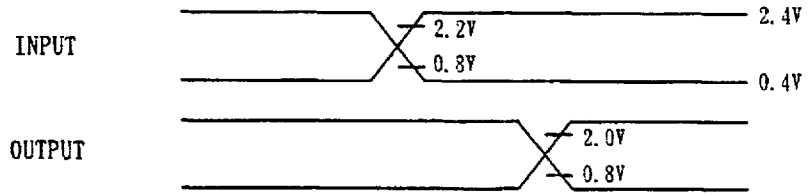
Parameter	Symbol	MIN.	MAX.	Unit	Note
Random read, write cycle time	t_{RC}	190	-	ns	
Random read modify write cycle time	t_{RMW}	250	-	ns	
$\overline{CE}$ pulse width	t_{CE}	120	10,000	ns	
$\overline{CE}$ precharge time	t_{P}	60	-	ns	
Address setup time	t_{AS}	0	-	ns	7
Row address hold time from $\overline{CE}$	t_{RAH}	30	-	ns	7
Column address hold time from $\overline{CE}$	t_{CAH}	120	-	ns	
CS setup time from $\overline{CE}$	t_{CSS}	0	-	ns	
CS hold time from $\overline{CE}$	t_{CSH}	30	-	ns	
Read command setup time	t_{RCS}	0	-	ns	15
Read command hold time	t_{RCH}	0	-	ns	13
$\overline{CE}$ Access time	t_{CEA}	-	120	ns	8
$\overline{OE}$ Access time	t_{OEA}	-	60	ns	8
$\overline{CE}$ to output in Low-Z	t_{CLZ}	20	-	ns	
$\overline{OE}$ to output in Low-Z	t_{OLZ}	0	-	ns	
Write disable to output in Low-Z	t_{WLZ}	0	-	ns	15
Chip disable to output in High-Z	t_{CHZ}	0	30	ns	
Output disable to output in High-Z	t_{OHZ}	0	30	ns	
$\overline{WE}$ to output in High-Z	t_{WHZ}	0	30	ns	13,17
Write command pulse width	t_{WCP}	35	-	ns	17
Write command setup time	t_{WCS}	35	10,000	ns	14,17
Write command hold time	t_{WCH}	120	10,000	ns	16,17
Data setup time from write disable	t_{DSW}	30	-	ns	9,16,17
Data setup time from chip disable	t_{DSC}	30	-	ns	9
Data hold time from write disable	t_{DHW}	0	-	ns	9,15,17
Data hold time from chip disable	t_{DHC}	30	-	ns	9
Data hold time from column address	t_{OH}	0	-	ns	
Column address hold time from chip disable	t_{AHC}	20	-	ns	9
Column address hold time from write disable	t_{AHW}	0	-	ns	9,17

11. AC Electrical Characteristics (Continued) (Ta = 0 to 70℃, Vcc = 3.0V ± 0.15V)

Parameter	Symbol	MIN.	MAX.	Unit	Note
Transition time (rise and fall)	t_T	3	50	ns	
Output disable setup time	t_{ODS}	0	-	ns	
Output disable hold time	t_{ODH}	15	-	ns	
Refresh time interval (2048 cycles)	t_{REF}	-	32	ms	10
Auto refresh cycle time	t_{FC}	190	-	ns	10
Refresh delay time from $\overline{CE}$	t_{RFD}	90	-	ns	
Refresh pulse width (Auto refresh)	t_{FAP}	80	1,000	ns	12
Refresh precharge time (Auto refresh)	t_{FP}	40	-	ns	
$\overline{CE}$ delay time from refresh enable (Auto refresh)	t_{FCE}	190	-	ns	
Refresh pulse width (Self refresh)	t_{FAS}	8,000	-	ns	12
$\overline{CE}$ delay time from refresh precharge (Self refresh)	t_{FRS}	600	-	ns	
Vcc recovery time from data retention	t_R	5	-	ms	
Refresh set up time	t_{FS}	0	-	ns	
Refresh disable hold time	t_{RDH}	15	-	ns	
Chip disable delay time from $\overline{RFSH}$	t_{RDD}	15	-	ns	

Note 5: AC characteristics are measured at t_T=5ns.

Note 6: AC characteristics are measured at the following condition.



Note 7: Row address signals are latched in the memory at the falling edge of $\overline{CE}$.

Note 8: Measured with a load equivalent to 50pF.

Note 9: Input data is latched in the memory at the earlier rising edge of $\overline{CE}$ and $\overline{UWE}/\overline{LWE}$. One of {$t_{AHW}$, t_{DSW}, t_{DHW}} and {t_{AHC}, t_{DSC}, t_{DHC}} needs to be satisfied, and the other is "Don't care".

Note 10: Address refresh or auto refresh is needed to be executed 2048 times within 32ms.

Note 11: In order to initialize the internal circuits, an initial pause of 500μs with $\overline{CE}$=$\overline{RFSH}$=V_{IH} is required after power-up, and followed by at least 8 dummy cycles. When supply voltage falls down below the recommended supply voltage by temporally power-down, a waiting time is required at Vcc=0V for more than 400ms before power-up, and a pause of 500μs with $\overline{CE}$=$\overline{RFSH}$=V_{IH} and 8 dummy cycles are also necessary after power-up.

Note 12: Auto refresh and self refresh are defined by $\overline{RFSH}$ pulse width during $\overline{CE}$=V_{IH}. If $\overline{RFSH}$ pulse width is shorter than t_{FAP}(MAX.), the cycle is an auto refresh cycle and memory cells are refreshed by an internal counter. If $\overline{RFSH}$ pulse width is longer than t_{FAS}(MIN.), the cycle is a self refresh cycle and memory cells are refreshed by an internal clock generator automatically.

Note 13: t_{RCH} and t_{WHZ} are determined by the earlier falling edge of $\overline{UWE}$ and $\overline{LWE}$.

Note 14: t_{WCS} is determined by the later falling edge of $\overline{UWE}$ and $\overline{LWE}$.

Note 15: t_{RCS}, t_{WLZ} and t_{DHW} are determined by the later rising edge of $\overline{UWE}$ and $\overline{LWE}$.

Note 16: t_{WCH} and t_{DSW} are determined by the earlier rising edge of $\overline{UWE}$ and $\overline{LWE}$.

Note 17: t_{WHZ}, t_{WCP}, t_{WCS}, t_{WCH}, t_{DSW}, t_{DHW}, t_{WLZ} and t_{AHW} should be satisfied by both $\overline{UWE}$ and $\overline{LWE}$.

Note 18: The transition time of the supply voltage in data retention mode is less than 0.05V/ms.

Note 19: The width of data retention period is more than t_{FAS}(min.) like self-refresh cycle.

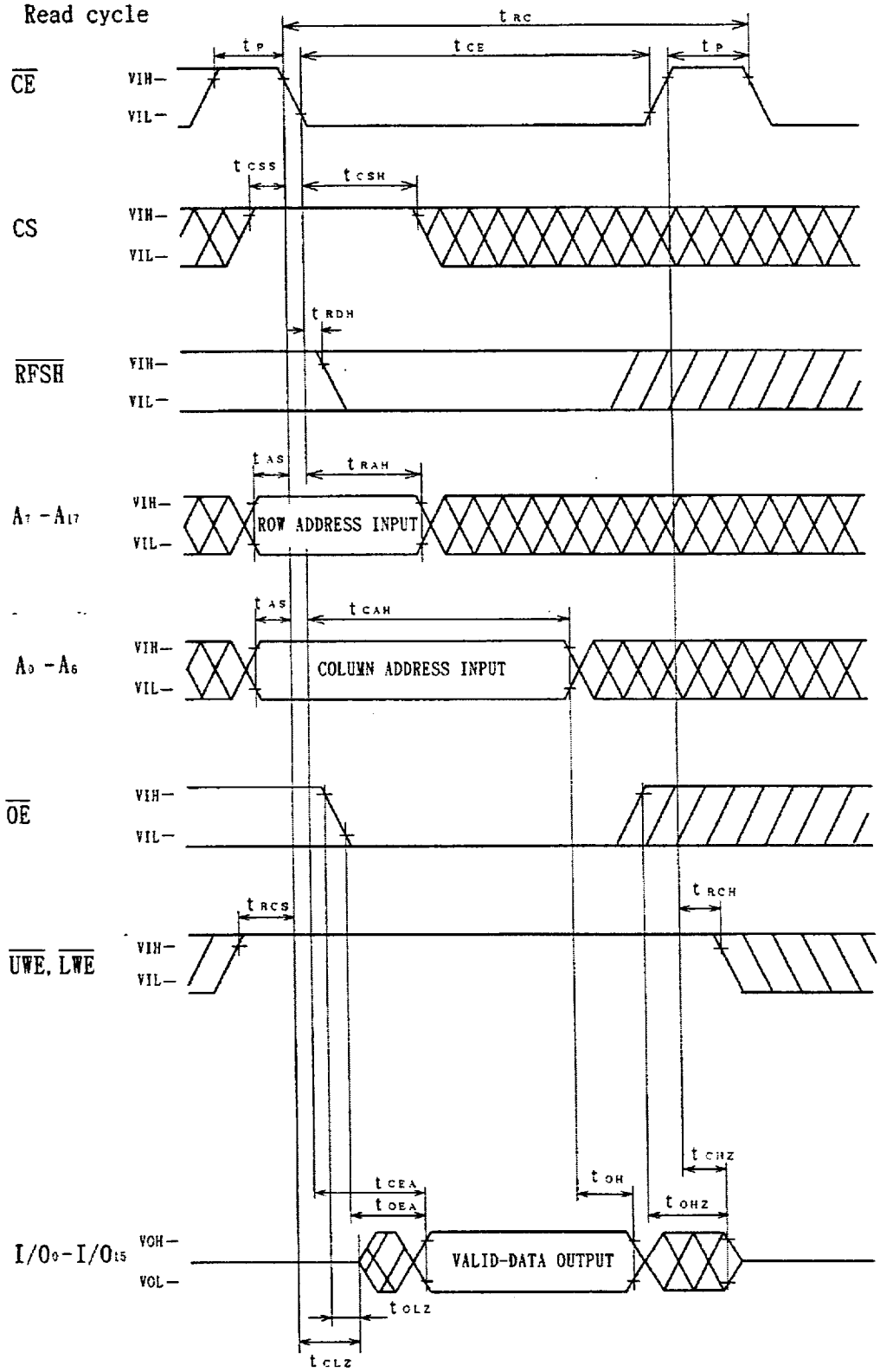
Note 20: All input pins are required to be higher than -0.3V.

Note 21: $\overline{RFSH}$ must be lower than 0.2V during the data retention period.

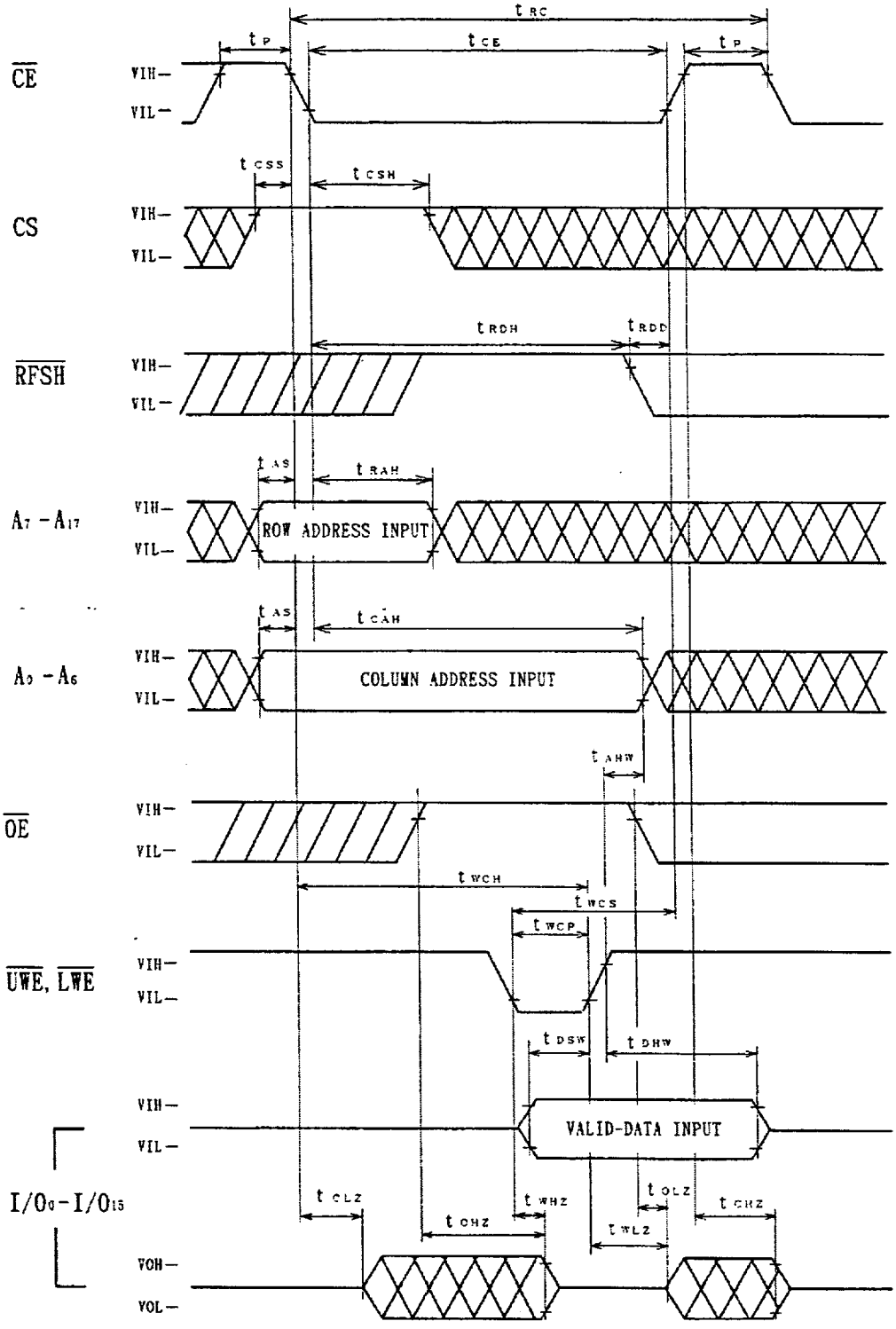
Note 22: $\overline{CE}$ and CS must be higher than Vcc-0.2V during the data retention period.

12. Timing Charts

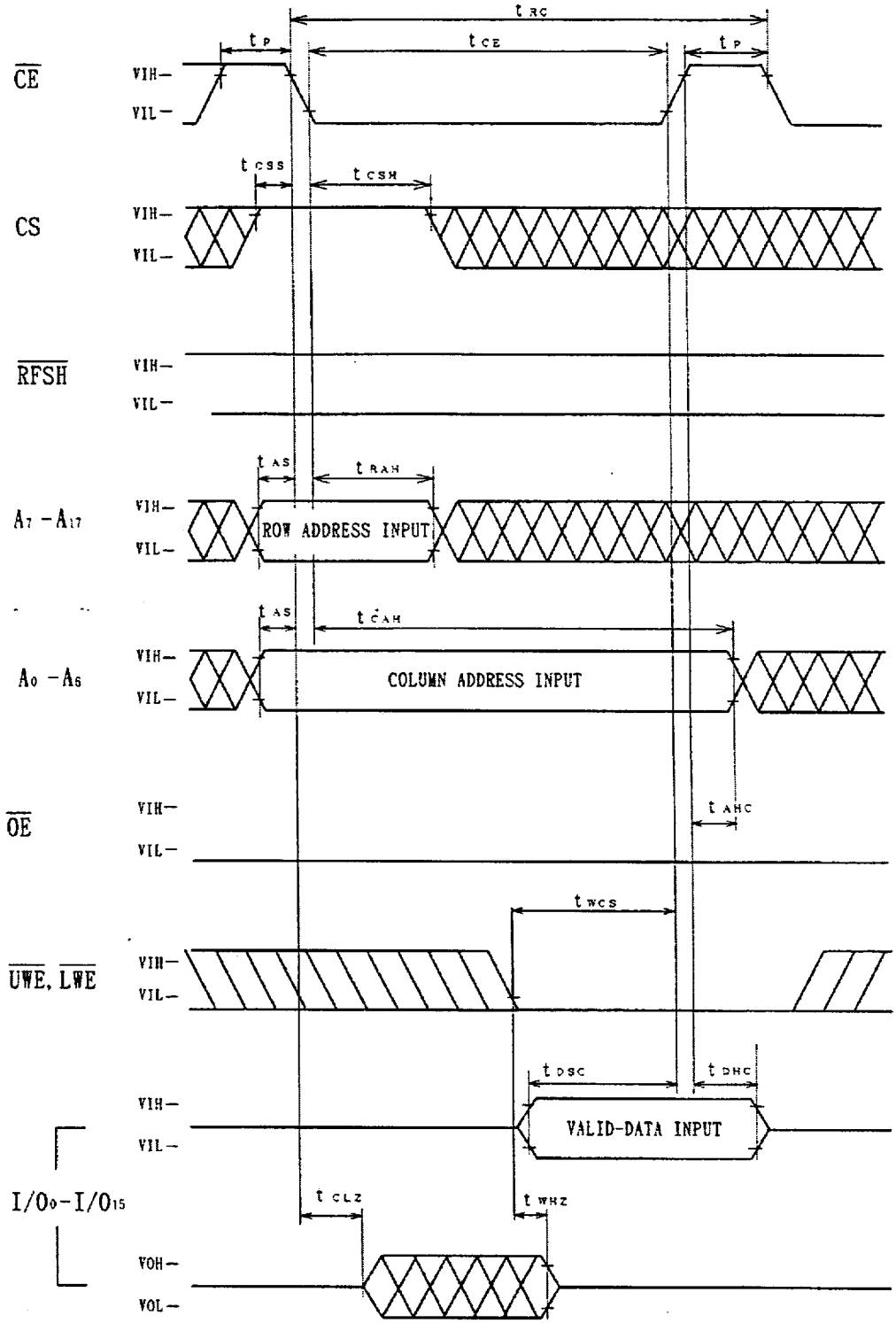
Read cycle



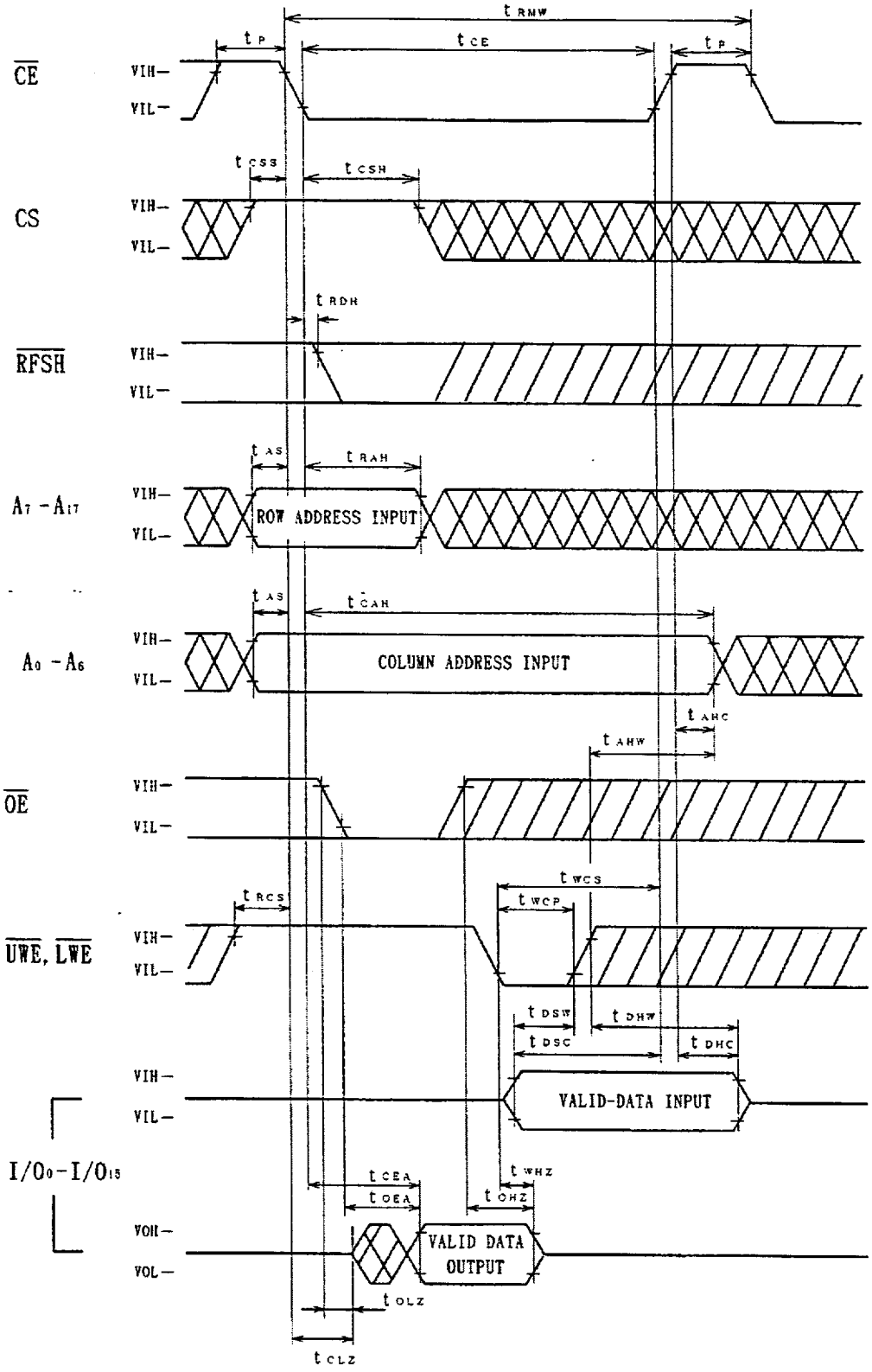
Write cycle(1) ($\overline{OE}$ Clock)



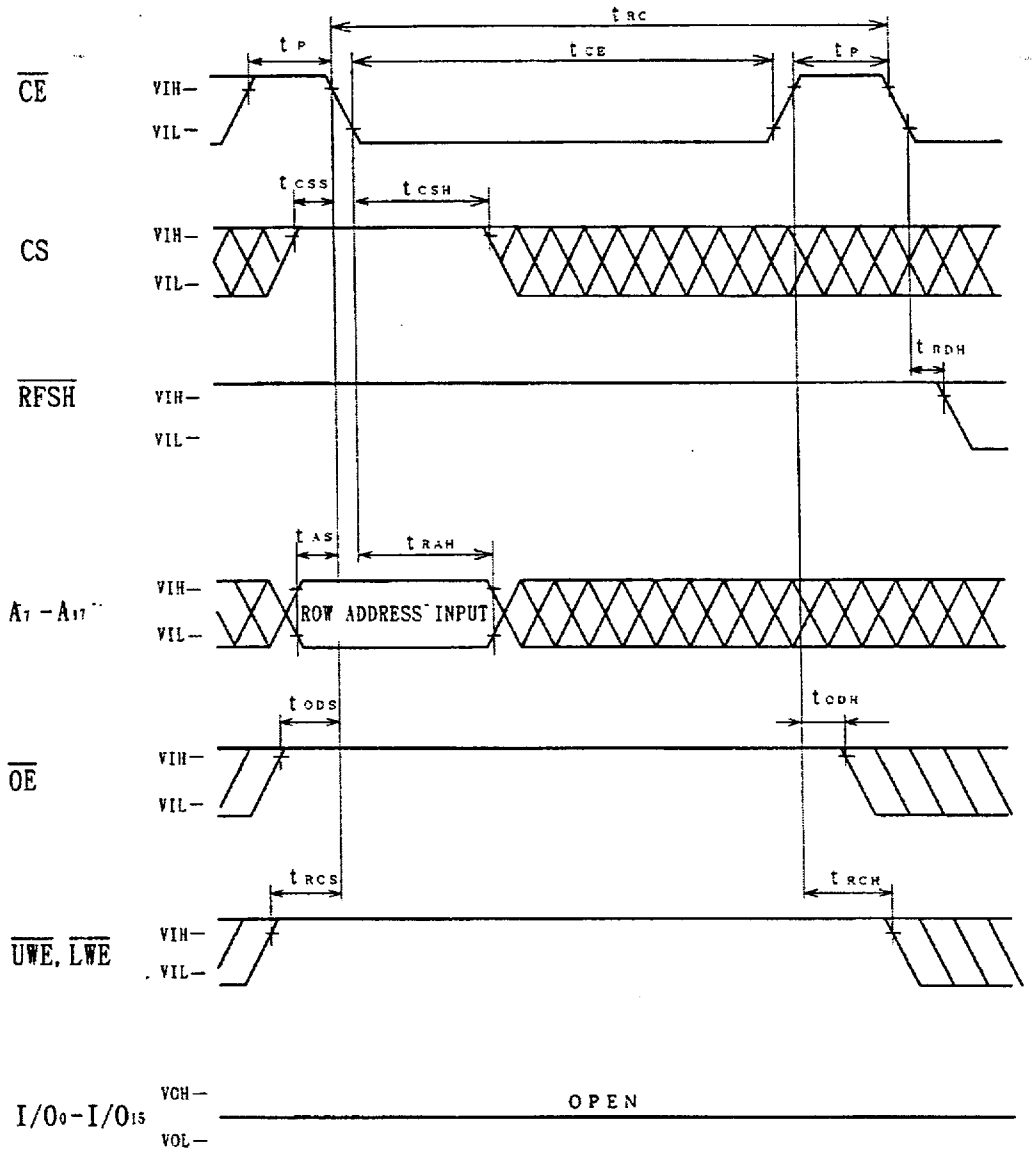
Write cycle(2) ($\overline{OE}$=Low, $\overline{CE}$ Control)



Read modify write cycle

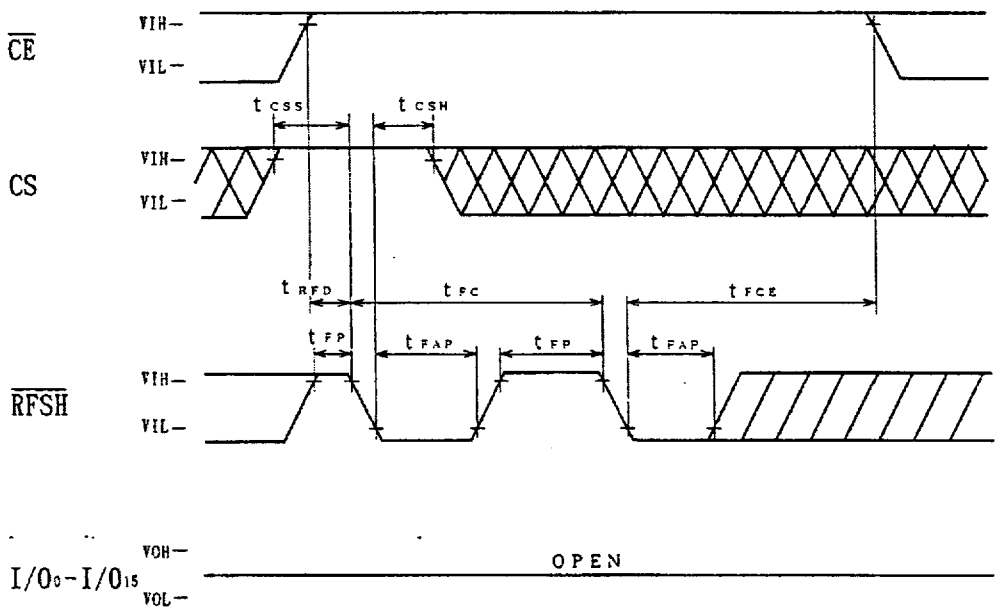


Address refresh cycle (Note. 10)



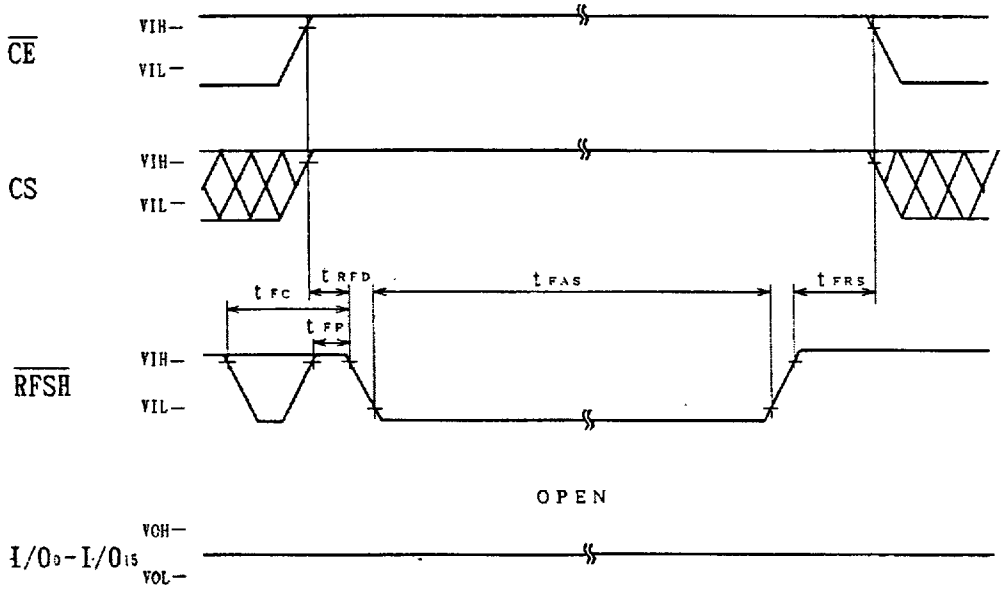
A0 - A6 =Don't Care

Auto refresh cycle (Note. 10, 12)



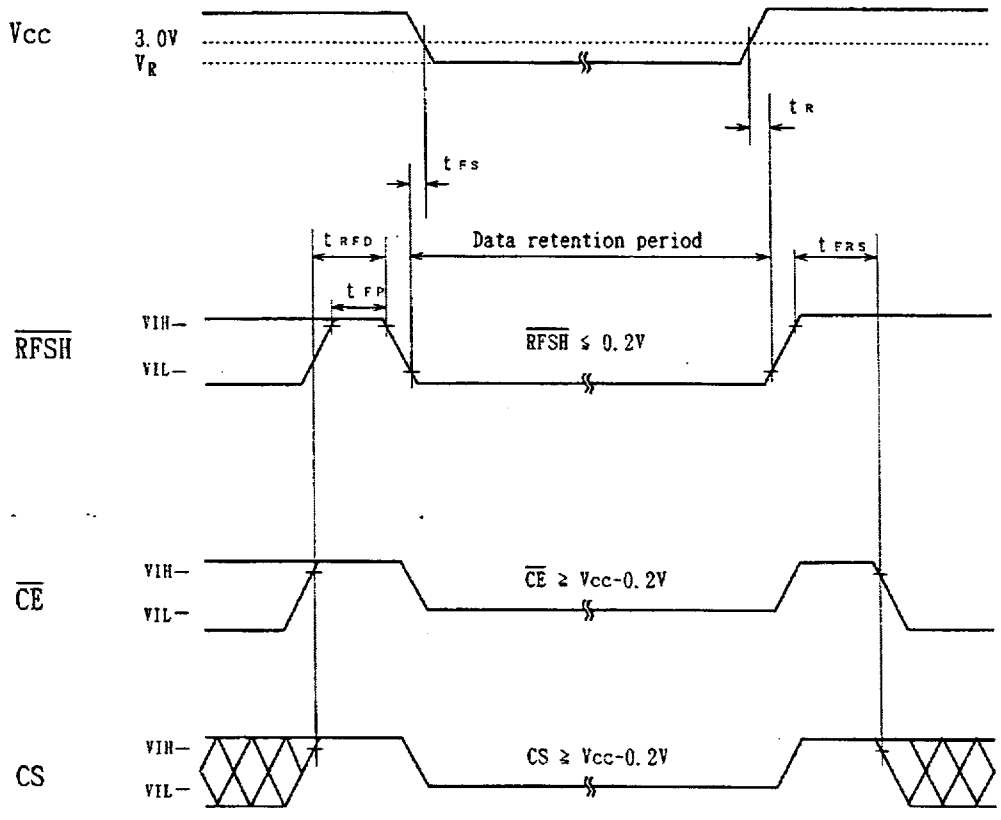
A_0 - A_{17}, $\overline{UWE}$, $\overline{LWE}$ and $\overline{OE}$ =Don't Care

Self refresh cycle (Note. 12)



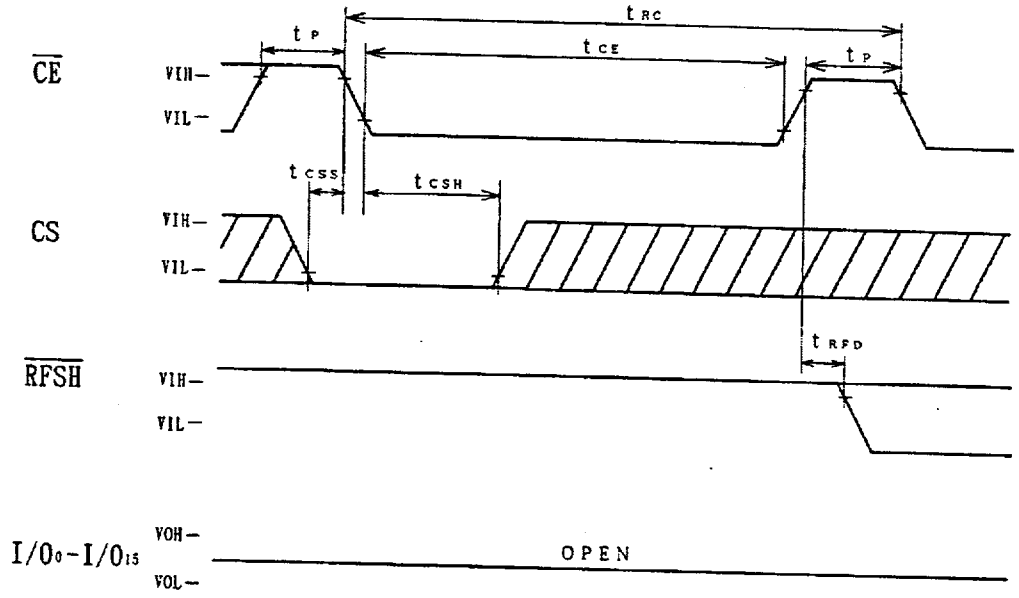
$A_0 - A_{17}$, $\overline{UWE}$, $\overline{LWE}$ and $\overline{OE}$ =Don't Care

Data Retention Mode (Note. 18, 19, 20, 21, 22)



A_0 - A_{17}, $\overline{UWE}$, $\overline{LWE}$ and $\overline{OE}$ =Don't Care

CS Standby mode



A_0 -A_{17}, $\overline{UWE}$, $\overline{LWE}$ and $\overline{OE}$ =Don't Care

13 Package and packing specification

1. Package Outline Specification

Refer to drawing No.AA1117

2. Markings

2−1. Marking contents

(1) Product name : LH5PV16256S−12LL

(2) Company name : SHARP

(3) Date code

(Example) YY WW ×××

- YY: Denotes the production year. (Lower two digits of the year.)
- WW: Denotes the production week. (01, 02, 03, · · · · · 52, 53)
- ×××: Denotes the production ref.code (1-3)

Indicates the product was manufactured in the WWth week of 19YY.

(4) The marking of "JAPAN" indicates the country of origin.

2−2. Marking layout

Refer drawing No.AA1117

(This layout do not define the dimensions of marking character and marking position.)

3. Packing Specification (Dry packing for surface mount packages)

- Dry-packing is used for the purpose of maintaining IC quality after mounting packages on the PCB (Printed Circuit Board).

When the epoxy resin which is used for plastic packages is stored at high humidity, it may absorb 0.15% or more of its weight in moisture. If the surface mount type package for a relatively large chip absorbs a large amount of moisture between the epoxy resin and insert material (e.g. chip, lead frame) this moisture may suddenly vaporize into steam when the entire package is heated during the soldering process (e.g. VPS). This causes expansion and results in separation between the resin and insert material, and sometimes cracking of the package. This dry packing is designed to prevent the above problem from occurring in surface mount packages.

3−1. Packing Materials

Material Name	Material Specificaiton	Purpose
Tray	Conductive plastic (50devices/tray)	Fixing of device
Upper cover tray	Conductive plastic (1tray/case)	Fixing of device
Laminated aluminum bag	Aluminum polyethylene (1bag/case)	Drying of device
Desiccant	Silica gel	Drying of device
P P band	Polypropylene (3pcs/case)	Fixing of tray
Inner case	Card board (500devices/case)	Packaging of device
Label	Paper	Indicates part number, quantity and date of manufacture
Outer case	Card board	Outer packing of tray

(Devices shall be placed into a tray in the same direction.)

3－2. Outline dimension of tray
Refer to attached drawing

4. Storage and Opening of Dry Packing

4－1. Store under conditions shown below before opening the dry packing
(1) Temperature range : 5～40℃
(2) Humidity : 80% RH or less

4－2. Notes on opening the dry packing
(1) Before opening the dry packing, prepare a working table which is grounded against ESD and use a grounding strap.
(2) The tray has been treated to be conductive or anti-static. If the device is transferred to another tray, use a equivalent tray.

4－3. Storage after opening the dry packing
Perform the following to prevent absorption of moisture after opening.
(1) After opening the dry packing, store the ICs in an environment with a temperature of 5～25℃ and a relative humidity of 60% or less and mount ICs within 3 days after opening dry packing.

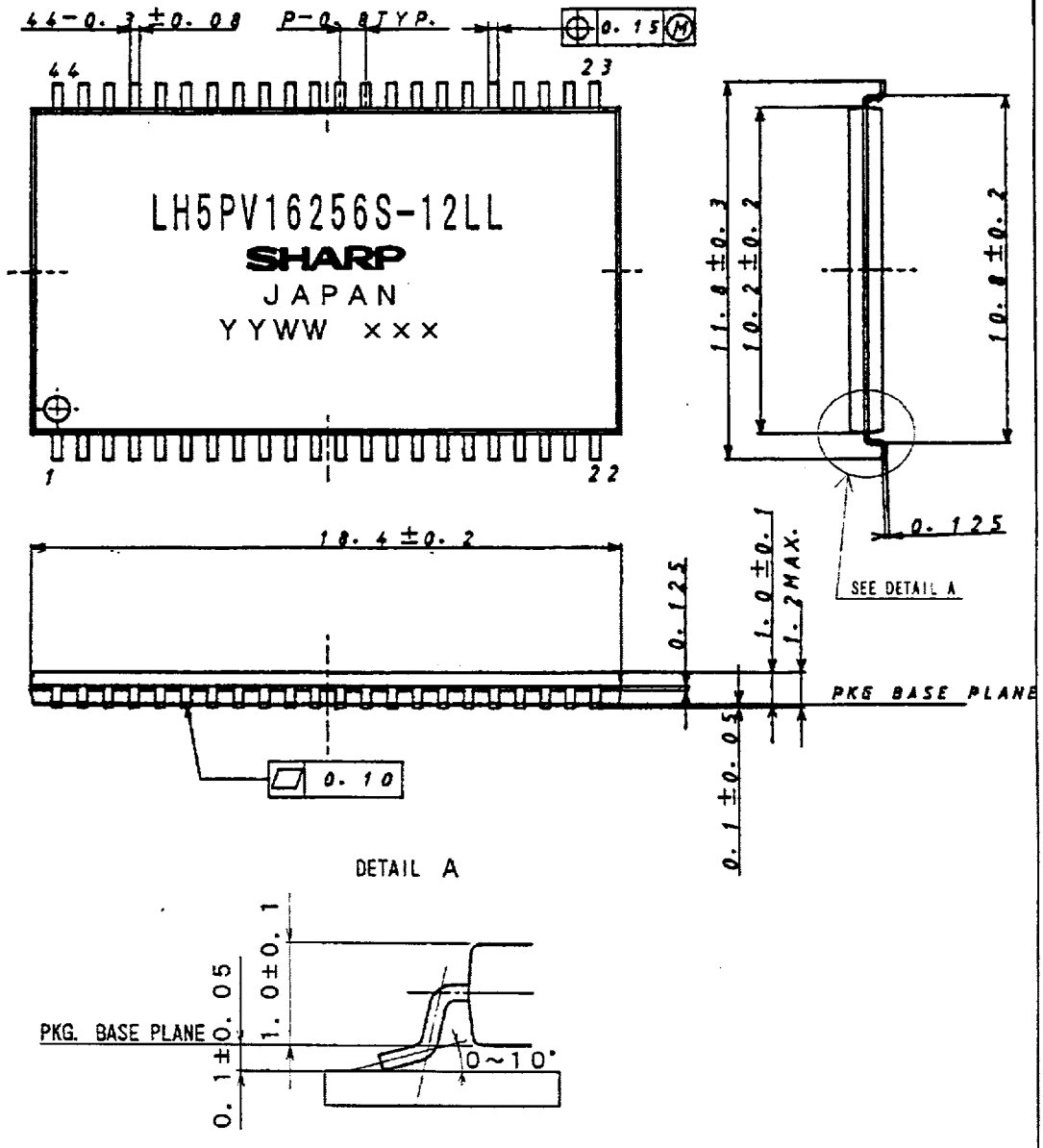
4－4. Baking (drying) before mounting
(1) Baking is necessary
(A) If the humidity indicator in the desiccant becomes pink
(B) If the procedure in section 4－3 could not be performed
(2) Recommended baking conditions
If the above conditions (A) and (B) are applicable, bake it before mounting. The recommended conditions are 4 hours or more at 125℃.
Heat resistance tray is used for shipping tray.

5. Surface Mount Conditions
Please perform the following conditions when mounting ICs not to deteriorate IC quality.

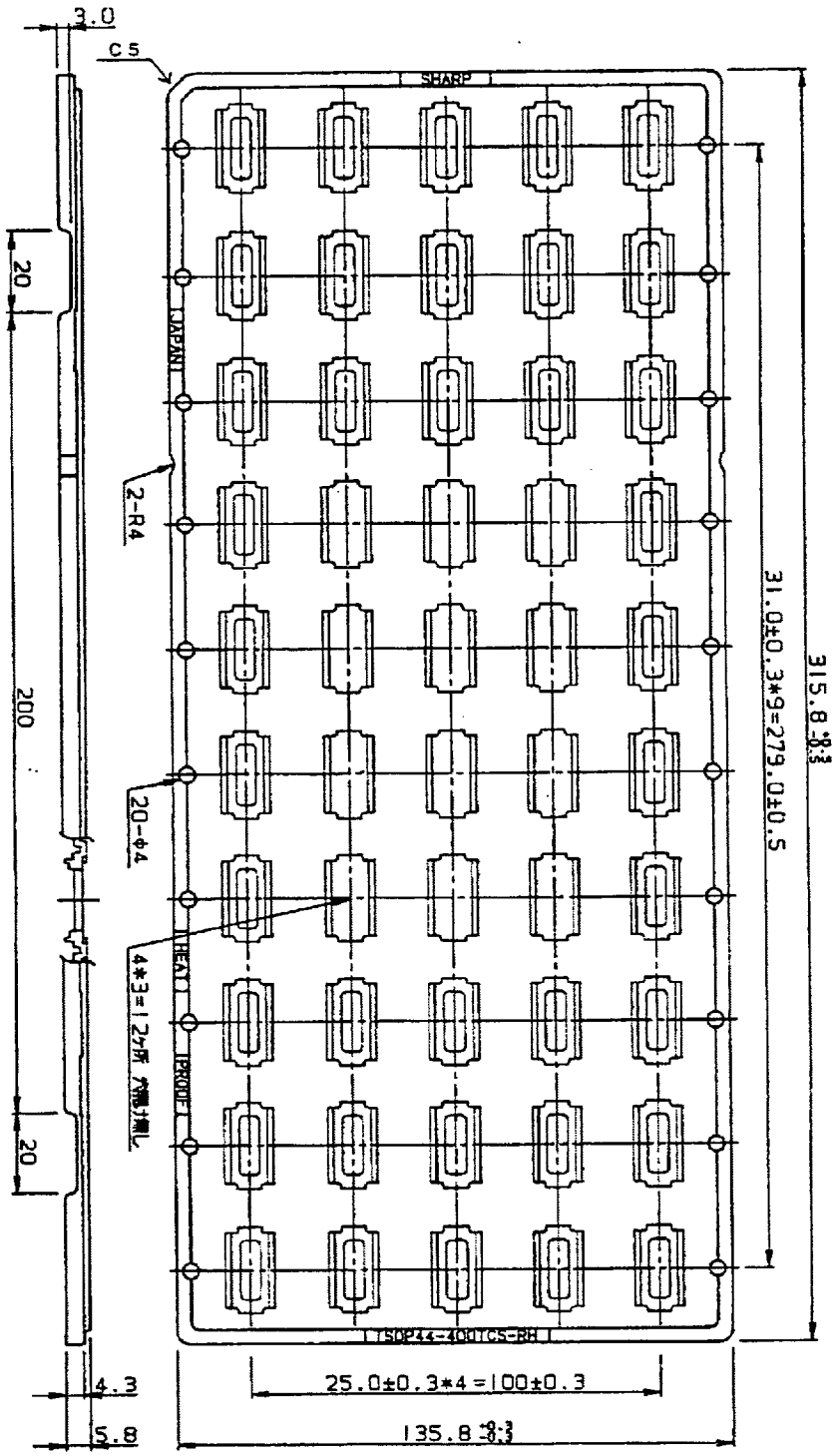
5－1. Soldering conditions (The following conditions are valid only for one time soldering.)

Mounting Method	Temperature and Duration	Measurement Point
Reflow soldering (air)	Peak temperature of 240℃, duration less than 15 seconds above 230℃, temperature increase rate of 1～4℃/second	IC surface
Manual soldering (soldering iron)	260℃ or less, duration less than 10 seconds	IC outer lead surface

5－2. Conditions for removal of residual flux
(1) Ultrasonic washing power : 25 Watts/liter or less
(2) Washing time : Total 1 minute maximum
(3) Solvent temperature : 15～40℃



名称 NAME	TSOP44-P-400	リード仕上 LEAD FINISH	TIN-LEAD PLATING	備考 プラスチックパッケージ外形寸法は、バリを含まないものとする。 NOTE Plastic body dimensions do not include burr of resin.
DRAWING NO.	AA1117	単位 UNIT	mm	



名称 NAME	TSOP44-400TCS-RH			備考 NOTE
DRAWING NO.	CV704	単位 UNIT	mm	