Description

The μPD42644 is a fast-page, low-power dynamic RAM organized as 1,048,576 words by 4 bits and designed to operate from a single +5-volt power supply. Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CAS}$ low. Data outputs return to high impedance when $\overline{CAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1,024 address combinations of A_0 - A_9 during a 16-ms refresh period.

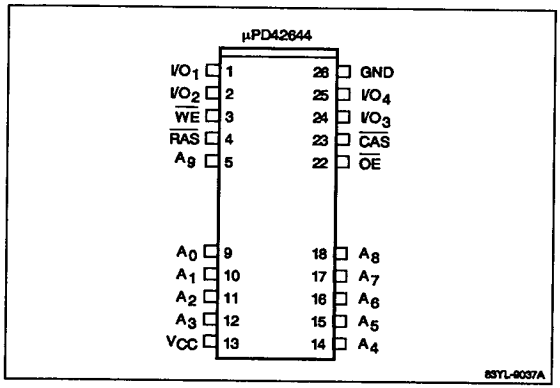
A low-power self-refresh cycle allows the μPD42644 to retain data for extended periods of time with very low power consuption (30 μA at 50°C). This feature allows the μPD42644 to be used in battery backup applications with greater savings in power consumption.

Features

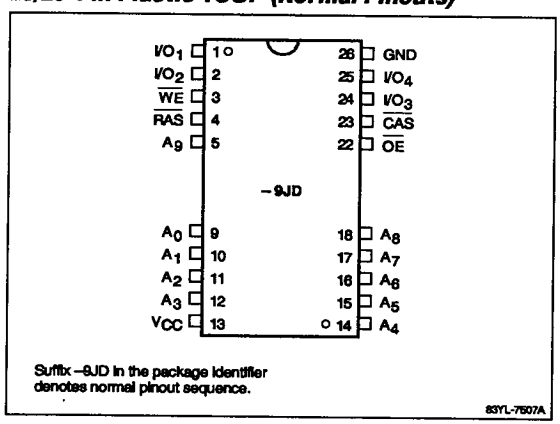
- 1,048,576 by 4-bit organization
- Single +5-volt power supply
- Fast-page option
- Low power dissipation
  - — 90 mA active
  - — 1.0 mA standby (CMSO interface)
  - — 30 μA self-refresh (t_{RCF} = 32 μs, T_A = 50°C)
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Automatic self-refreshing by $\overline{RAS}$ input cycling
- Nonlatched, three-state outputs
- Low input capacitance
- 1024 refresh cycles every 16 ms
- 26/20-pin plastic SOJ (300 mil), 20-pin plastic ZIP, and 26/20-pin plastic TSOP packaging

Pin Configurations

26/20-Pin Plastic SOJ

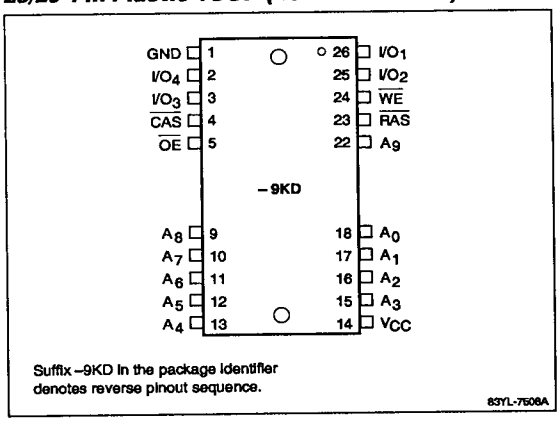


26/20-Pin Plastic TSOP (Normal Pinouts)



Pin Configurations (cont)

26/20-Pin Plastic TSOP (Reverse Pinouts)



Suffix –9KD in the package identifier denotes reverse pinout sequence.

83YL-7508A

Pin Identification

Name	Function
A_0 - A_9	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

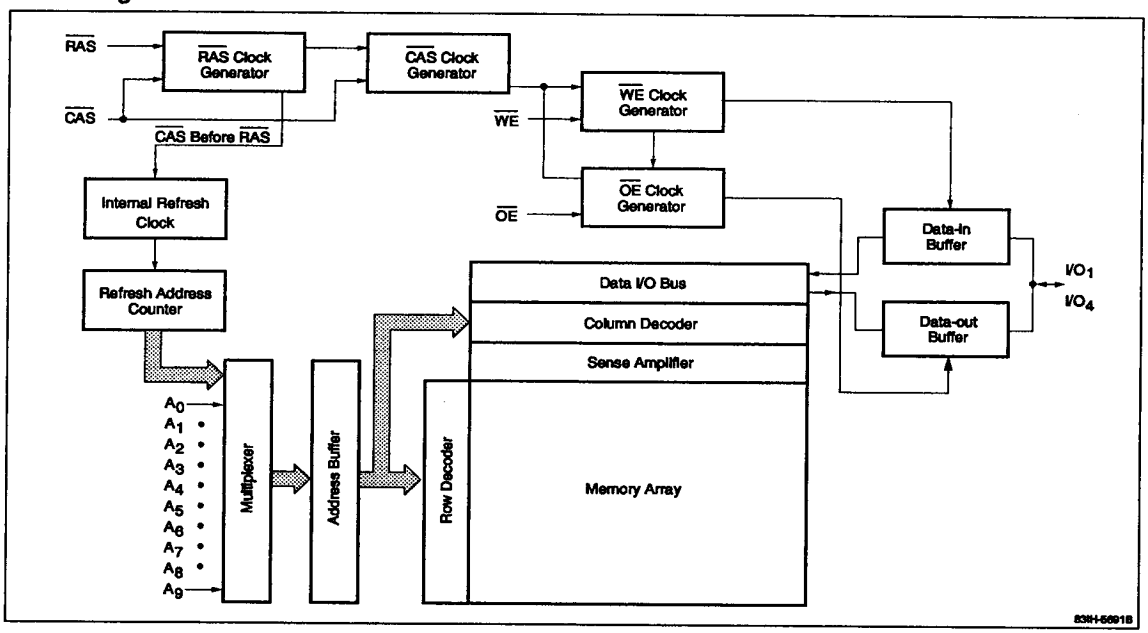
Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_4

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V; A_0 - A_9, I/O and $\overline{WE}$ ≥ V_{CC} − 0.2 or ≤ 0.2 V; $I_{I/O}$ = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

Block Diagram



Ordering Information

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Power Option	Package
μPD42644LA-80L	80 ns	160 ns	50 ns	Standard	26/20-pin plastic SOJ (300 mil)
μPD42644GS-80L	80 ns	160 ns	50 ns	Standard	26/20-pin plastic TSOP (normal pinouts)
μPD42644GSM-80L	80 ns	160 ns	50 ns	Standard	26/20-pin plastic TSOP (reverse pinouts)

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-80		-10			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		90		80	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC4}		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, self-refresh mode, average	I_{CC5}		30		30	μA	$\overline{RAS}$ cycling at 32 kHz (Notes 16, 17, 18)
			60		60	μA	$\overline{RAS}$ cycling at 64 kHz (Notes 16, 17, 18)
			120		120	μA	$\overline{RAS}$ cycling at 128 kHz (Notes 16, 17, 18)
Operating current, fast-page cycle, average	I_{CC6}		90		60	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		40		50	ns	(Notes 3, 4, 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		45		55	ns	(Notes 3, 4, 7, 8)
Column address setup time	t_{ASC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	65		80		ns	(Note 14)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		25	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		20		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		ns	(Notes 4, 7)
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		15		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP1}	10		10		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	45		55		ns	(Note 14)

AC Characteristics (cont)

Parameter	Symbol	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		ns	
Data-in hold time	t_{DH}	15		20		ns	(Note 13)
Data-in setup time	t_{DS}	0		0		ns	(Note 13)
Access time from $\overline{OE}$	t_{OEA}		20		25	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ delay data time	t_{OED}	20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		ns	
$\overline{OE}$ to inactive setup time	t_{OES}	0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	20	0	25	ns	(Note 9)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		ns	(Notes 6, 7)
Fast-page cycle time	t_{PC}	50		60		ns	(Note 6)
Fast-page read-modify-write cycle time	t_{PRWC}	100		120		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		80		100	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	17	50	ns	(Note 8)
Row address hold time	t_{RAH}	12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	80	125,000	100	125,000	ns	
Random read or write cycle time	t_{RC}	160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	70	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		ns	
Refresh period	t_{REF}		32		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		ns	(Note 11)
$\overline{RAS}$ hold time	t_{RSH}	20		25		ns	
Read-write cycle time	t_{RWC}	210		250		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	105		130		ns	(Note 14)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		20		ns	(Note 12)
Write command setup time	t_{WCS}	0		0		ns	(Note 14)
$\overline{WE}$ hold time	t_{WHR}	15		20		ns	

AC Characteristics (cont)

Parameter	Symbol	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write command pulse width	t_{WP}	15		20		ns	(Note 12)
$\overline{WE}$ setup time	t_{WSR}	10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70 °C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V and V_{OL} = 0.8 V).

(8) If $t_{RCD} \leq t_{RCS}$ (max) and $t_{RAD} \leq t_{RAD}$ (max) access time is defined by t_{RAC} (max). If $t_{RCD} \geq t_{RCD}$ (max) access time is defined by t_{CAC} (max) and if $t_{RAD} \geq t_{RAD}$ (max) access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(13) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(14) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(15) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertantly be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

(16) When $t_{CSF} \leq 35$ ms, I_{CC5} depends on the $\overline{RAS}$ clock; I_{CC5} (typ) = 1.5 mA. When $t_{CSF} \geq 35$ ms, I_{CC5} (typ) = 1.5 mA in the first 35 ms after a self-refresh set cycle is applied (depending on the status of $\overline{RAS}$). Subsequently, I_{CC5} is 120 μA or as shown in the following table for the -L version.

Operating Temperature (T_A)	Clock Frequency (min)	Self-Refresh Current (max)
0 to 50°C	32 kHz	30 μA at 32 kHz
0 to 60°C	64 kHz	60 μA at 64 kHz
0 to 70°C	128 kHz	120 μA at 128 kHz

(17) t_{RCF} depends on operating temperature as reflected in the table below:

Operating Temperature (T_A)	t_{RCF} (max)
0 to 50°C	32 μs
0 to 60°C	16 μs
0 to 70°C	8 μs

(18) Average power supply current required for self-refreshing is measured according to the following conditions: $\overline{RAS}$ is cycling at 32, 64 or 128 kHz; $\overline{CAS} \leq 0.2$ V; $\overline{WE} \geq V_{CC} - 0.2$ V; $V_{IH} > V_{CC} - 0.2$ V; $V_{IL} < 0.2$ V; $t_T \leq 50$ ns; A_0 - A_9 and I/O = V_{CC} to GND. During self-refresh operation, the $\overline{RAS}$ input must be cycled at or exceeding the minimum frequency requirements.

Self-Refresh Cycle

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
$\overline{CAS}$ pulse width in self-refresh operation	t_{CSF}	360		ns	(Note 1)
$\overline{RAS}$ cycle time in self-refresh operation	t_{RCF}	360	(Note 2)	ns	
$\overline{RAS}$ precharge time in self-refresh operation	t_{RPF}	200		ns	
$\overline{RAS}$ pulse width in self-refresh operation	t_{RSF}	150	1000	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time from self-refresh operation to normal read/write operation	t_{CRP2}	200		ns	
$\overline{CAS}$ setup time for self-refresh operation	t_{CSR2}	10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time $\overline{CAS}$ before $\overline{RAS}$ refresh operation	t_{CRP3}	40		ns	
$\overline{CAS}$ precharge time in $\overline{CAS}$ before $\overline{RAS}$ refresh operation	t_{CPC}	20		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time from self-refresh operation to normal read/write operation	t_{RPC2}	100		ns	

Notes:

(1) When $t_{CSF} \leq 35$ ms, I_{CC5} depends on the $\overline{RAS}$ clock; I_{CC5} (typ) = 1.5 mA. When $t_{CSF} \geq 35$ ms, I_{CC5} (typ) = 1.5 mA in the first 35 ms after a self-refresh set cycle is applied (depending on the status of $\overline{RAS}$). Subsequently, I_{CC5} is 120 μA or as shown in the following table for the –L version.

Operating Temperature (T_A)	Clock Frequency (min)	Self-Refresh Current (max)
0 to 50°C	32 kHz	30 μA at 32 kHz
0 to 60°C	64 kHz	60 μA at 64 kHz
0 to 70°C	128 kHz	120 μA at 128 kHz

(2) The value for t_{RCF} (min) is specified in AC Characteristics. The value for t_{RCF} (max) is dependent upon temperature as shown in the table below:

Operating Temperature (T_A)	t_{RCF} (max)
0 to 50°C	32 μs
0 to 60°C	16 μs
0 to 70°C	8 μs

(3) When exiting self-refresh to a period of read and write operation that includes $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, t_{RCR} is delayed between the last self-refresh cycle pulse and the first $\overline{CAS}$ before $\overline{RAS}$ cycle. When entering self-refresh operation, t_{RCF} is the delay between the last $\overline{CAS}$ before $\overline{RAS}$ cycle and the first self-refresh pulse.

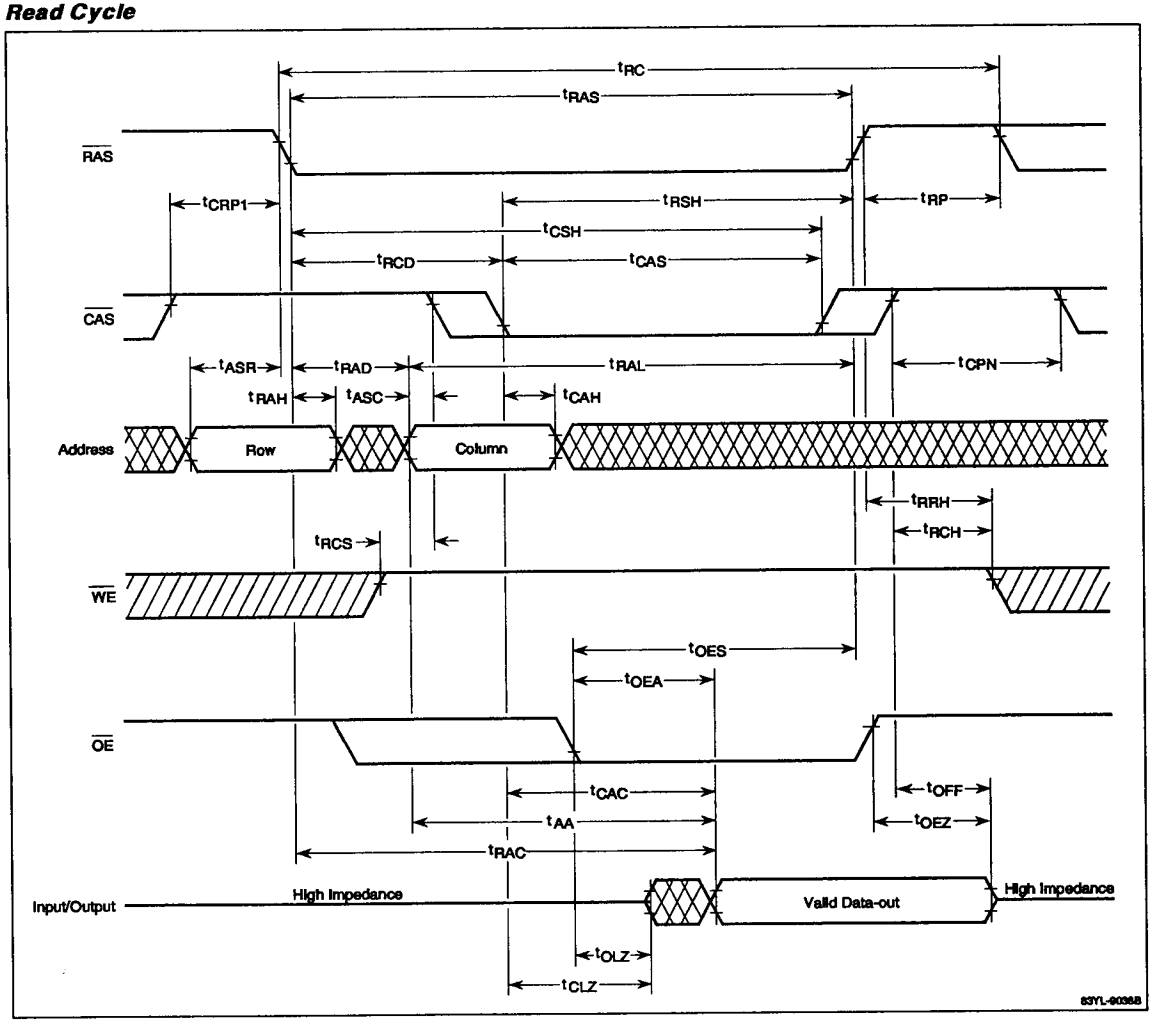
(4) In this period of normal read/write operation, there are no $\overline{CAS}$ before $\overline{RAS}$ refresh cycles or less than 1024 $\overline{RAS}$-only refresh cycles.

(5) The time delay beetween the last self-refresh pulse in one self-refresh cycle and the first self-refresh pulse in the next cycle is defined by t_{RCF} (max) when the intervening period of read and write operation meets the conditions in note 3.

(6) The bulit-in counter generates the refresh address in self-refresh and $\overline{CAS}$ before $\overline{RAS}$ refresh cycles. Since this address increments sequentialy from the last cycle in either self-refresh or $\overline{CAS}$ before $\overline{RAS}$ operation to the first cycle in the alternate refresh mode, $\overline{CAS}$ before $\overline{RAS}$ refreshing should be used during normal read and write operation to refresh one address location every 32 μs or less. If some other means of refreshing is used, it is necessary to execute a burst refresh of all storage cells just before changing to and just after exiting self-refresh operation.

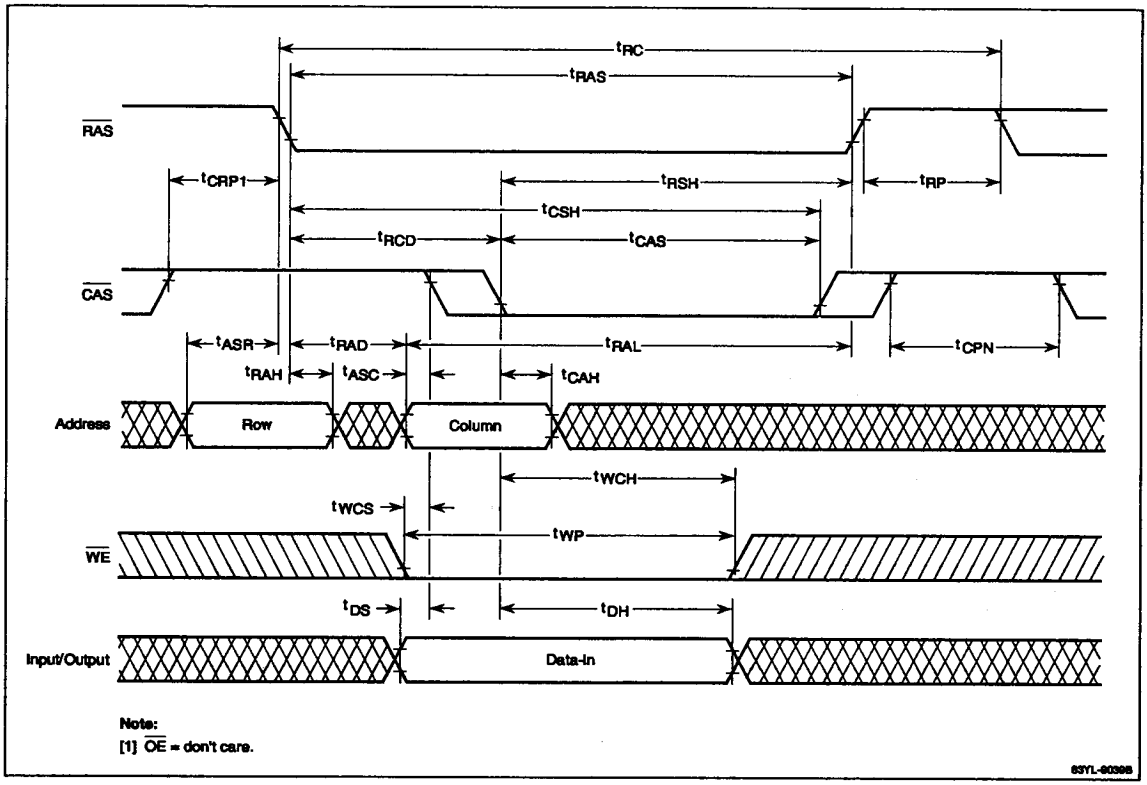
Timing Waveforms

Read Cycle



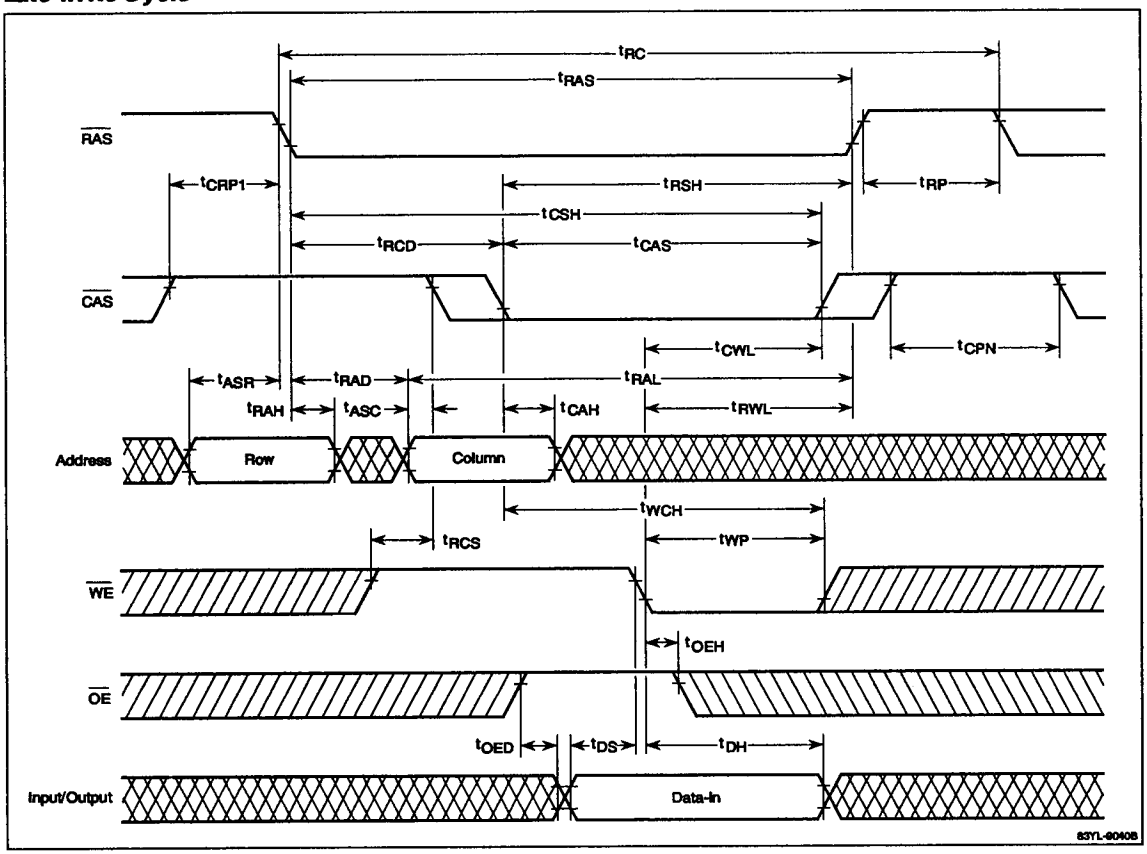
Timing Waveforms (cont)

Early Write Cycle



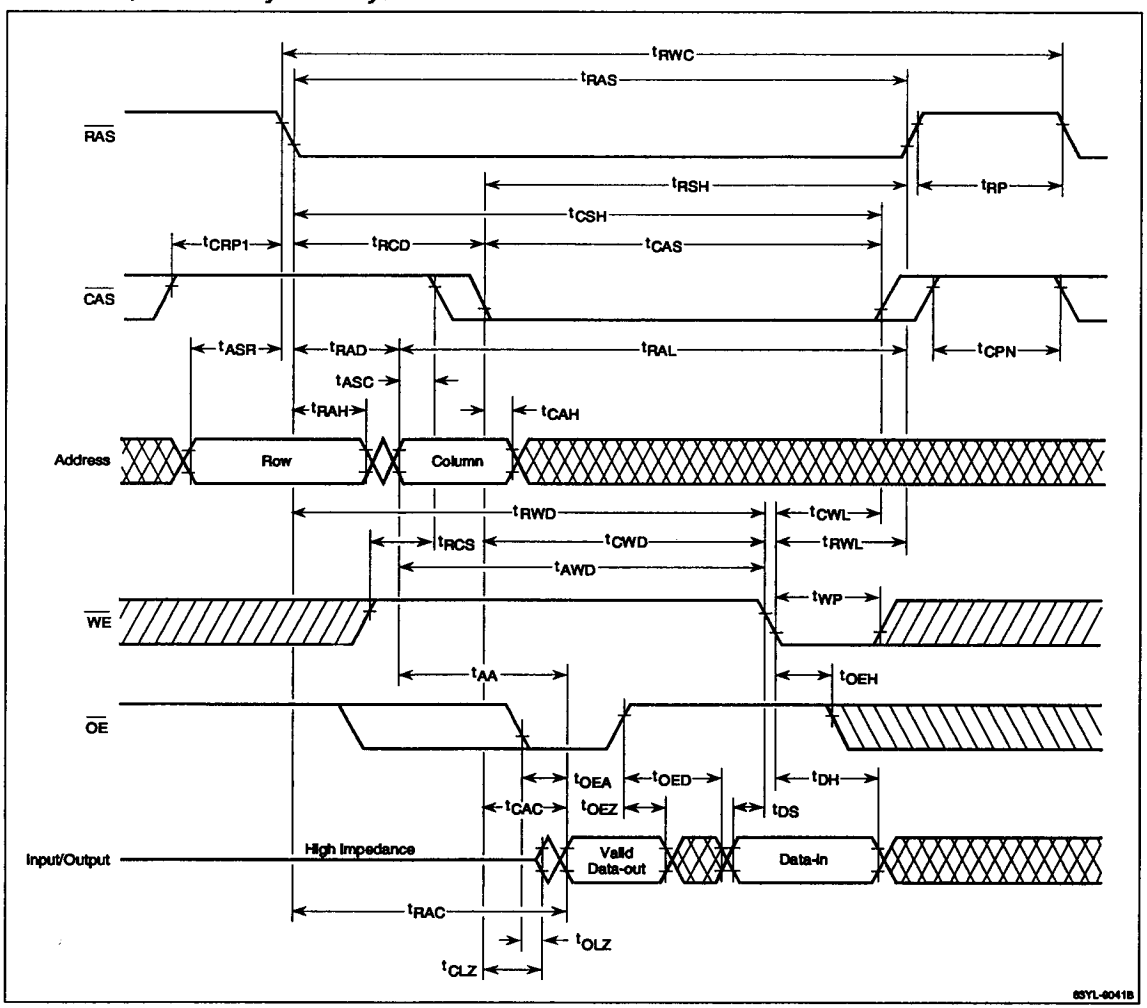
Timing Waveforms (cont)

Late Write Cycle



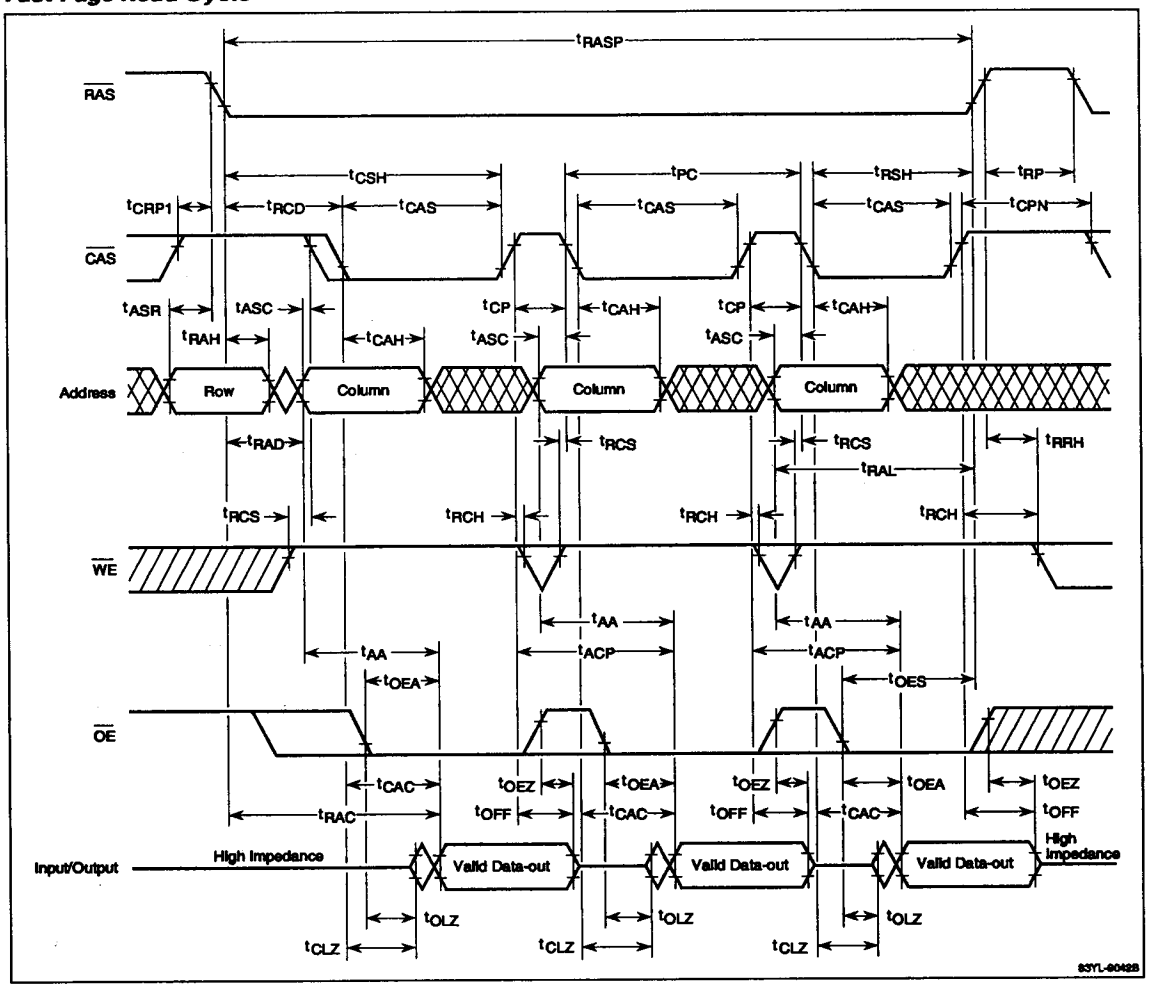
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



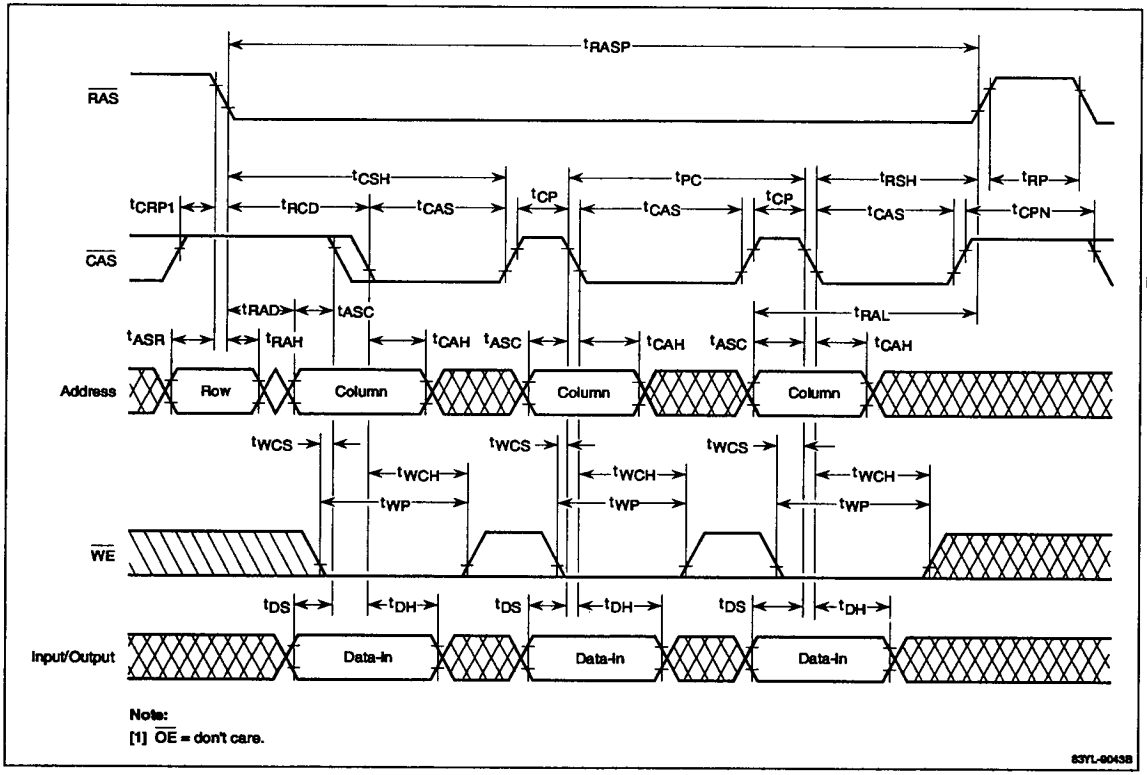
Timing Waveforms (cont)

Fast-Page Read Cycle



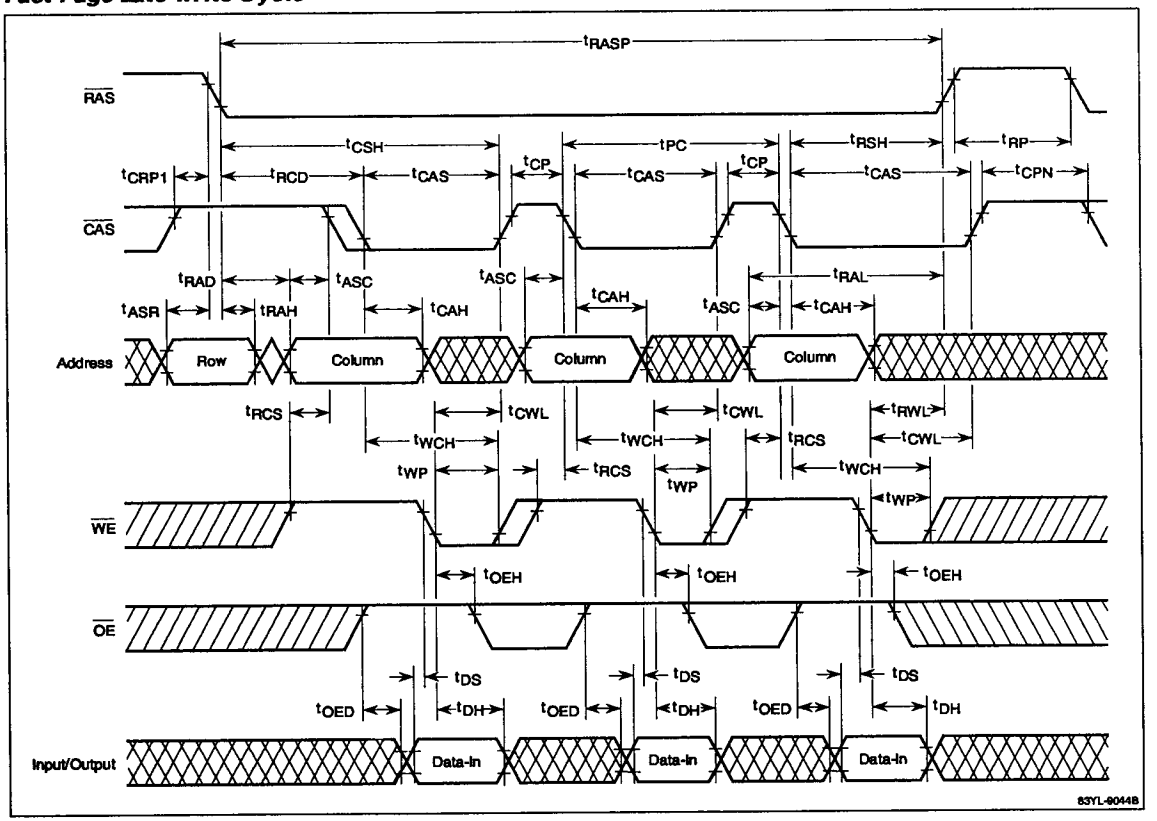
Timing Waveforms (cont)

Fast-Page Early Write Cycle



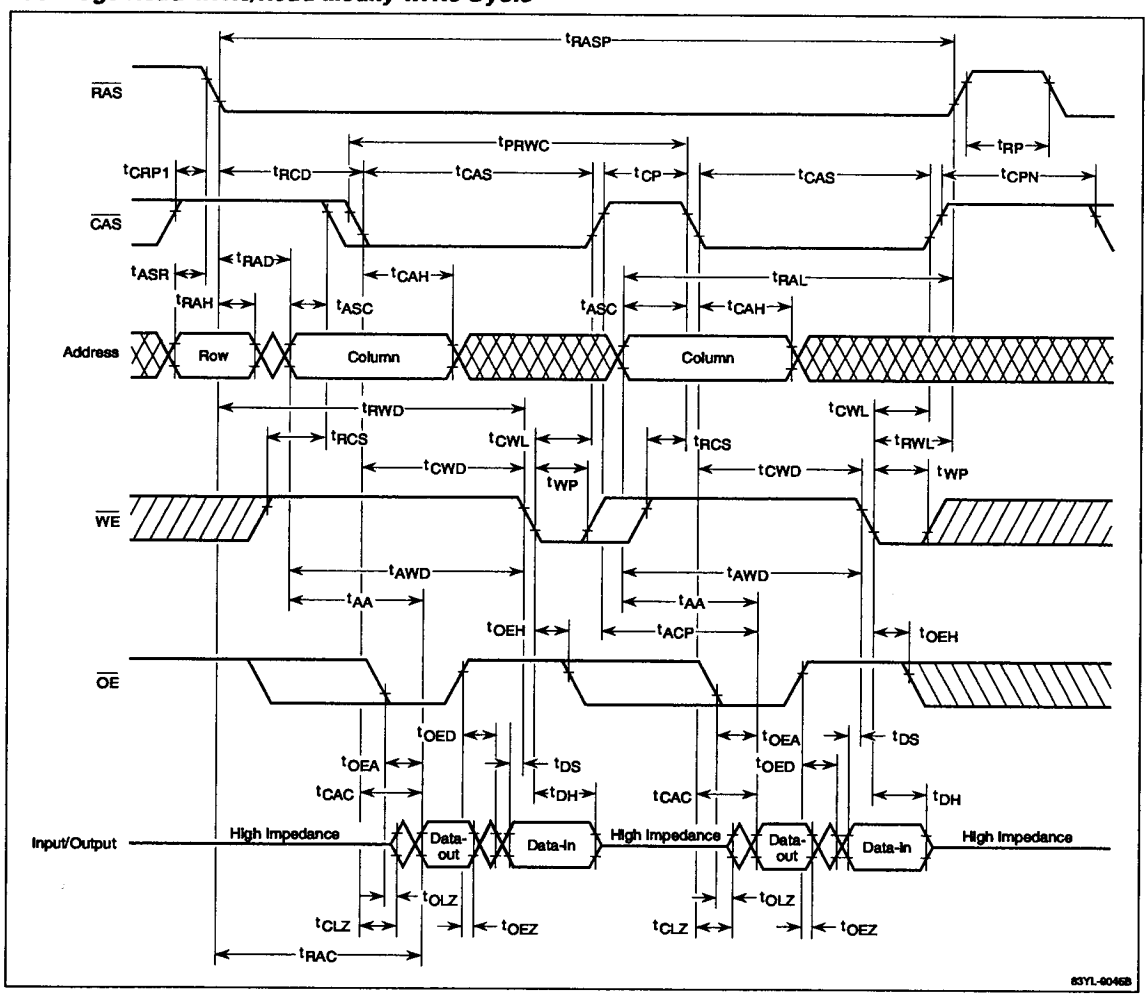
Timing Waveforms (cont)

Fast-Page Late Write Cycle



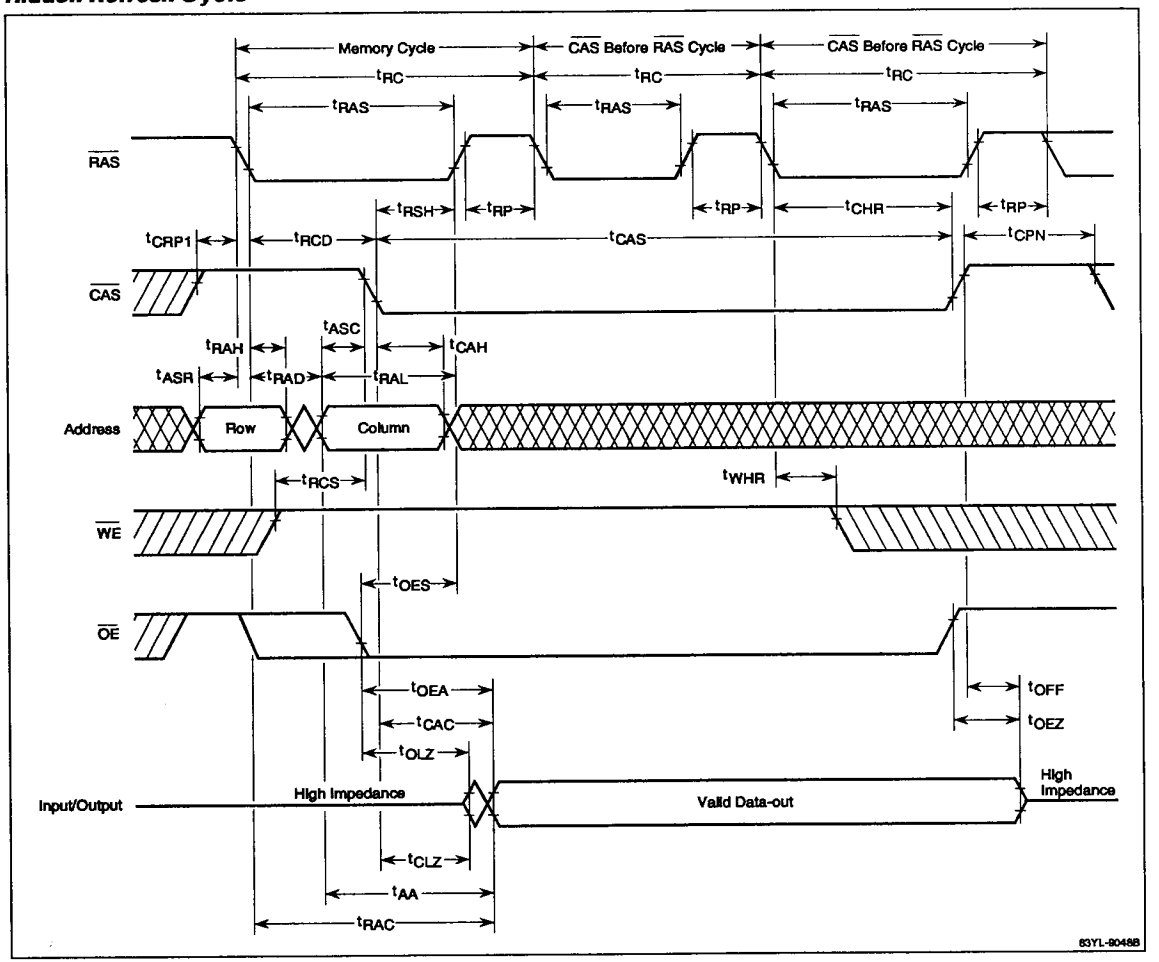
Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



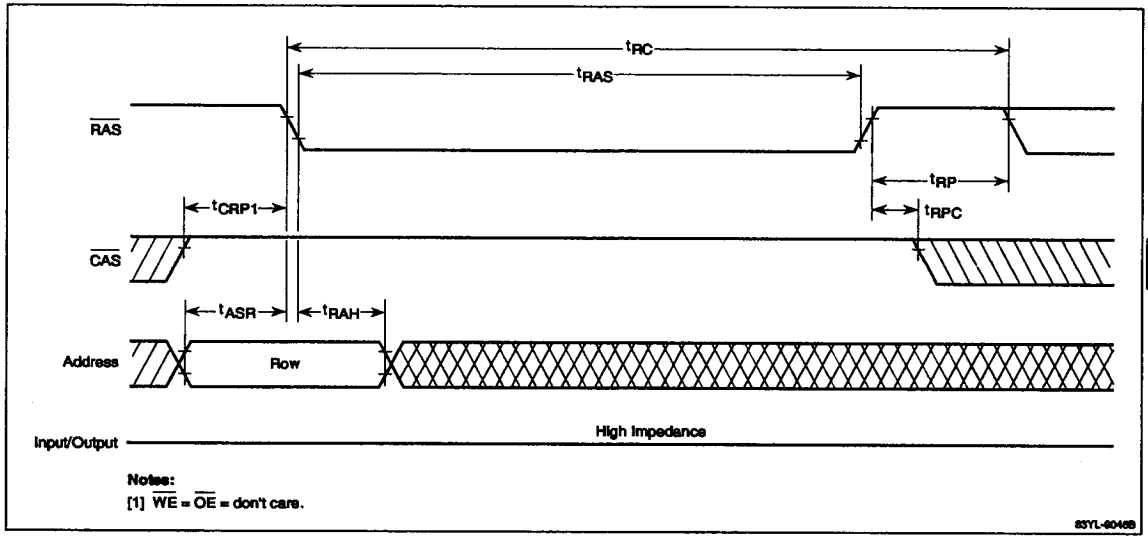
Timing Waveforms (cont)

Hidden Refresh Cycle

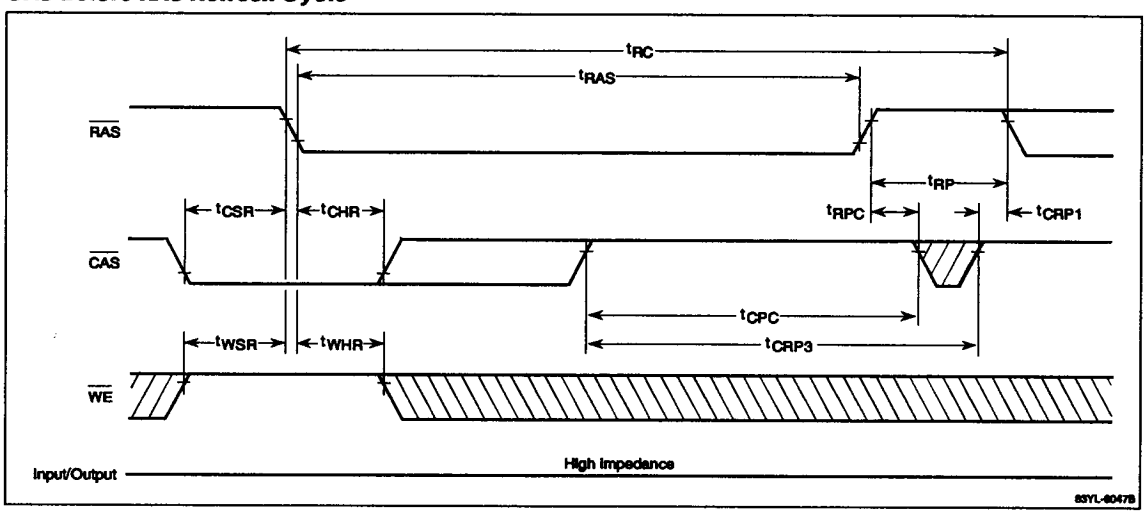


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle

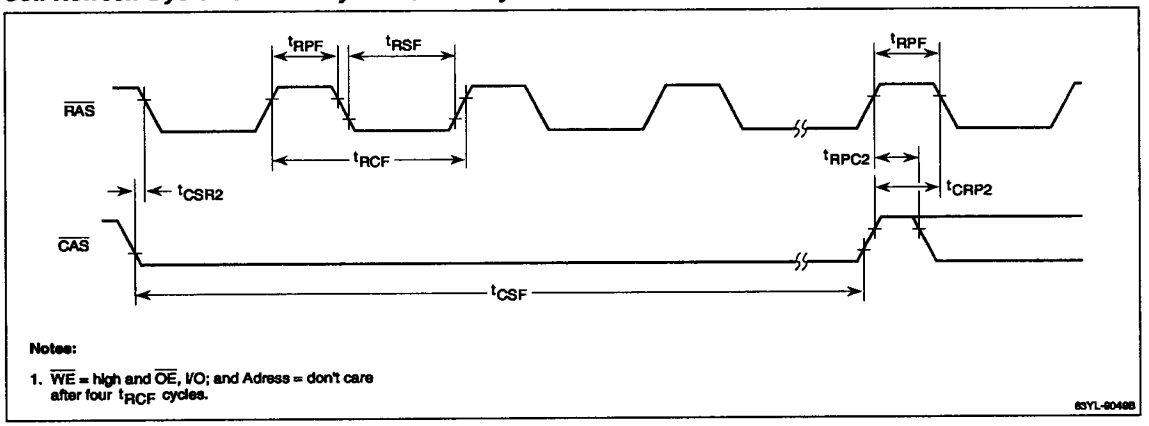


$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Timing Waveforms (cont)

Self-Refresh Cycle Followed by Read/WriteCycle

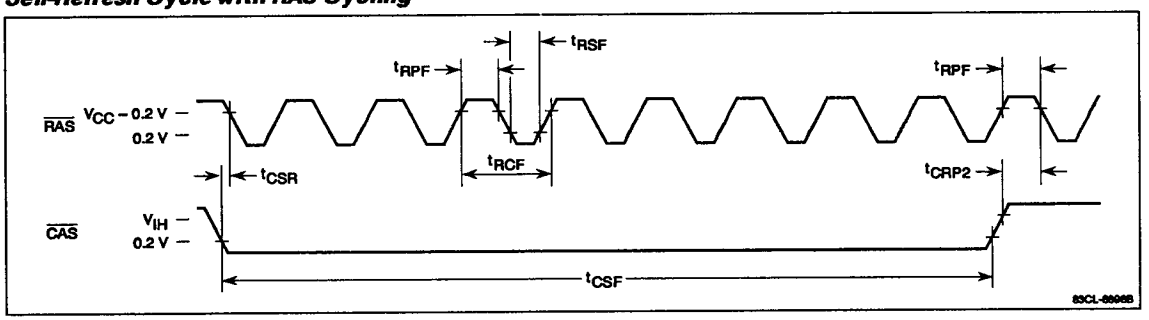


Notes:

1. $\overline{WE}$ = high and $\overline{OE}$, I/O; and Adress = don't care after four t_{RCF} cycles.

83YL-8049B

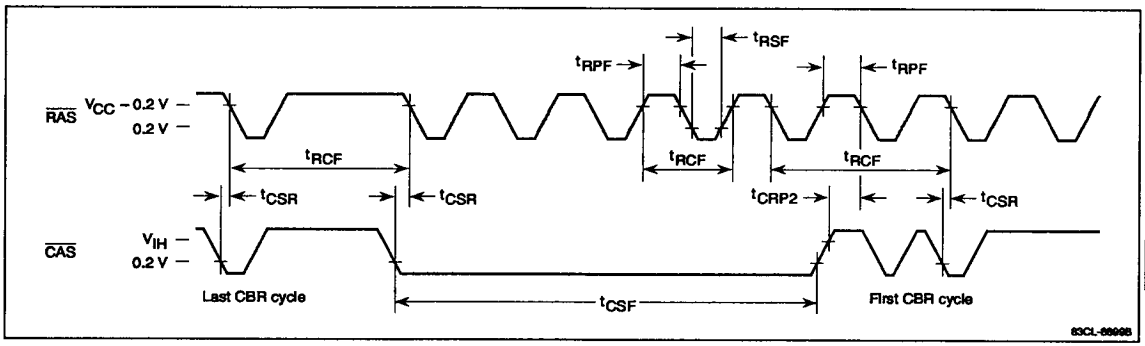
Self-Refresh Cycle with $\overline{RAS}$ Cycling



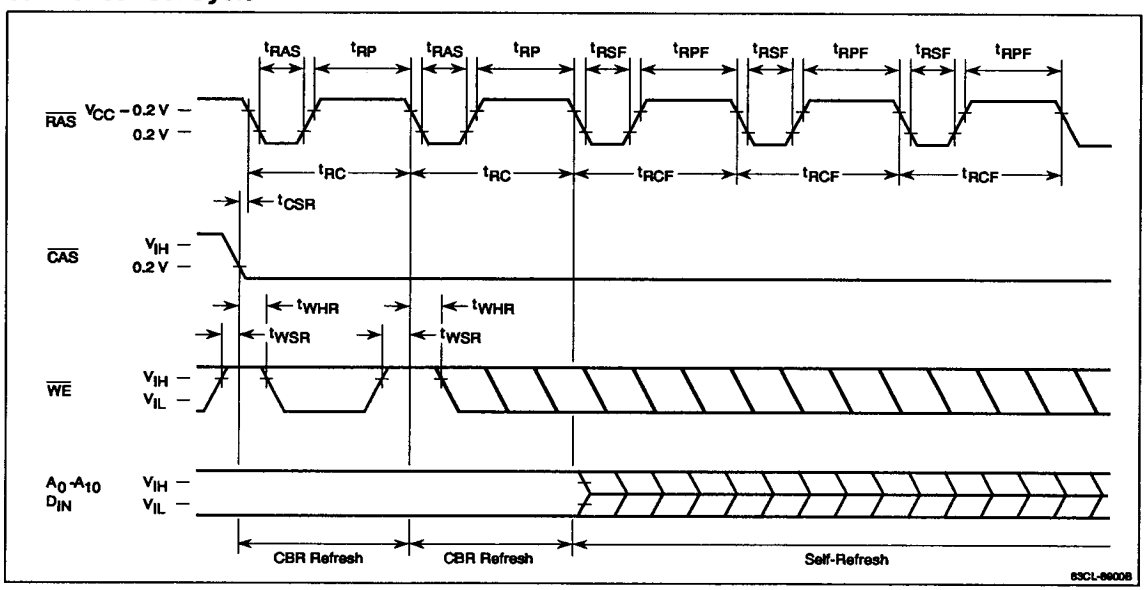
83CL-8006B

Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Followed by Self-Refresh Cycle



Self-Refresh Set Cycle



Timing Waveforms (cont)

Self-Refresh Set Cycle