μPD77522
ADPCM Codec

Preliminary

Description

The μPD77522 is a single-chip coder and decoder (codec) for 32-kb/s adaptive differential pulse-code modulation (ADPCM). The ADPCM technique conforms to the 1988 CCITT Recommendation G.721.

The serial data input to the coder and serial data output from the decoder can directly interface a PCM codec. The μPD77522 is ideal for application to digital cordless telephone systems in which the data rate of the PCM signal must be reduced.

Features

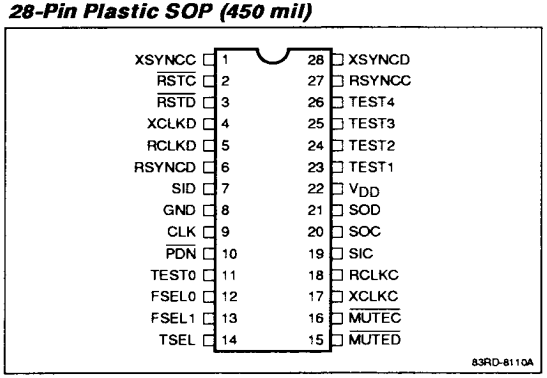
- 32-kb/s ADPCM codec conforms to CCITT Recommendation G.721
  - Processes high-quality modem signals up to 4800 b/s
  - Recovers from an error in the telecommunication circuit
  - Free from sound quality degradation in multistage digital connections
- Built-in digital signal processor (DSP)
- Simultaneous coding and decoding
- Pin-selectable PCM format: μ-law, A-law, or 16-bit linear
- Selectable coder and decoder muting
- Direct interface with μ-law or A-law PCM codec
- Low operating power
  - 28 mA max at 5 V
  - 20 mA max at 2.7 V
- Power-down mode
  - 100 μA max at 5 V
  - 70 μA max at 2.7 V

Ordering Information

Part No.	Package
μPD77522GU	28-pin plastic SOP (450 mil)

Pin Configuration

28-Pin Plastic SOP (450 mil)



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Pin Identification

Symbol	I/O	Function
CLK	In	System clock, 10 to 14 MHz
FSEL0	In	Format select 0
FSEL1	In	Format select 1
$\overline{\text{MUTEC}}$	In	Coder mute control
$\overline{\text{MUTED}}$	In	Decoder mute control
$\overline{\text{PDN}}$	In	Power-down control
RCLKC	In	PCM data clock to coder
RCLKD	In	ADPCM data clock to decoder
$\overline{\text{RSTC}}$	In	Coder reset
$\overline{\text{RSTD}}$	In	Decoder reset
RSYNCC	In	Frame sync for coder PCM input
RSYNCD	In	Frame sync for decoder ADPCM input
SIC	In	PCM serial data input to coder
SID	In	ADPCM serial data input to decoder
SOC	Out	ADPCM serial data output from coder
SOD	Out	PCM serial data output from decoder
TEST0	In	Factory test; connect to ground for normal use
TEST1–TEST4	I/O	Factory test; connect to ground for normal use

Pin Identification (cont)

Symbol	I/O	Function
TSEL	In	Data input/output timing select
XCLKC	In	Transmit (output) data clock to coder
XCLKD	In	Transmit (output) data clock to decoder
XSYNCC	In	Frame sync for coder ADPCM output
XSYNCD	In	Frame sync for decoder PCM output
V_{DD}	In	+5-volt dc power
GND	In	Signal and power ground

FUNCTIONAL OPERATION

The block diagram shows serial data signal flow through the μPD77522, PCM-to-ADPCM on the coder side and ADPCM-to-PCM on the decoder side. Note that signal names are suffixed with C or D to denote the coder or decoder side, respectively.

Figure 1 shows the equivalent circuits at input and output pins.

Block Diagram

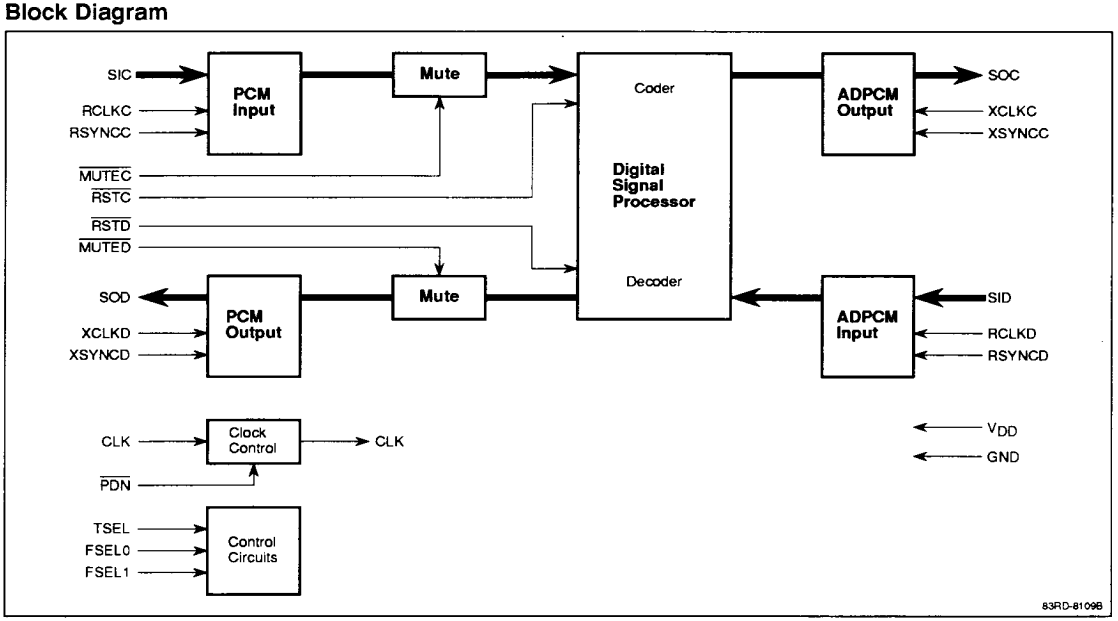
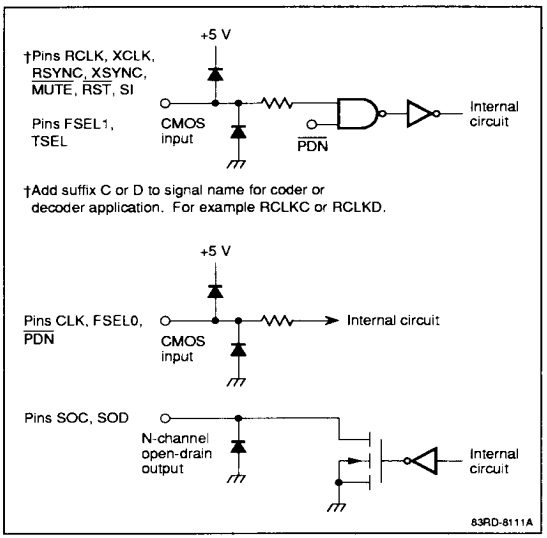


Figure 1. Input and Output Circuits



Power-Up

Following the application of power, the μPD77522 enters the standby state within 250 μs after system clock (CLK) input. In this state, PCM or ADPCM signals may be input. See figure 2.

Low inputs at $\overline{\text{RSTC}}$ and $\overline{\text{RSTD}}$ reset the coder and decoder, enabling operation. Reset timing is the same as the timing in figure 2 to fetch the least significant bit (LSB) of the SIC and SID input data. The state of the SOC and SOD output pins at reset is high impedance or low level.

Power-Down

Two clock cycles after a low level is applied to the $\overline{\text{PDN}}$ pin, the μPD77522 enters the power-down mode. The low level must be maintained for at least four clock cycles. See figure 3.

In power-down mode, the SIC and SOD output pins are in the high-impedance state.

Two clock cycles after a high level is applied to the $\overline{\text{PDN}}$ pin, the μPD77522 is released from the power-down mode. Before restarting the μPD77522, reset the coder and decoder by low inputs at the $\overline{\text{RSTC}}$ and $\overline{\text{RSTD}}$ pins.

Data Signal Interface

PCM and ADPCM data signals are input or output serially (MSB first) in synchronization with the frame sync and data clock signals listed in table 1. Frame sync is 8 kHz and the data clock is in the 64 kHz to 2.048 MHz range.

Table 1. PCM and ADPCM Interfaces

Interface	Frame Sync	Data Clock	Data
PCM input to coder	RSYNCC	RCLKC	SIC
ADPCM output from coder	XSYNCC	XCLKC	SOC
ADPCM input to decoder	RSYNCD	RCLKD	SID
PCM output from decoder	XSYNCD	XCLKD	SOD

Data Signal Timing

The first data bit of a frame may begin with the rising or falling edge of frame sync depending on the type of PCM codec the μPD77522 interfaces. The selection is made by connecting the TSEL pin to + 5V (1) or ground (0) as shown in figure 4.

PCM Codec	TSEL Pin
μPD95xx Series	1
μPD96xx Series	0

Coder Operation

When frame sync RSYNCC goes high, input data from the PCM codec at the SIC pin is stored in an internal register in synchronization with the trailing edge of data clock RCLKC. The data may be 8-bit companded or 16-bit linear.

The coder converts the PCM input data to 4-bit ADPCM output data and stores it in an internal register. When frame sync XSYNCC goes high, the ADPCM data is output at the SOC pin in synchronization with the leading edge of data clock XCLKC. The SOC pin returns to high impedance when the data output is complete.

Decoder Operation

When frame sync RSYNCD goes high, 4-bit ADPCM input data at the SID pin is stored in an internal register in synchronization with the trailing edge of data clock RCLKD.

The decoder converts the ADPCM input data to PCM data, 8-bit companded or 16-bit linear. When frame sync XSYNCD goes high, the PCM data is output at the SOD pin in synchronization with the leading edge of data clock XCLKD. The SOD pin returns to high impedance when the data output is complete.

Figure 2. Power-Up Timing

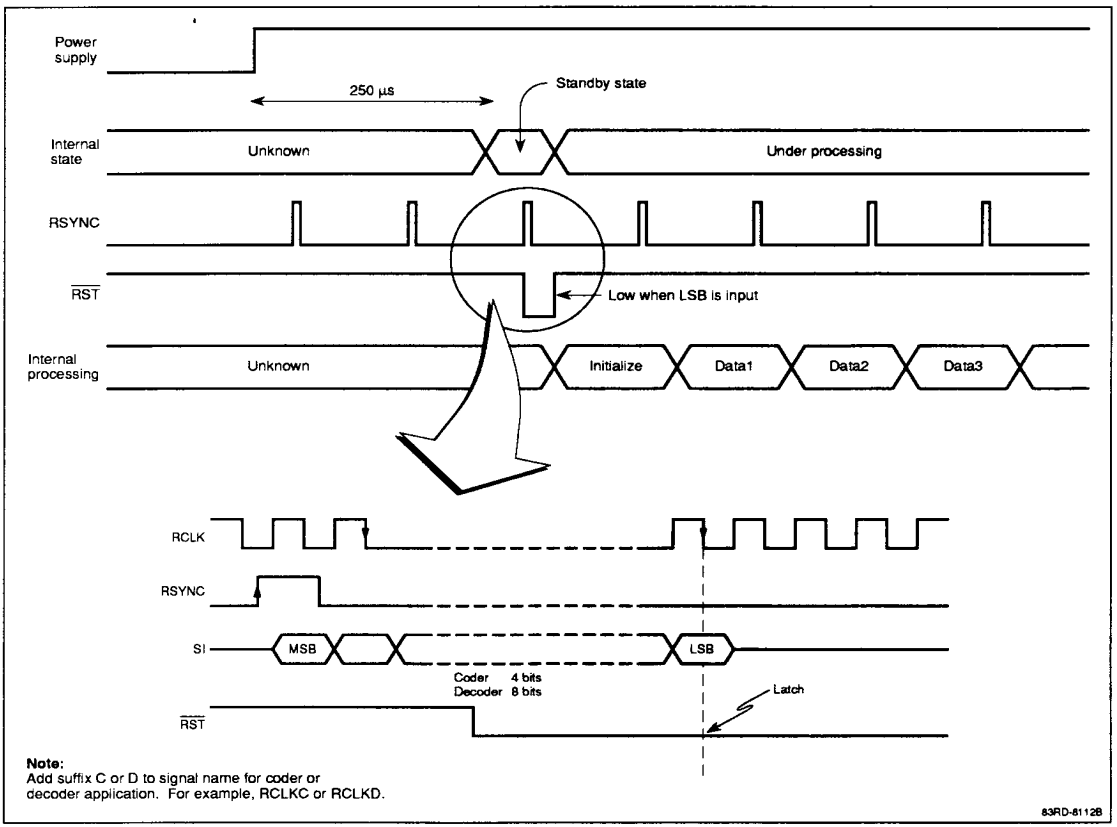


Figure 3. Power-Down Timing

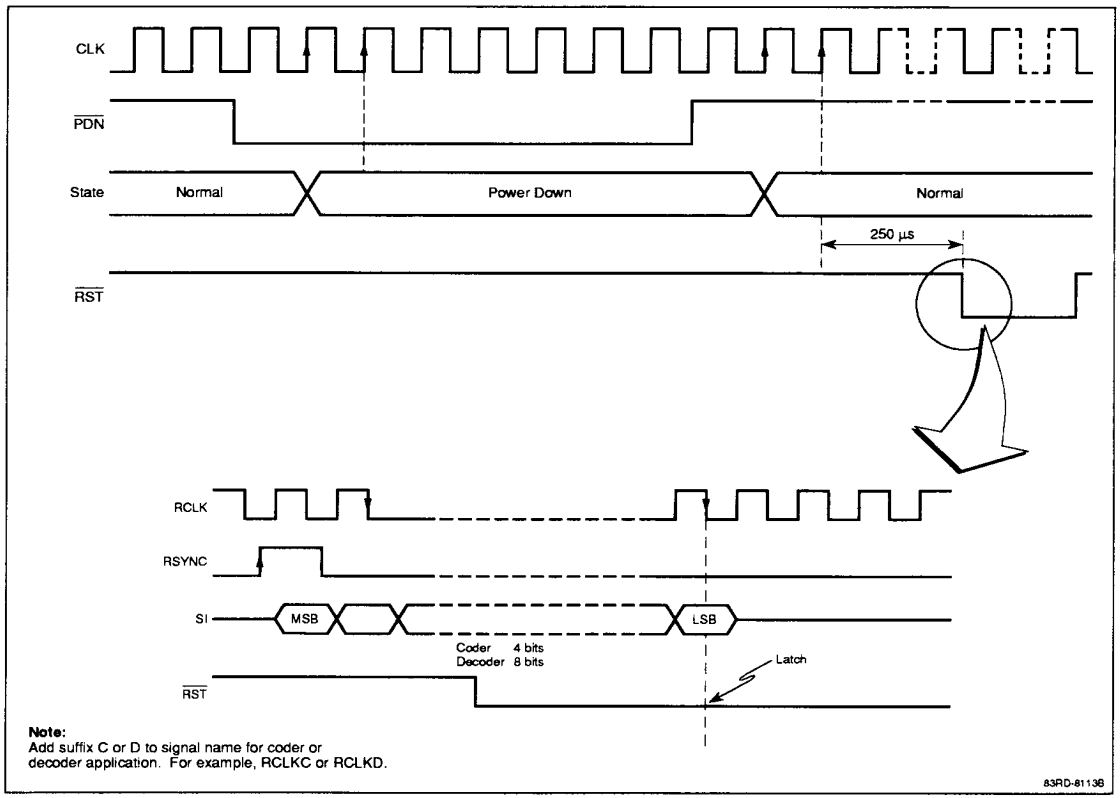


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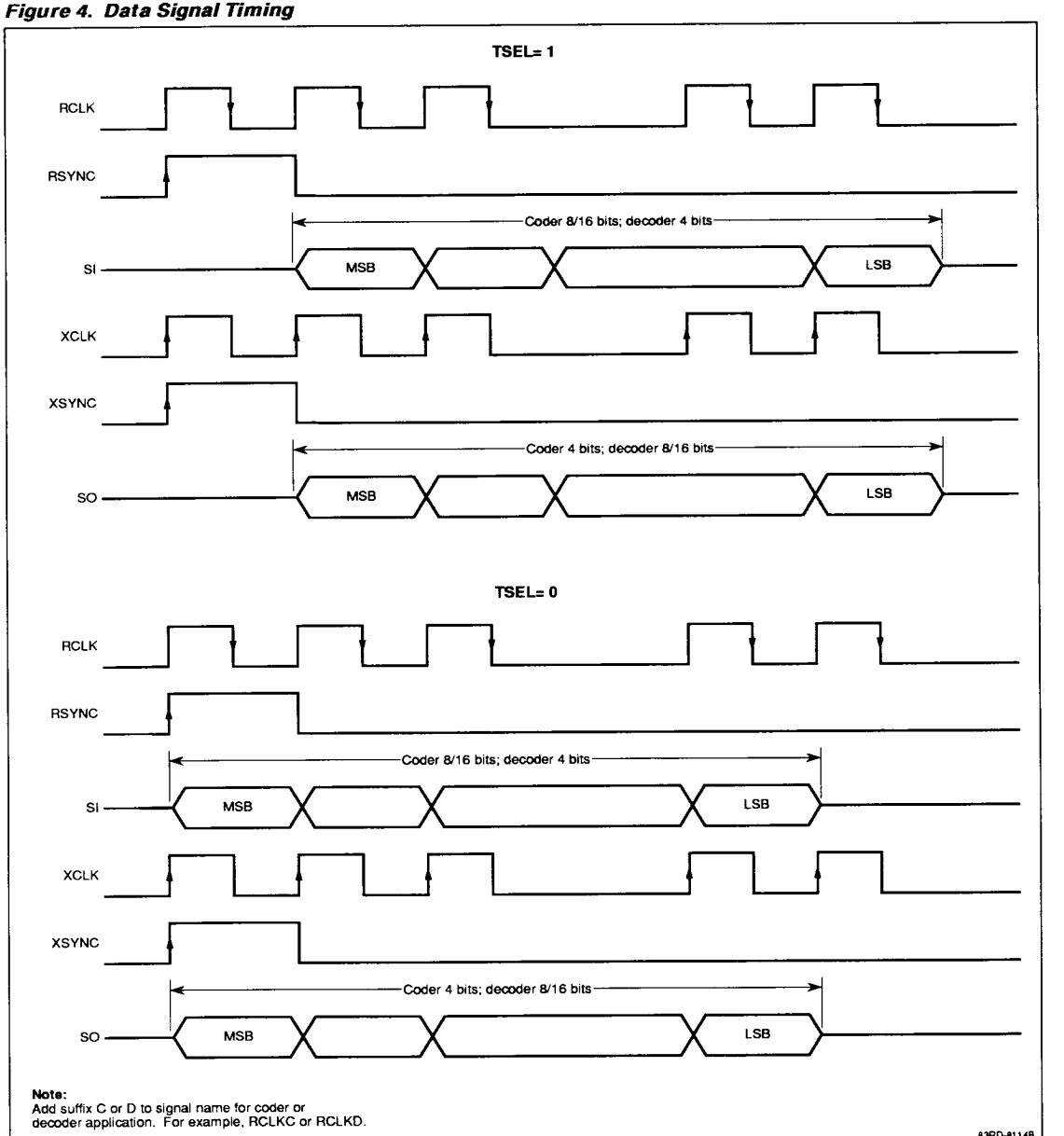
Figure 4. Data Signal Timing



Note:
Add suffix C or D to signal name for coder or decoder application. For example, RCLKC or RCLKD.

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Input-to-Output Delay

Input data to the coder or decoder is latched on the trailing edge of the receive data clock and output on the leading edge of the transmit data clock. If the clocks are synchronized, there will be a one-half clock cycle delay between data input and output.

I/O Data Format

The I/O data format at the PCM interface is coordinated with the companding characteristic of the PCM codec by connecting pins FSEL0 and FSEL1 to + 5 V (1) and GND (0) as shown below.

FSEL0	FSEL1	I/O Data Format
1	1	A-law with even-bit inverter
1	0	A-law
0	1	μ-law
0	0	16-bit linear

Muting

Pins $\overline{\text{MUTEC}}$ and $\overline{\text{MUTED}}$ control muting of the PCM signal at the coder input and decoder output, respectively. A low level at the pin cuts off the signal within 1 ms; a high level inhibits muting.

Internal Timing

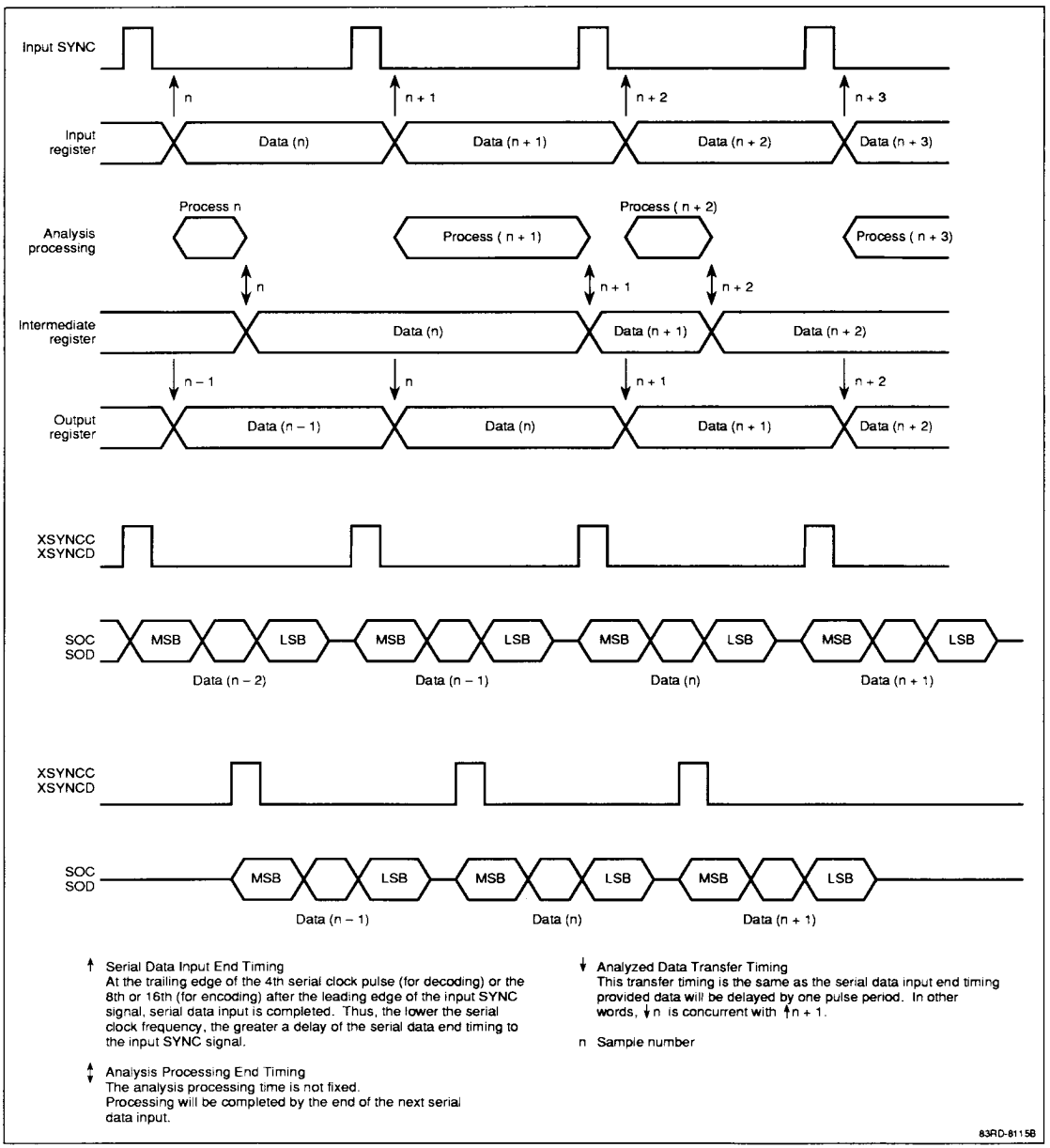
Encoding or decoding (analysis processing) starts on completion of serial data input. Processed data is immediately transferred to the intermediate register. Simultaneously, the previously processed data sample is transferred to the output register. See figure 5.

The output register contents exit serially in synchronization with the rising edge of the output SYNC signal if SYNC leads SCK, or the rising edge of serial clock SCK if SCK leads SYNC.

SYSTEM CONFIGURATION

Figure 6 is an example of a basic system with serial interfaces. The system uses the μPD9604/μPD9605 as a PCM codec and the μPD78C14 as a control CPU.

Figure 5. Processing Timing



↑ Serial Data Input End Timing
At the trailing edge of the 4th serial clock pulse (for decoding) or the 8th or 16th (for encoding) after the leading edge of the input SYNC signal, serial data input is completed. Thus, the lower the serial clock frequency, the greater a delay of the serial data end timing to the input SYNC signal.

↕ Analysis Processing End Timing
The analysis processing time is not fixed.
Processing will be completed by the end of the next serial data input.

↓ Analyzed Data Transfer Timing
This transfer timing is the same as the serial data input end timing provided data will be delayed by one pulse period. In other words, ↓n is concurrent with ↑n + 1.

n Sample number

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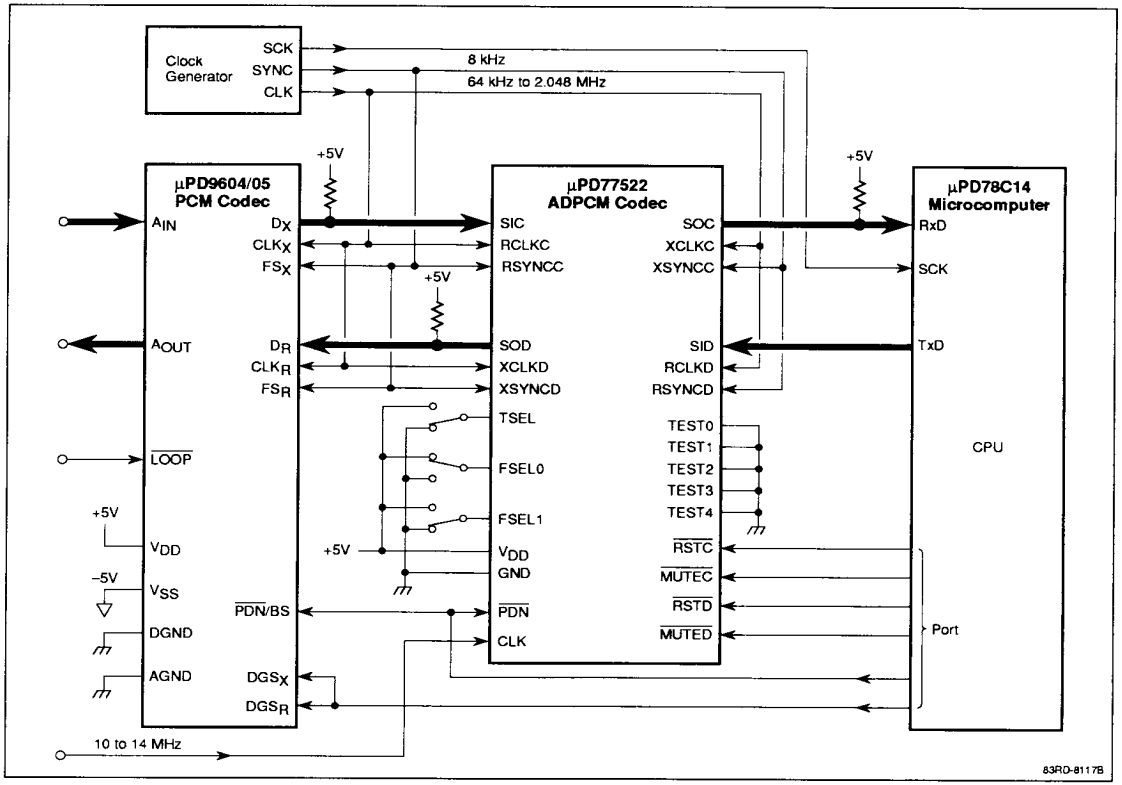
Figure 6. System Configuration



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

T_A = +25°C

Power supply voltage, V_{DD}	−0.5 to +7.0 V
Input voltage, V_I	−0.5 to V_{DD} + 0.5 V
Open drain output voltage, V_O	−0.5 to + 8.0 V
Operating temperature, T_{OPT}	−40 to +85°C
Storage temperature, T_{STG}	−65 to +150°C

Capacitance

T_A = +25°C

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_{IN}		10	pF
Output capacitance	C_{OUT}		15	pF
I/O capacitance	$C_{I/O}$		20	pF

Recommended Operating Conditions

T_A = −40 to +85°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Operating voltage	V_{DD1}	2.7		5.5	V	f_{CLK} = 10 to 11 MHz
	V_{DD2}	4.0		5.5	V	f_{CLK} = 10 to 14 MHz
Low-level input voltage	V_{IL}			0.3 V_{DD}	V	V_{DD} = 2.7 to 5.5 V
High-level input voltage	V_{IH}	0.7 V_{DD}			V	V_{DD} = 2.7 to 5.5 V

DC Characteristics

T_A = −40 to +85°C; f_{CLK} = 11 MHz; V_{DD} = 2.7 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Current consumption	I_{DD1}		20	28	mA	t_{WC} = 91 ns, V_{DD} = 5.0 V
			15	20	mA	t_{WC} = 91 ns, V_{DD} = 2.7 V
Current consumption in power down mode	I_{DD2}			100	μA	V_{DD} = 5.0 V
				70	μA	V_{DD} = 2.7 V
Low-level output voltage	V_{OL}			0.45	V	I_{OL} = 2 mA
High-level output voltage	V_{OH}	V_{DD} −0.3			V	I_{OH} = −20 μA
Low-level input leakage current	I_{IL}			10	μA	V_{IL} = 0 V
High-level input leakage current	I_{IH}			−10	μA	V_{IH} = V_{DD}

AC Characteristics

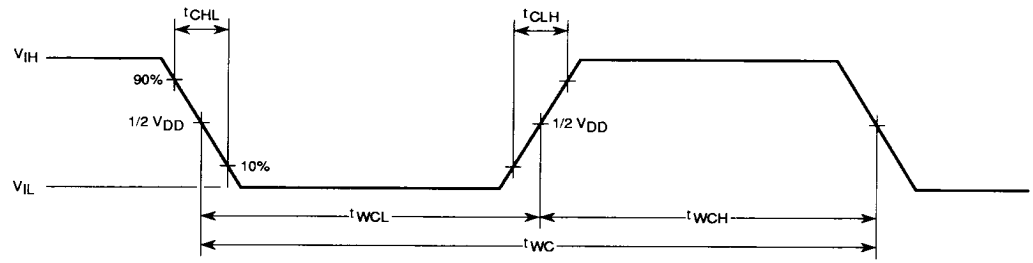
T_A = −40 to +85°C; V_{DD} = 2.7 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
CLK cycle time	t_{WC}	91		100	ns	V_{DD} = 2.7 to −5.5 V
		72		100	ns	V_{DD} = 4.0 to −5.5 V
CLK low pulse width	t_{WCL}	40		50	ns	See timing charts
CLK high pulse width	t_{WCH}	40		50	ns	
CLK rise time	t_{CLH}			10	ns	
CLK fall time	t_{CHL}			10	ns	
Transmit clock frequency	t_{XCLK}			2048	kHz	
Receive clock frequency	t_{RCLK}			2048	kHz	
Transmit sync signal frequency	t_{XSYNC}		8		kHz	
Receive sync signal frequency	t_{RSYNC}		8		kHz	
Transmit sync signal low pulse width	t_{WXSL}	1			XCLK	Measured at 1/2 V_{DD}
Transmit sync signal high pulse width	t_{WXSH}	1			XCLK	
Transmit sync signal low pulse width	t_{WRSL}	1			RCLK	
Receive sync signal high pulse width	t_{WRSH}	1			RCLK	
Transmit sync signal set time	t_{SXS}	140			ns	Measured at 1/2 V_{DD} (vs XCLK)
Transmit sync signal hold time	t_{HXS}	8			ns	
Receive sync signal set time	t_{SRS}	140			ns	Measured at 1/2 V_{DD} (vs RCLK)
Receive sync signal hold time	t_{HRS}	8			ns	
SI, RST, MUTE set time	t_{SD}	40			ns	
SI, RST, MUTE hold time	t_{HD}	8			ns	
Serial mode; SO delay time vs XSYNC ↑	t_{PDS}			90	ns	R_L = 1000 Ω; C_L = 100 pF
SO delay time vs XCLK ↑	t_{PDC}			130	ns	

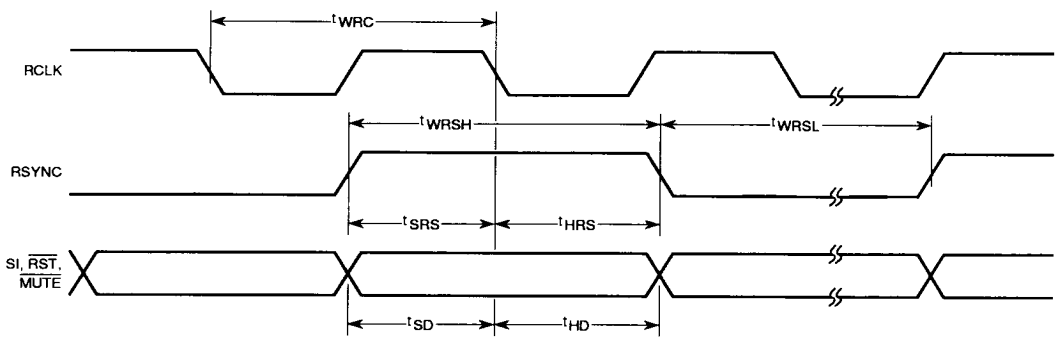
Note: The voltage at the measurement point is 1/2 V_{DD}.

Timing Waveforms

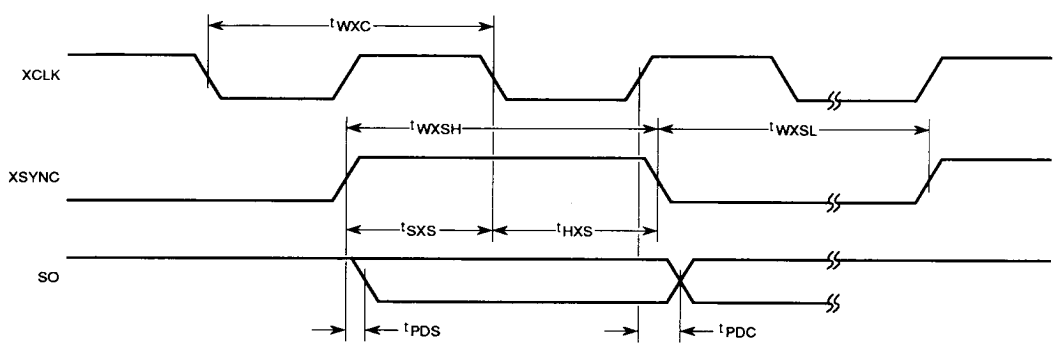
Clock Input



Serial Data Input



Serial Data Output



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