National Semiconductor

74VHC4316
Quad Analog Switch with Level Translator

General Description

These devices are digitally controlled analog switches implemented in advanced silicon-gate CMOS technology. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Three supply pins are provided on the '4316 to implement a level translator which enables this circuit to operate with 0V–6V logic levels and up to ±6V analog switch levels. The '4316 also has a common enable input in addition to each switch's control which when low will disable all switches to their off state. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

Features

- Typical switch enable time: 20 ns
- Wide analog input voltage range: ±6V
- Low "on" resistance: 50 typ. ($V_{CC}-V_{EE}=4.5V$)
  30 typ. ($V_{CC}-V_{EE}=9V$)
- Low quiescent current: 80 μA maximum (74VHC)
- Matched switch characteristics
- Individual switch controls plus a common enable
- Pin functional compatible with 74HC4316

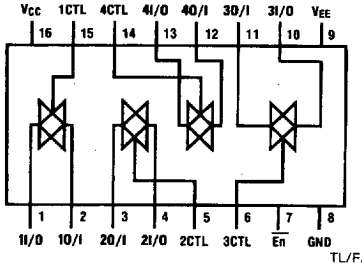
Ordering Code: See Section 6

Commercial	Package Number	Package Description
74VHC4316M	M16A	16-Lead Molded JEDEC SOIC (0.150" Wide)
74VHC4315WM	M16B	16-Lead Molded JEDEC SOIC (0.300" Wide)
74VHC4316N	N16E	16-Lead Molded DIP

Note: Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignment for SOIC and PDIP



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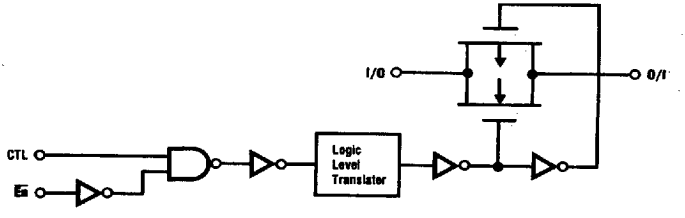
Top View

Truth Table

Inputs		Switch
$\overline{En}$	CTL	I/O–O/I
H	X	"OFF"
L	L	"OFF"
L	H	"ON"

Logic Diagram



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Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.5V
Supply Voltage (V_{EE})	+0.5 to −7.5V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Switch I/O Voltage (V_{IO})	V_{EE}−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
Supply Voltage (V_{EE})	0	−6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
74VHC	−40	+85	°C
Input Rise or Fall Times (t_r, t_f)			
V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns
V_{CC} = 12.0V		250	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A = 25°C	74VHC T_A = −40°C to +85°C		Units
					Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0V 4.5V 6.0V		1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low Level Input Voltage			2.0V 4.5V 6.0V		0.5 1.35 1.8	0.5 1.35 1.8	V
R_{ON}	Minimum "ON" Resistance (See Note 5)	V_{CTL} = V_{IH}, I_S = 2.0 mA, V_{IS} = V_{CC} to V_{EE} *(Figure 1)*	GND −4.5V −6.0V	4.5V 4.5V 6.0V	100 40 30	170 85 70	200 105 85	Ω
		V_{CTL} = V_{IH}, I_S = 2.0 mA, V_{IS} = V_{CC} or V_{EE} *(Figure 1)*	GND GND −4.5V −6.0V	2.0V 4.5V 4.5V 6.0V	100 40 50 20	180 80 60 40	215 100 75 60	
R_{ON}	Maximum "ON" Resistance Matching	V_{CTL} = V_{IH}, V_{IS} = V_{CC} to V_{EE}	GND −4.5V −6.0V	4.5V 4.5V 6.0V	10 5 5	15 10 10	20 15 15	Ω
I_{IN}	Maximum Control Input Current	V_{IN} = V_{CC} or GND	GND	6.0V		±0.1	±1.0	μA
I_{IZ}	Maximum Switch "OFF" Leakage Current	V_{OS} = V_{CC} or V_{EE}, V_{IS} = V_{EE} or V_{CC}, V_{CTL} = V_{IL} *(Figure 2)*	GND −6.0V	6.0V 6.0V		±30 ±50	±300 ±500	nA
I_{IZ}	Maximum Switch "ON" Leakage Current	V_{IS} = V_{CC} to V_{EE}, V_{CTL} = V_{IH}, V_{OS} = OPEN *(Figure 3)*	GND −6.0V	6.0V 6.0V		±20 ±30	±75 ±150	nA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA	GND −6.0V	6.0V 6.0V		1.0 4.0	10 40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for VHC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.

Note 5: At supply voltages (V_{CC}–V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics

V_{CC} = 2.0V–6.0V, V_{EE} = 0V–6V, C_L = 50 pF unless otherwise specified

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	$T_A = +25°C$		74VHC $T_A = -40°C$ to $+85°C$	Units
					Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		GND	3.3V	15	30	37	ns
			GND	4.5V	5	10	13	
			−4.5V	4.5V	4	8	12	
			−6.0V	6.0V	3	7	11	
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay (Control)	$R_L = 1\ k\Omega$	GND	3.3V	25	97	120	ns
			GND	4.5V	20	35	43	
			−4.5V	4.5V	15	32	39	
			−6.0V	6.0V	14	30	37	
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay (Control)	$R_L = 1\ k\Omega$	GND	3.3V	35	145	180	ns
			GND	4.5V	25	50	63	
			−4.5V	4.5V	20	44	55	
			−6.0V	6.0V	20	44	55	
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay (Enable)		GND	3.3V	27	120	150	ns
			GND	4.5V	20	41	52	
			−4.5V	4.5V	19	38	48	
			−6.0V	6.0V	18	36	45	
t_{PLZ}, t_{PHZ}	Maximum Switch Turn "OFF" Delay (Enable)		GND	3.3V	42	155	190	ns
			GND	4.5V	28	53	67	
			−4.5V	4.5V	23	47	59	
			−6.0V	6.0V	21	47	59	
	Minimum Frequency Response *(Figure 7)* 20 log (V_{OS}/V_{IS}) = −3 dB	$R_L = 600\Omega$, $V_{IS} = 2V_{PP}$ at ($V_{CC}-V_{EE}/2$) (Notes 6, 7)	0V	4.5	40			MHz
			−4.5V	4.5V	100			
	Control to Switch Feedthrough Noise *(Figure 8)*	$R_L = 600\Omega$, F = 1 MHz C_L = 50 pF (Notes 7, 8)	0V	4.5V	100			mV
			−4.5V	4.5V	250			
	Crosstalk Between any Two Switches *(Figure 9)*	$R_L = 600\Omega$, F = 1 MHz	0V	4.5V	−52			dB
			−4.5V	4.5V	−50			
	Switch OFF Signal Feedthrough Isolation *(Figure 10)*	$R_L = 600\Omega$, F = 1 MHz $V_{CTL} = V_{IL}$, (Notes 7, 8)	0V	4.5V	−42			dB
			−4.5V	4.5V	−44			
THD	Sinewave Harmonic Distortion *(Figure 11)*	R_L = 10 KΩ, C_L = 50 pF, F = 1 KHz $V_{IS} = 4\ V_{PP}$	0V	4.5V	0.013			%
		$V_{IS} = 8\ V_{PP}$	−4.5V	4.5V	0.008			
C_{IN}	Maximum Control Input Capacitance				5			pF
C_{IN}	Maximum Switch Input Capacitance				35			pF
C_{IN}	Maximum Feedthrough Capacitance	V_{CTL} = GND			0.5			pF
C_{PD}	Power Dissipation Capacitance				15			pF

Note 6: Adjust 0 dBm for F = 1 kHz (Null R_L/Ron Attenuation).

Note 7: V_{IS} is centered at $V_{CC}-V_{EE}/2$.

Note 8: Adjust for 0 dBm.

AC Test Circuits and Switching Time Waveforms

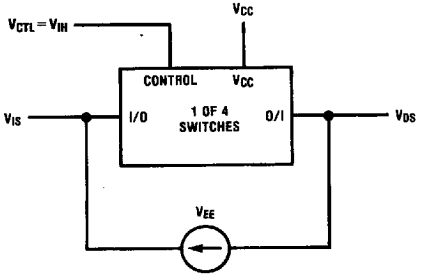

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FIGURE 1. "ON" Resistance

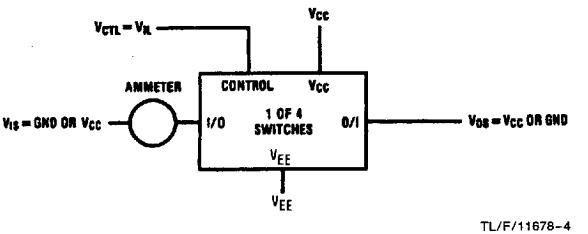

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FIGURE 2. "OFF" Channel Leakage Current

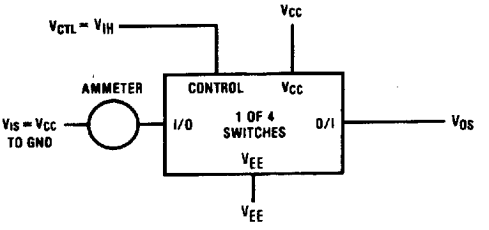

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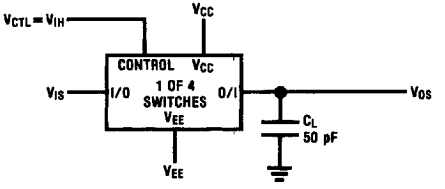
FIGURE 3. "ON" Channel Leakage Current



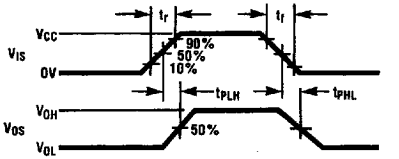


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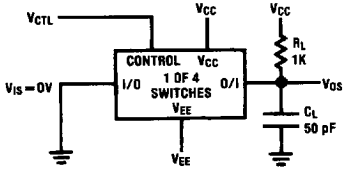
FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output



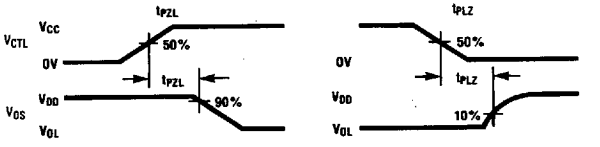


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FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

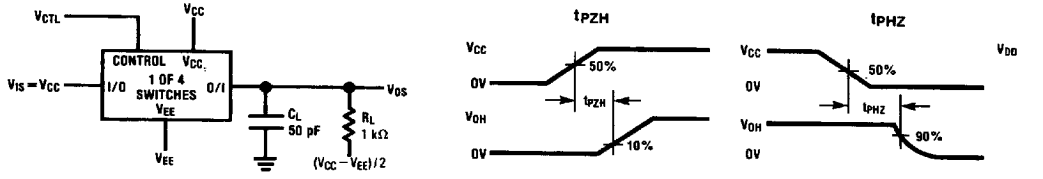

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FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

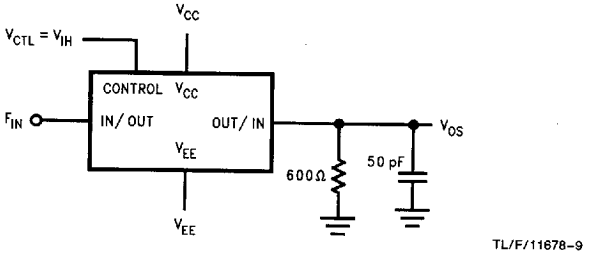

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FIGURE 7. Frequency Response

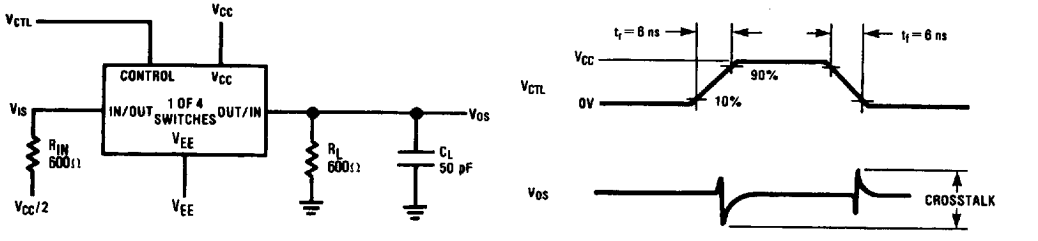

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FIGURE 8. Crosstalk: Control Input to Signal Output

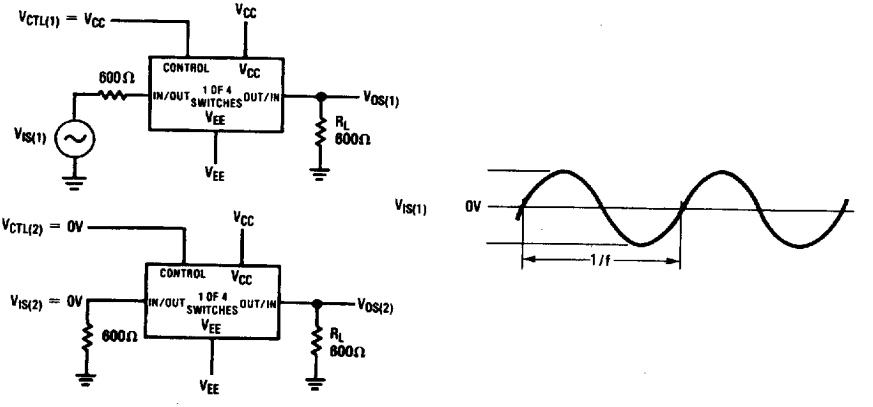

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FIGURE 9: Crosstalk between Any Two Switches

AC Test Circuits and Switching Time Waveforms (Continued)

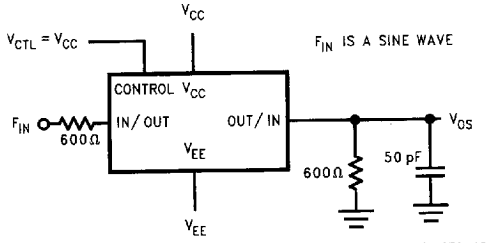


FIGURE 10. Switch OFF Signal Feedthrough Isolation

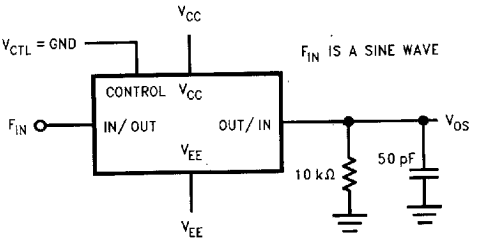
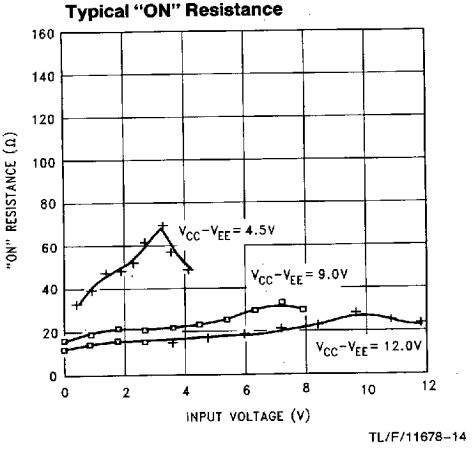
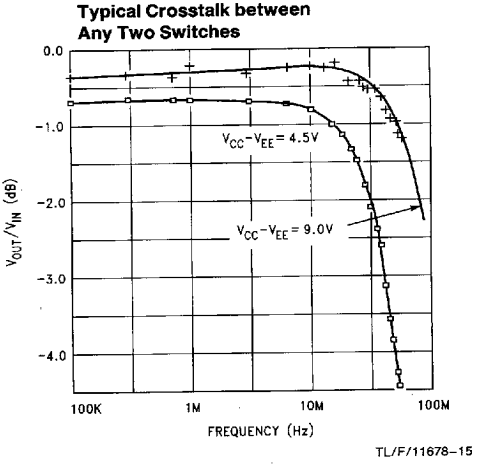
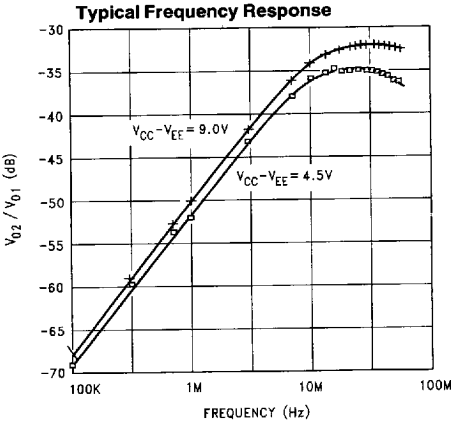


FIGURE 11. Sinewave Distortion

Typical Performance Characteristics







Special Considerations

In certain applications the external load-resistor current may include both V_{CC} and signal line components. To avoid drawing V_{CC} current when switch current flows into the analog switch input pins, the voltage drop across the switch must not exceed 0.6V (calculated from the ON resistance).