4M×4 CMOS Synchronous DRAM
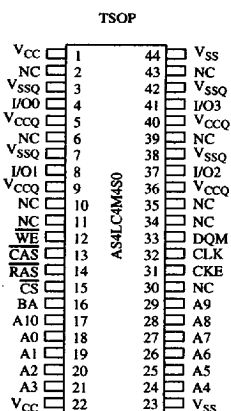
Advance information

Features

- Organization: 2,097,152 words × 4 bits × 2 banks
- All signals reference to positive edge of clock
- Dual internal banks (controlled by BA)
- High speed
  - 100/83/66 MHz bus speeds
  - 8/10/12 ns clock access time
- Low power consumption
  - Active: 540 mW max
  - Standby: 7.2 mW max, CMOS I/O
- 4096 refresh cycles, 64 ms refresh interval
- Auto refresh and self refresh
- Automatic and direct precharge

- Burst read/write, single write
- Can assert random column address in every cycle
- LVTTL compatible I/O
- 3.3V power supply
- JEDEC standard package, pinout and function
  - 400 mil, 44-pin TSOP type 2
- Read/write data masking
- Programmable burst length (1/2/4/8)
- Programmable burst sequence (sequential/interleaved)
- Programmable $\overline{CAS}$ latency (1/2/3)
- Latch-up current ≥ 200 mA
- ESD protection ≥ 2000 mA

Pin arrangement

TSOP

V$_{CC}$	1	44	V$_{SS}$
NC	2	43	NC
V$_{SSQ}$	3	42	V$_{SSQ}$
I/O0	4	41	I/O3
V$_{CCQ}$	5	40	V$_{CCQ}$
NC	6	39	NC
V$_{SSQ}$	7	38	V$_{SSQ}$
I/O1	8	37	I/O2
V$_{CCQ}$	9	36	V$_{CCQ}$
NC	10	35	NC
NC	11	34	NC
$\overline{WE}$	12	33	DQM
$\overline{CAS}$	13	32	CLK
$\overline{RAS}$	14	31	CKE
$\overline{CS}$	15	30	NC
BA	16	29	A9
A10	17	28	A8
A0	18	27	A7
A1	19	26	A6
A2	20	25	A5
A3	21	24	A4
V$_{CC}$	22	23	V$_{SS}$

(AS4LC4M4S0)

Pin designation

Pin(s)	Description
DQM	I/O mask
A0 to A10	Address inputs
BA	Bank address
I/O0 to I/O3	Input/output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V$_{CC}$, V$_{CCQ}$	Power (3.3V ± 0.3V)
V$_{SS}$, V$_{SSQ}$	Ground
CLK	Clock input
CKE	Clock enable

DRAM

Selection guide

	Symbol	4LC4M4S0-10	4LC4M4S0-12	4LC4M4S0-15	Unit
Bus frequency (CL = 3)	f_{max}	100	83.3	66.6	MHz
Maximum clock access time (CL = 3)	t_{AC}	8	10	12	ns
Minimum input setup time	t_S	2.5	3.0	3.0	ns
Minimum input hold time	t_H	1	1.5	1.5	ns
Minimum row cycle time	t_{RC}	90	108	120	ns
Maximum operating current (burst, CL = 3)	I_{CC1}	150	125	100	mA
Maximum CMOS standby current, self refresh	I_{CC6}	2	2	2	mA

9003449 0000965 688

Functional description

The AS4LC4M4S0 is a high performance 16 megabit CMOS Synchronous Dynamic Random Access Memory (SDRAM) organized as 2,097,152 words × 4 bits × 2 banks. Very high bandwidth is achieved using a pipelined architecture where all inputs and outputs are referenced to the rising edge of a common clock. Programmable burst mode can be used to read up to 8 nibbles of data without selecting a new column address. Burst mode allows a 4-bit data word to be output during each clock cycle for a peak data bandwidth of 267 megabits per second at 66 MHz.

The AS4LC4M4S0 also includes two internal banks that can be alternately accessed (read or write) at the maximum clock frequency for seamless interleaving operations. This provides a significant advantage over asynchronous EDO and fast page mode devices.

This SDRAM product also features a programmable mode register, allowing users to select read latency as well as burst length and type (sequential or interleaved). Lower latency improves first data access in terms of CLK cycles, while higher latency improves maximum frequency of operation. This feature enables flexible performance optimization for a variety of applications.

SDRAM commands and functions are decoded from control inputs. Basic commands are as follows:

- Mode register set
- De-activate bank
- Deactivate all banks
- Select row, activate bank
- Select column, write
- Select column, read
- CBR refresh
- Self refresh
- Deselect, power down (CKE)
- Auto-precharge with read/write

The AS4LC4M4S0 is available in 44-pin plastic TSOP type 2 package and operates with a power supply of 3.3V ± 0.3V. Multiple power and ground pins are provided for low switching noise and EMI. Inputs and outputs are LVTTL compatible.

Logic block diagram

■ 9003449 0000966 514 ■