



Description

The GM71C16100C is the new generation dynamic RAM organized 16,777,216 x 1 Bit. GM71C16100C has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71C16100C offers Fast Page Mode as a high speed access mode. Multiplexed address inputs permit the GM71C16100C to be packaged in a standard 300 mil 24(26) pin SOJ. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply 5V_i±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

Features

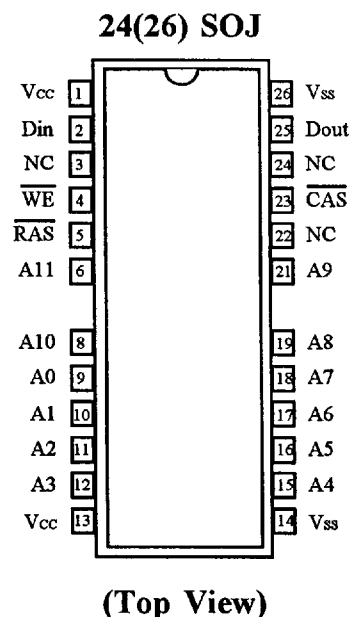
- 16,777,216 Words x 1 Bit
- Fast Page Mode Capability
- Single Power Supply (5V_i±10%)
- Fast Access Time & Cycle Time

(Unit: ns)

	t _{TRAC}	t _{CAC}	t _{RC}	t _{PC}
GM71C16100C-5	50	13	90	35
GM71C16100C-6	60	15	110	40
GM71C16100C-7	70	18	130	45

- Low Power
Active : 495/440/385mW (MAX)
Standby : 11mW (CMOS level : MAX)
- $\overline{\text{RAS}}$ Only Refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 4096 Refresh Cycles/64 μ s
- Test function : 16-bit parallel test mode

Pin Configuration



Pin Description

Pin	Function	Pin	Function
A0-A11	Address Inputs	$\overline{WE}$	Read/Write Enable
A0-A11	Refresh Address Inputs	DOUT	Data Output
DIN	Data Input	NC	No Connection
$\overline{RAS}$	Row Address Strobe	V _{CC}	Power (+5V)
$\overline{CAS}$	Column Address Strobe	V _{SS}	Ground

Ordering Information

Type No.	Access Time	Package
GM71C16100CJ-5 GM71C16100CJ-6 GM71C16100CJ-7	50\$Å 60\$Å 70\$Å	300 Mil 24(26) Pin Plastic SOJ

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T _A	Ambient Temperature under Bias	0 ~ 70	°C
T _{STG}	Storage Temperature (Plastic)	-55 ~ 125	°C
V _{IN/OUT}	Voltage on any Pin Relative to V _{SS}	-1.0 ~ 7.0	V
V _{CC}	Voltage on V _{CC} Relative to V _{SS}	-1.0 ~ 7.0	V
I _{OUT}	Short Circuit Output Current	50	mA
P _D	Power Dissipation	1.0	W

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended DC Operating Conditions (T_A = 0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.4	-	6.5	V
V _{IL}	Input Low Voltage	-1.0	-	0.8	V

DC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$, $T_A = 0 \sim 70^\circ\text{C}$)

Symbol	Parameter	Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage ($I_{OH} = -5\text{mA}$)	2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage ($I_{OL} = 4.2\text{mA}$)	0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC \min}$)	50 μA	-	90	μA 1, 2
		60 μA	-	80	
		70 μA	-	70	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS} = V_{IH}$, $D_{OUT} = \text{High-Z}$)	-	2	μA	
I_{CC3}	$\overline{RAS}$ -Only Refresh Current Average Power Supply Current $\overline{RAS}$ -Only Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC \min}$)	50 μA	-	90	μA 2
		60 μA	-	80	
		70 μA	-	70	
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC \min}$)	50 μA	-	80	μA 1, 3
		60 μA	-	70	
		70 μA	-	60	
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS} = V_{CC} - 0.2V$, $D_{OUT} = \text{High-Z}$)	-	1	μA	
I_{CC6}	$\overline{CAS}$ -before- $\overline{RAS}$ Refresh Current ($t_{RC} = t_{RC \min}$)	50 μA	-	90	μA
		60 μA	-	80	
		70 μA	-	70	
I_{CC7}	Standby Current $\overline{RAS} = V_{IH}$ $\overline{CAS} = V_{IL}$ $D_{OUT} = \text{Enable}$	-	5	μA	1
$I_{L(I)}$	Input Leakage Current Any Input ($0V_i \sim V_{DD} \pm 6V$)	-10	10	μA	
$I_{L(O)}$	Output Leakage Current (D_{OUT} is Disabled, $0V_i \sim V_{DD} \pm 6V$)	-10	10	μA	

Note: 1. I_{CC} depends on output load condition when the device is selected.

$I_{CC}(\text{max})$ is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.

3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

Capacitance ($V_{CC} = 5V \pm 10\%$, $T_A = 25^\circ\text{C}$)

Symbol	Parameter	Min	Max	Unit	Note
C_{II}	Input Capacitance (Address)	-	5	μF	1
C_{I2}	Input Capacitance (Clocks)	-	7	μF	1
C_O	Output Capacitance (Data-Out)	-	7	μF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{\text{CAS}} = V_{IH}$ to disable D_{OUT} .

AC Characteristics ($V_{CC} = 5V \pm 10\%$, $T_A = 0 \sim 70^\circ\text{C}$, Notes 1, 2, 17)

Test Conditions

Input rise and fall times: 5Ω

Input timing reference levels: 0.8V, 2.4V

Output timing reference levels: 0.4V, 2.4V

Output timing reference levels: 0.4V, 2.4V

Output load : 2 TTL gate + C_L (100 μF)

(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71C16100 C-5		GM71C16100 C-6		GM71C16100 C-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	90	-	110	-	130	-	ns	
t_{RP}	$\overline{\text{RAS}}$ Precharge Time	30	-	40	-	50	-	ns	
t_{CP}	$\overline{\text{CAS}}$ Precharge Time	7	-	10	-	10	-	ns	
t_{RAS}	$\overline{\text{RAS}}$ Pulse Width	50	10,000	60	10,000	70	10,000	ns	
t_{CAS}	$\overline{\text{CAS}}$ Pulse Width	13	10,000	15	10,000	18	10,000	ns	
t_{ASR}	Row Address Set up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	7	-	10	-	10	-	ns	
t_{ASC}	Column Address Set-up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	7	-	10	-	15	-	ns	
t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	17	45	20	45	20	52	ns	3
t_{RAD}	$\overline{\text{RAS}}$ to Column Address Delay Time	12	30	15	30	15	35	ns	4
t_{RSH}	$\overline{\text{RAS}}$ Hold Time	13	-	15	-	18	-	ns	
t_{CSH}	$\overline{\text{CAS}}$ Hold Time	50	-	60	-	70	-	ns	
t_{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	5	-	5	-	5	-	ns	
t_t	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	5

Read Cycle

Symbol	Parameter	GM71C16100 C-5		GM71C16100 C-6		GM71C16100 C-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{RAC}	Access Time from $\overline{\text{RAS}}$	-	50	-	60	-	70	ns	6,7,16
t _{CAC}	Access Time from $\overline{\text{CAS}}$	-	13	-	15	-	18	ns	7,8,15,16
t _{AA}	Access Time from Address	-	25	-	30	-	35	ns	7,9,16,17
t _{RCS}	Read Command Setup Time	0	-	0	-	0	-	ns	
t _{RCH}	Read Command Hold Time to $\overline{\text{CAS}}$	0	-	0	-	0	-	ns	10
t _{RRH}	Read Command Hold Time to $\overline{\text{RAS}}$	5	-	5	-	5	-	ns	10
t _{RAL}	Column Address to $\overline{\text{RAS}}$ Lead Time	25	-	30	-	35	-	ns	
t _{CAL}	Column Address to $\overline{\text{CAS}}$ Lead Time	25	-	30	-	35	-	ns	
t _{CLZ}	$\overline{\text{CAS}}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t _{OH}	Output Data Hold Time	3	-	3	-	3	-	ns	
t _{OFF}	Output Buffer Turn-off Time	-	13	-	15	-	15	ns	11

Write Cycle

Symbol	Parameter	GM71C16100 C-5		GM71C16100 C-6		GM71C16100 C-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{WCS}	Write Command Setup Time	0	-	0	-	0	-	ns	12
t _{WCH}	Write Command Hold Time	7	-	10	-	15	-	ns	
t _{WP}	Write Command Pulse Width	7	-	10	-	10	-	ns	
t _{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	13	-	15	-	18	-	ns	
t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	13	-	15	-	18	-	ns	
t _{DS}	Data-in Setup Time	0	-	0	-	0	-	ns	13
t _{DH}	Data-in Hold Time	7	-	10	-	15	-	ns	13

Read-Modify-Write Cycle

Symbol	Parameter	GM71C16100 C-5		GM71C16100 C-6		GM71C16100 C-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{RWC}	Read-Modify-Write Cycle Time	107	-	130	-	153	-	ns	
t _{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	50	-	60	-	70	-	ns	12
t _{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	13	-	15	-	18	-	ns	12
t _{AWD}	Column Address to $\overline{\text{WE}}$ Delay Time	25	-	30	-	35	-	ns	12

Refresh Cycle

Symbol	Parameter	GM71C16100 C-5		GM71C16100 C-6		GM71C16100 C-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{CSR}	$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	5	-	5	-	5	-	§A	
t _{CHR}	$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	10	-	10	-	10	-	§A	
t _{WRP}	$\overline{\text{WE}}$ Setup Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	0	-	0	-	0	-	§A	
t _{WRH}	$\overline{\text{WE}}$ Hold Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	10	-	10	-	10	-	§A	
t _{RPC}	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	5	-	5	-	5	-	§A	

Fast Page Mode Cycle

Symbol	Parameter	GM71C16100 C-5		GM71C16100 C-6		GM71C16100 C-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{PC}	Fast Page Mode Cycle Time	35	-	40	-	45	-	§A	
t _{RASP}	Fast Page Mode $\overline{\text{RAS}}$ Pulse Width	-	100,000	-	100,000	-	100,000	§A	14
t _{ACP}	Access Time from $\overline{\text{CAS}}$ Precharge	-	30	-	35	-	40	§A	7,15,16
t _{RHCP}	$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	30	-	35	-	40	-	§A	

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	GM71C16100 C-5		GM71C16100 C-6		GM71C16100 C-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	52	-	60	-	68	-	§Å	
t _{CPW}	$\overline{\text{WE}}$ Delay Time from $\overline{\text{CAS}}$ Precharge	30	-	35	-	40	-	§Å	12

Test Mode Cycle*18

Symbol	Parameter	GM71C16100 C-5		GM71C16100 C-6		GM71C16100 C-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{WTS}	Test Mode $\overline{\text{WE}}$ Setup Time	0	-	0	-	0	-	ns	
t _{WTH}	Test Mode $\overline{\text{WE}}$ Hold Time	10	-	10	-	10	-	ns	

Notes:

1. AC Measurements assume $t_r = 5\text{§Å}$.
2. An initial pause of 200§Å is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles are required.
3. Operation with the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RCD}}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
4. Operation with the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RAD}}(\text{max})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
5. $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$.
6. Assume that $t_{\text{RCD}} \hat{=} t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \hat{=} t_{\text{RAD}}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 2 TTL loads and 100§Ü .
8. Assume that $t_{\text{RCD}} \hat{=} t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \hat{=} t_{\text{RAD}}(\text{max})$.
9. Assume that $t_{\text{RCD}} \hat{=} t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \hat{=} t_{\text{RAD}}(\text{max})$.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.

11. $t_{OFF}(\max)$ and $t_{OEZ}(\max)$ define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
12. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}(\min)$, the cycles is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\min)$, the $t_{CWD} \geq t_{CWD}(\min)$, and $t_{AWD} \geq t_{AWD}(\min)$, or $t_{CWD} \geq t_{CWD}(\min)$, $t_{AWD} \geq t_{AWD}(\min)$ and $t_{CPW} \geq t_{CPW}(\min)$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
14. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
15. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}
16. The 16M DRAM offers a 16-bit time saving parallel test mode. Address CA0 and CA1, CA10 and CA11 for the 16M x 1 are don't care during test mode. Test mode is set by performing a $\overline{WE}$ -and- $\overline{CAS}$ -before- $\overline{RAS}$ (WCBR) cycle. In 16-bit parallel test mode, data is written into 16 bits in parallel at Din and read out from Dout. If 16 bits are equal (all 1s or 0s), data output pin is high state during test mode read cycle, then the device has passed. If they are not equal, data output pin is a low state, then the device has failed. Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles. To get out of test mode and enter a normal operation mode, perform either a regular $\overline{CAS}$ -before- $\overline{RAS}$ refresh cycle or $\overline{RAS}$ -only refresh cycle.
17. In a test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} and t_{ACP} is delayed by 2 μ s to 5 μ s for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

Timing Waveforms

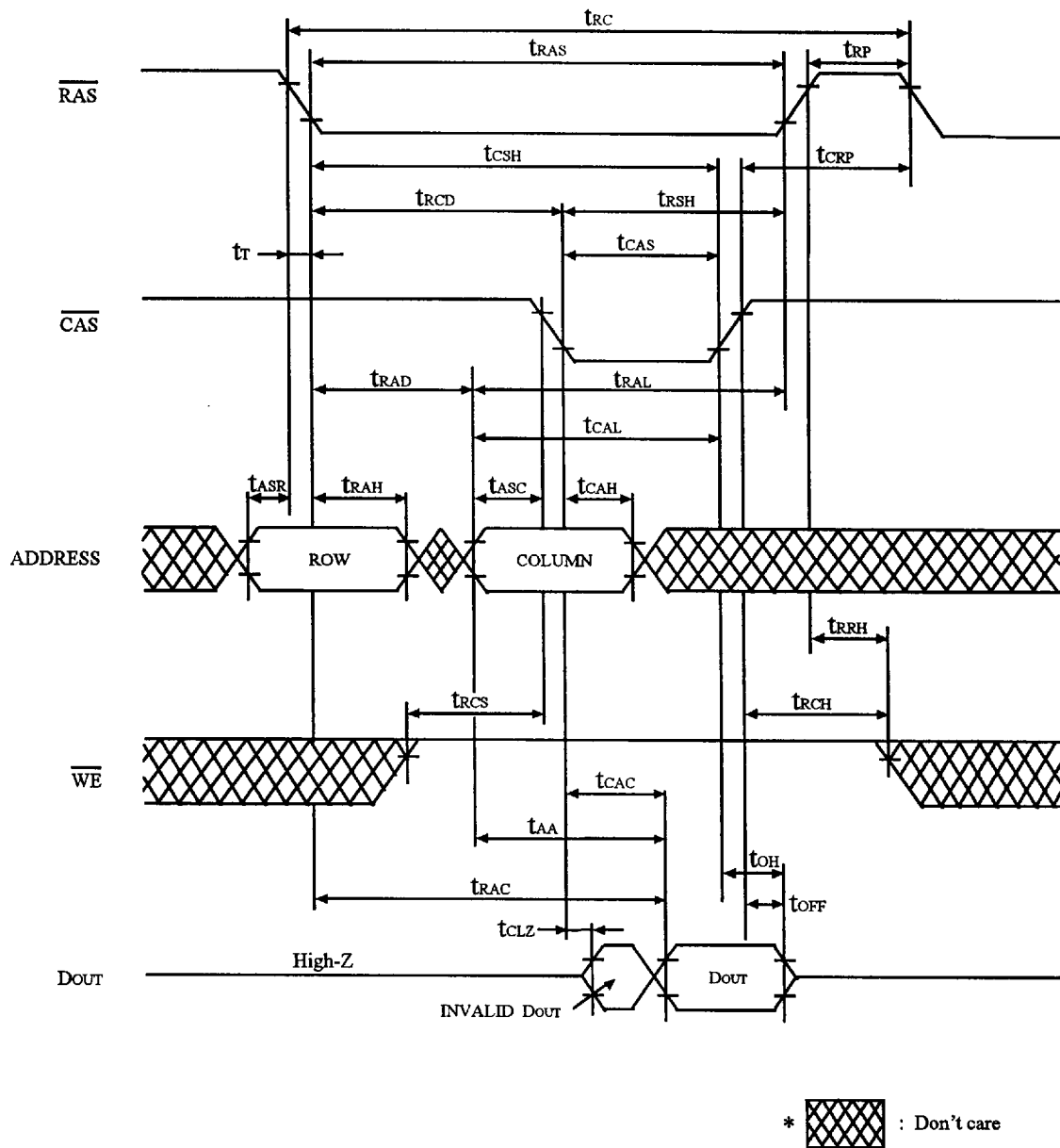
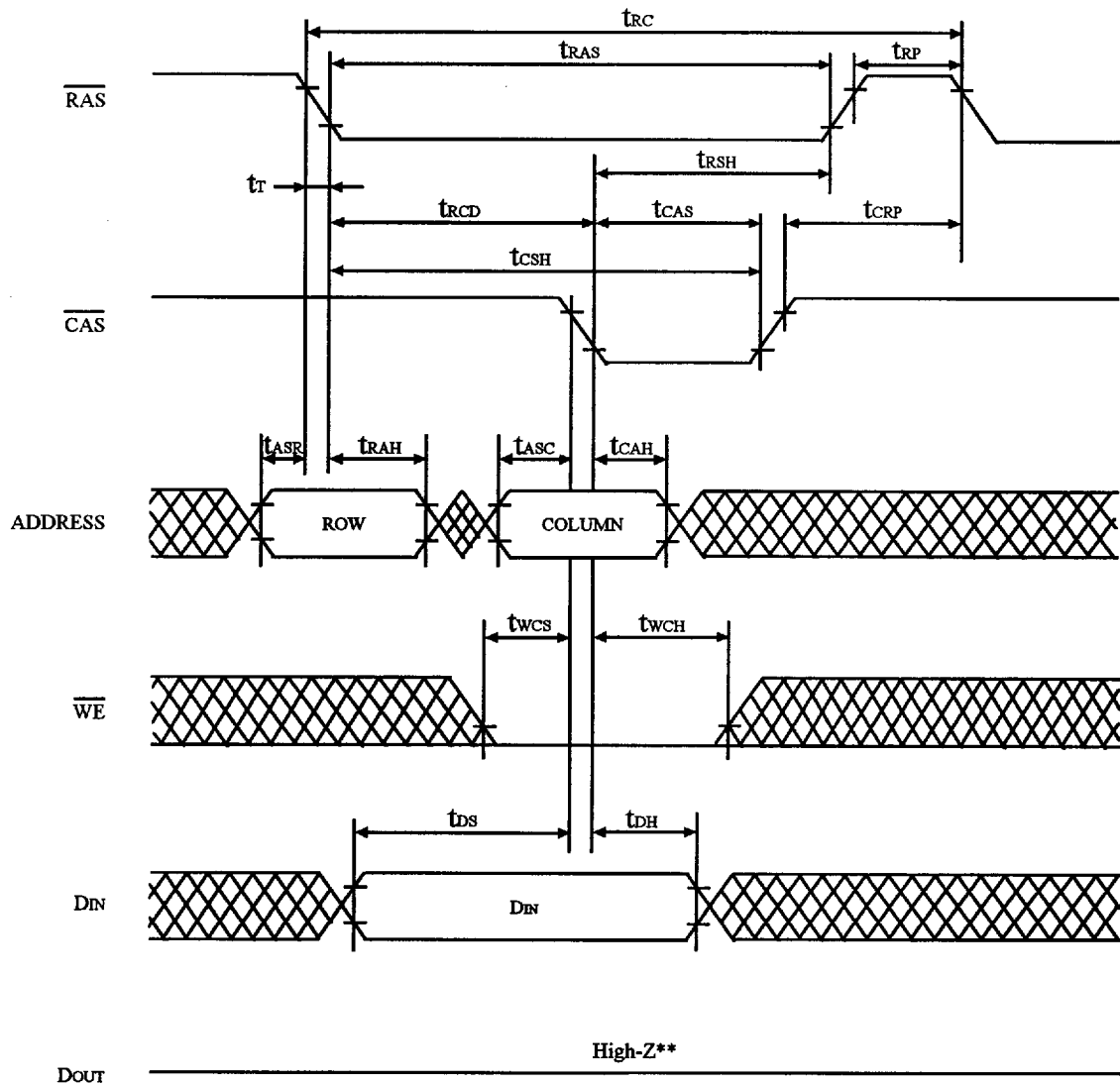


FIGURE 1. READ CYCLE



*  : Don't care

** $t_{WCS} \geq t_{WCS}(\min)$

FIGURE 2. EARLY WRITE CYCLE

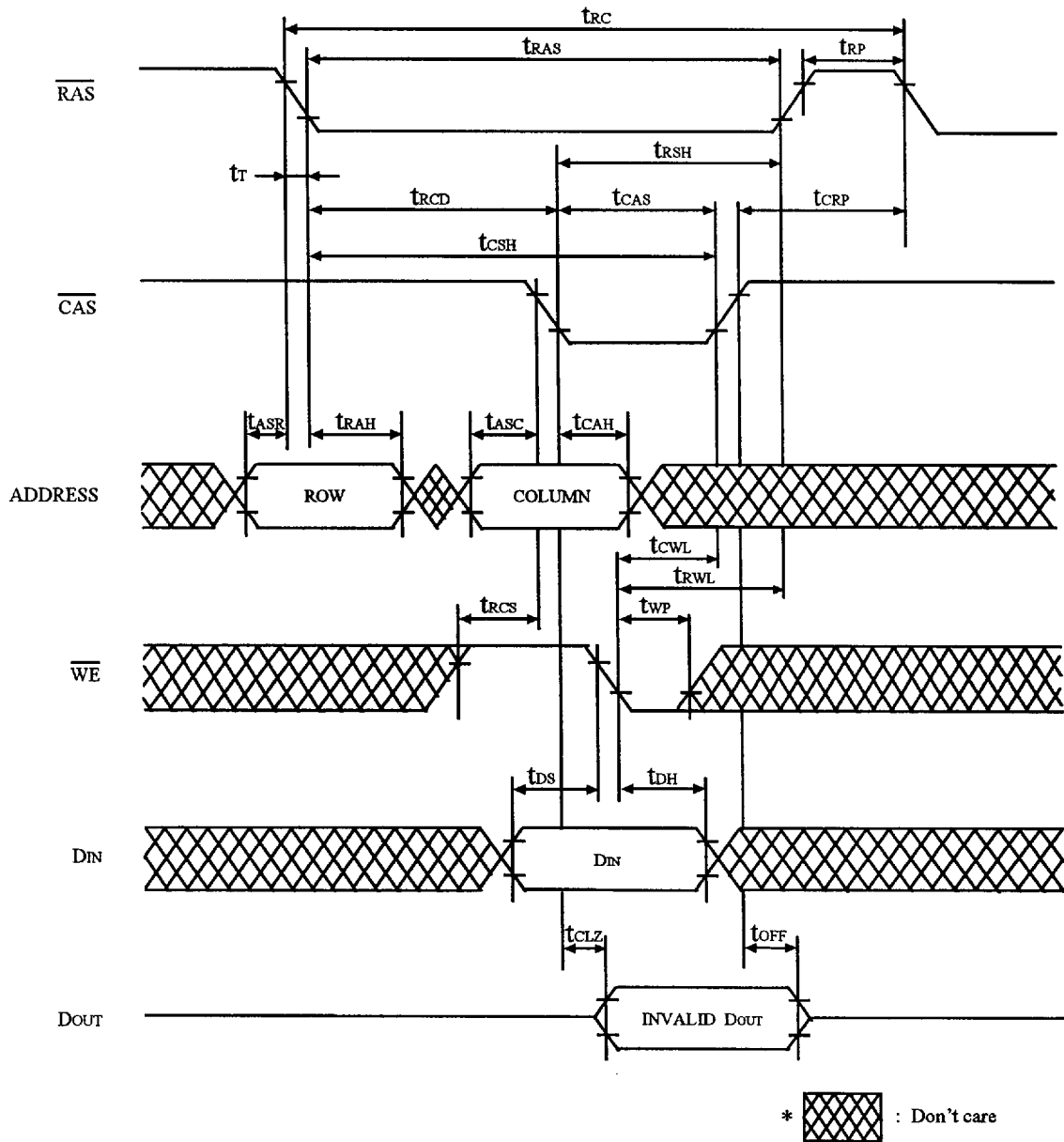


FIGURE 3. DELAYED WRITE CYCLE

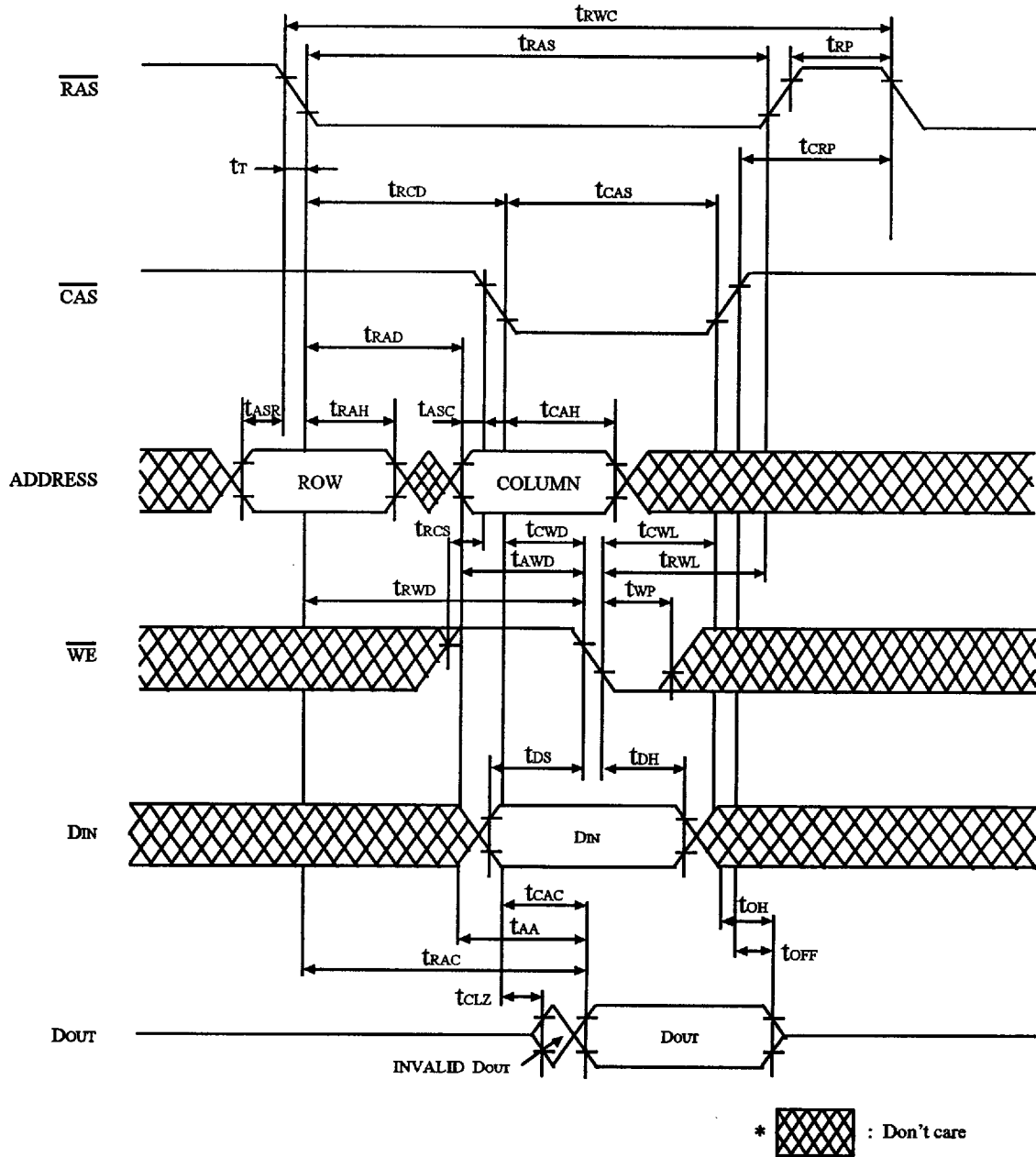


FIGURE 4. READ MODIFY WRITE CYCLE

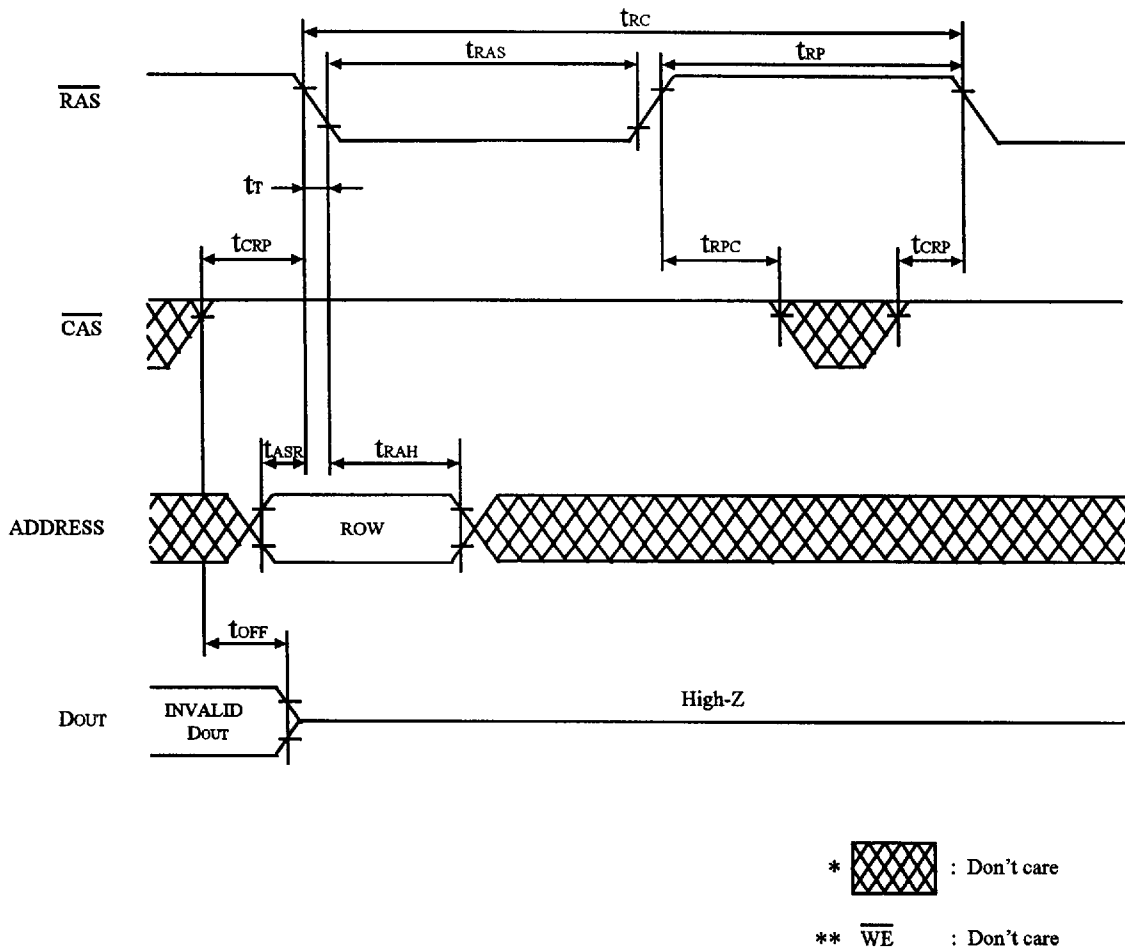
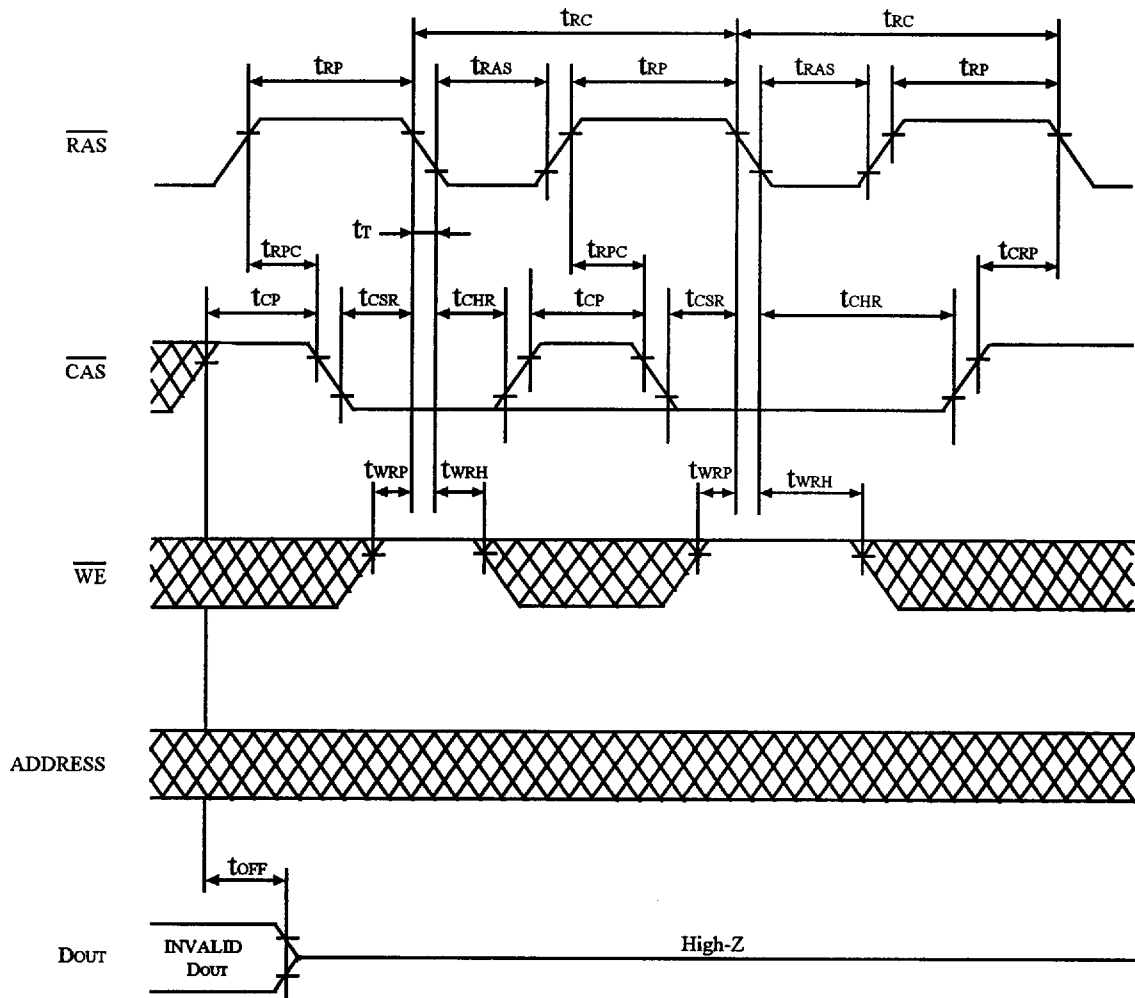


FIGURE 5. $\overline{\text{RAS}}$ ONLY REFRESH CYCLE



*  : Don't care

FIGURE 6. $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

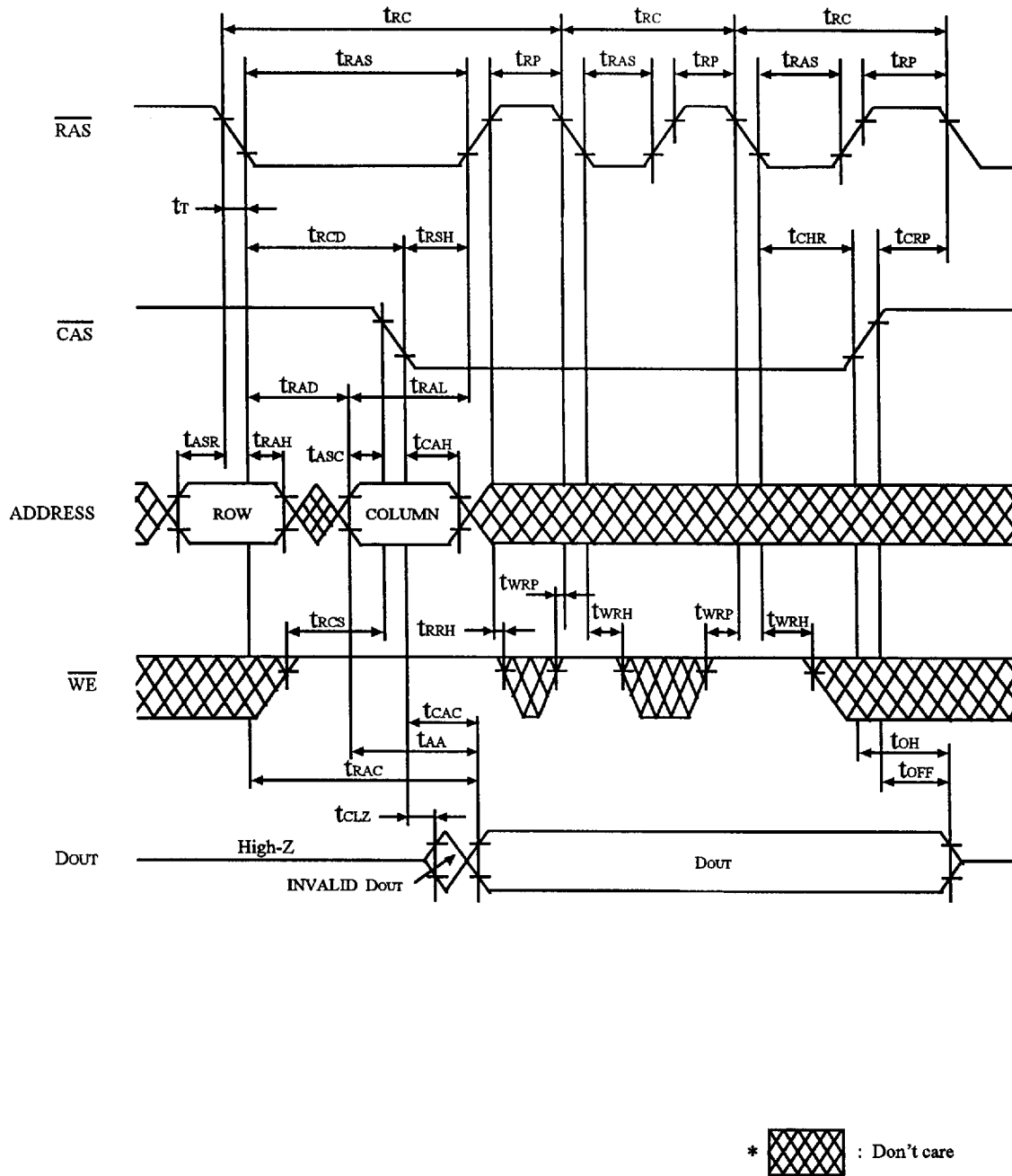


FIGURE 7. HIDDEN REFRESH CYCLE



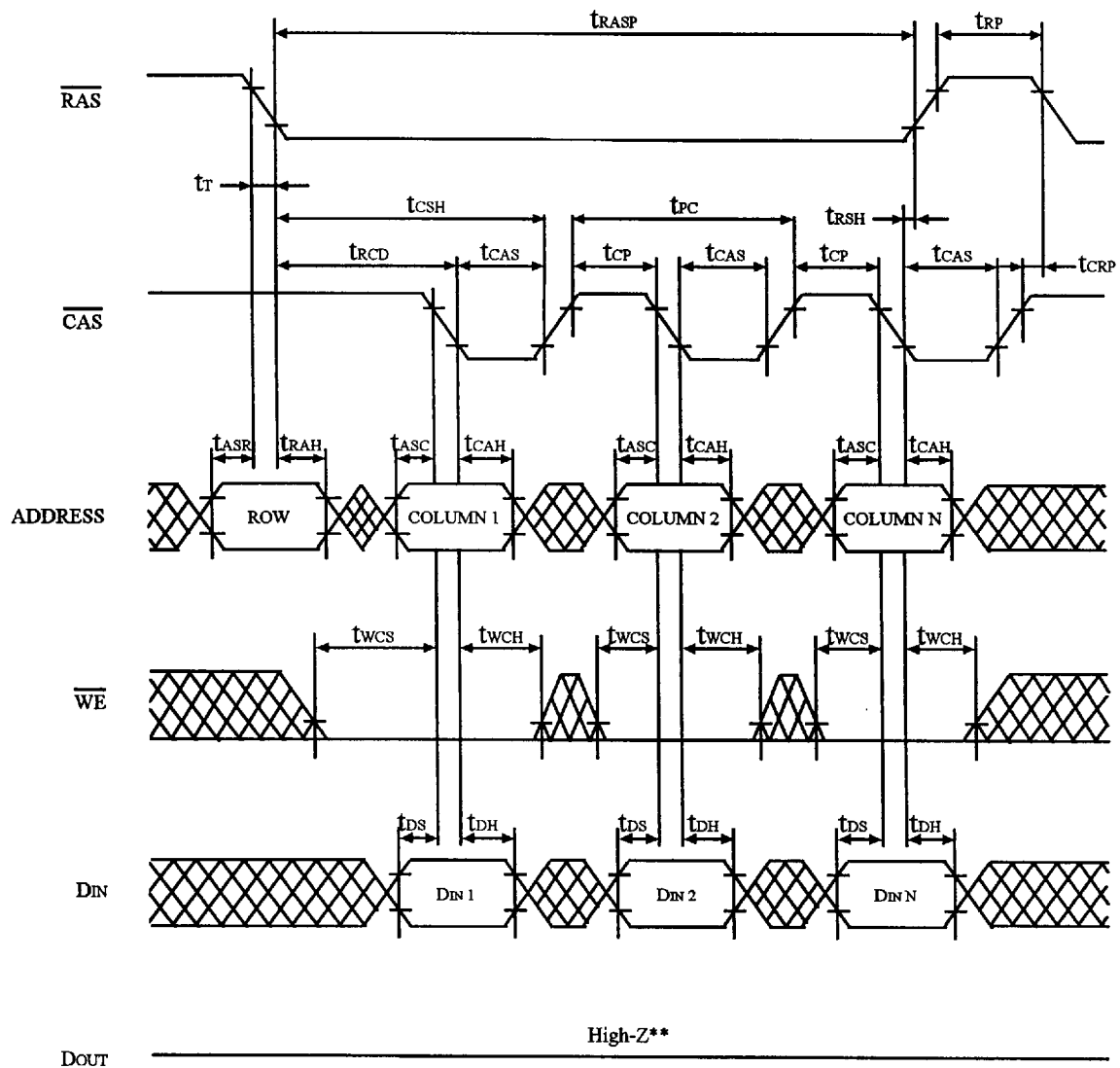


FIGURE 9. FAST PAGE MODE EARLY WRITE CYCLE

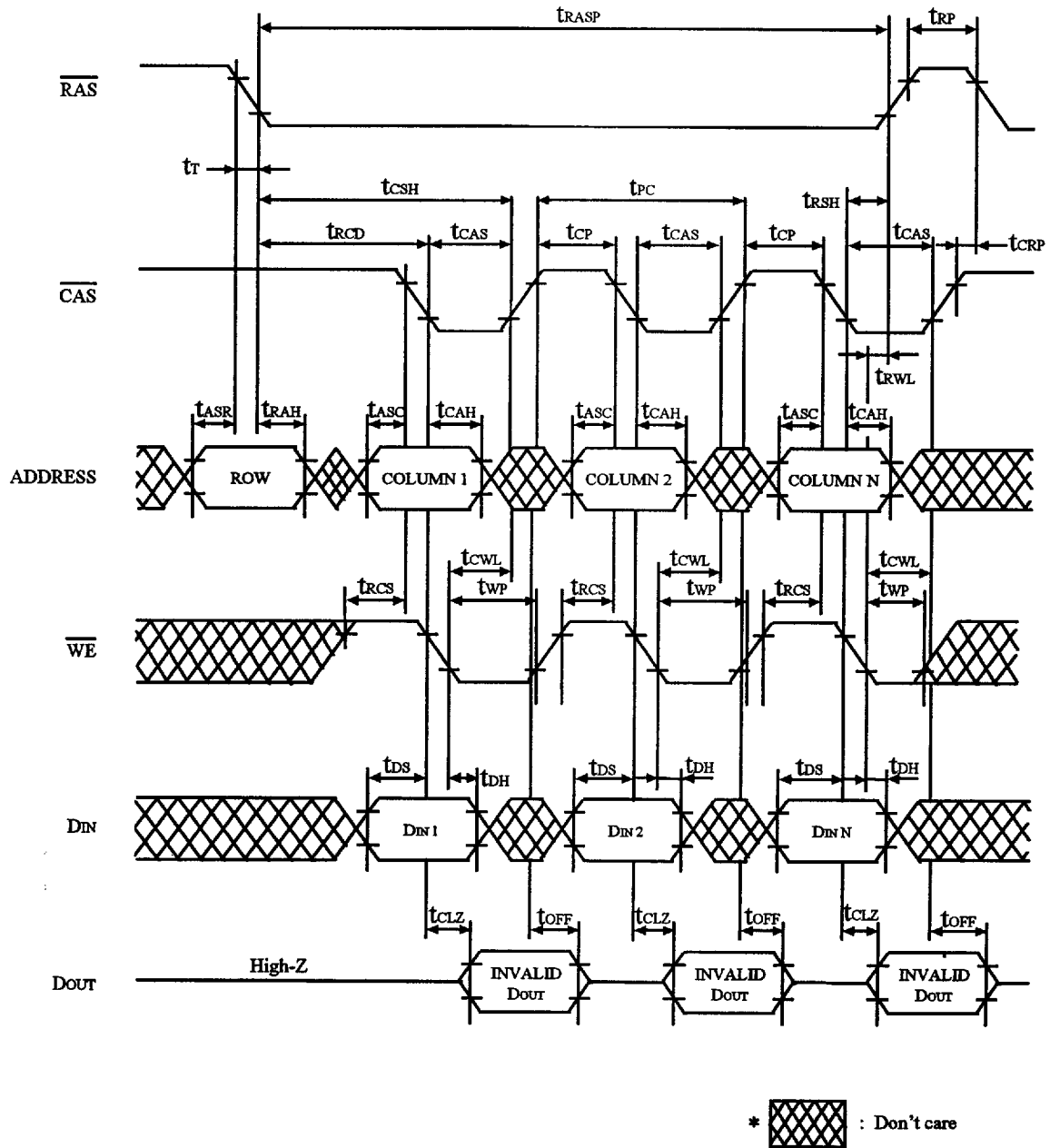


FIGURE 10. FAST PAGE MODE DELAYED WRITE CYCLE

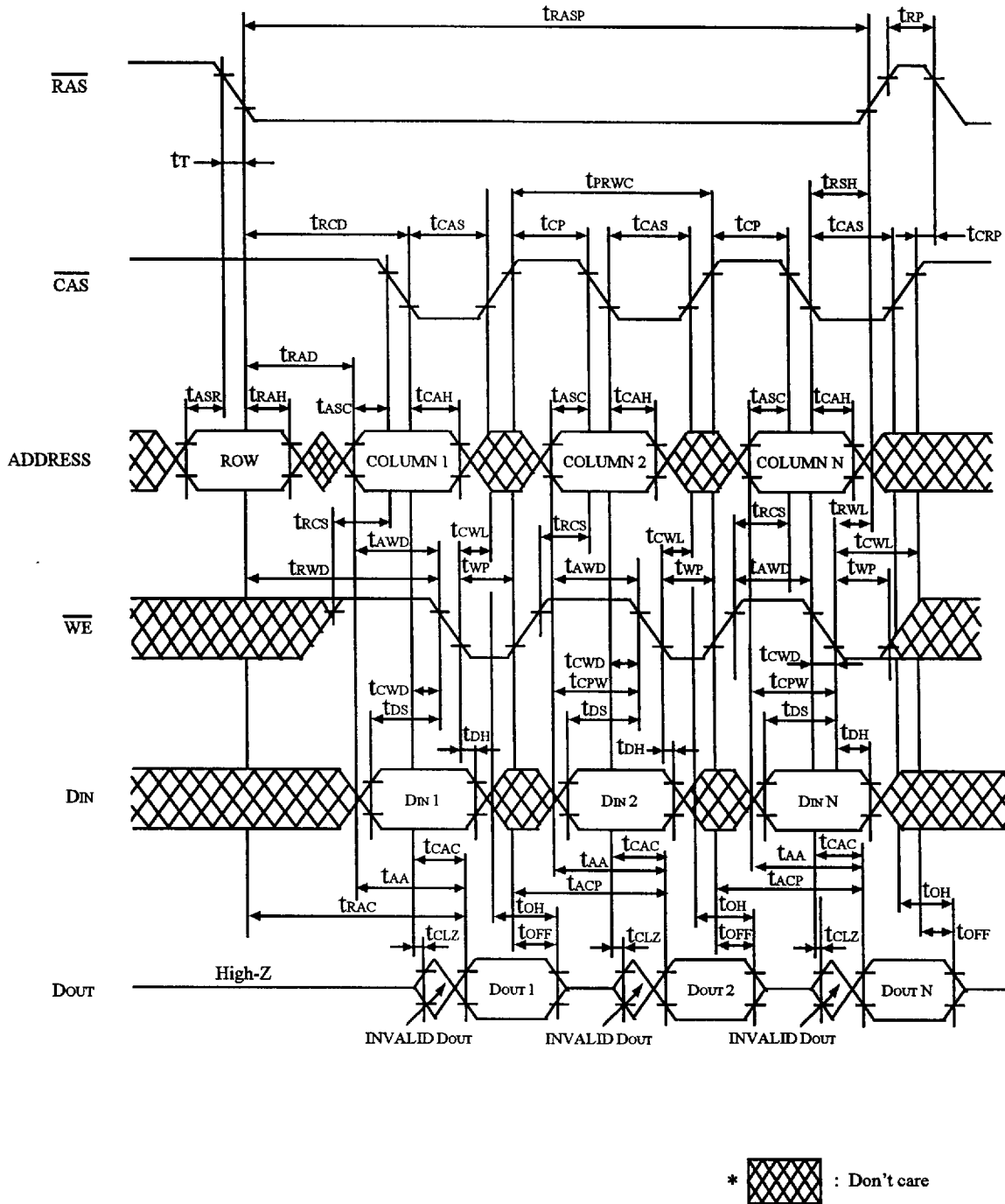


FIGURE 11. FAST PAGE MODE READ MODIFY WRITE CYCLE

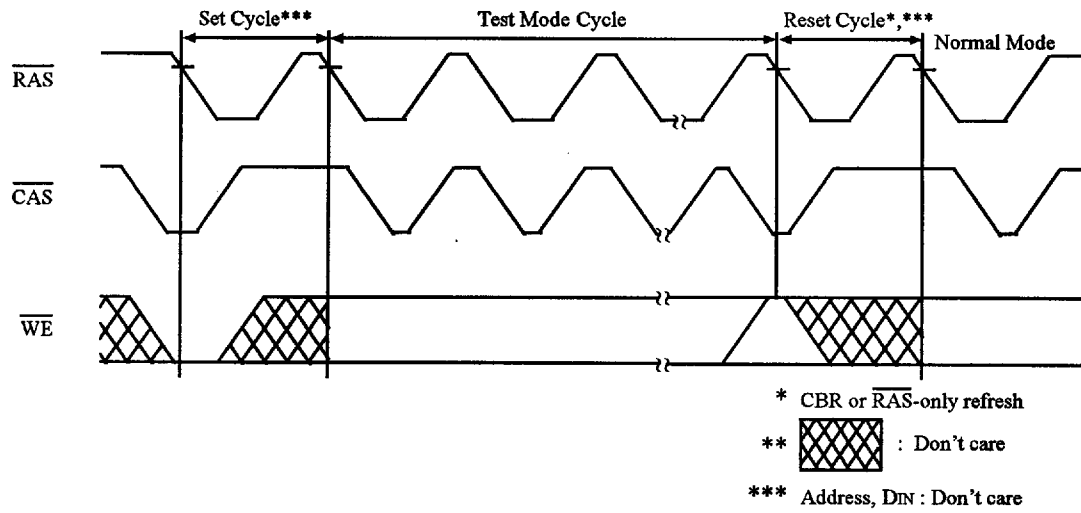


FIGURE 12. TEST MODE CYCLE

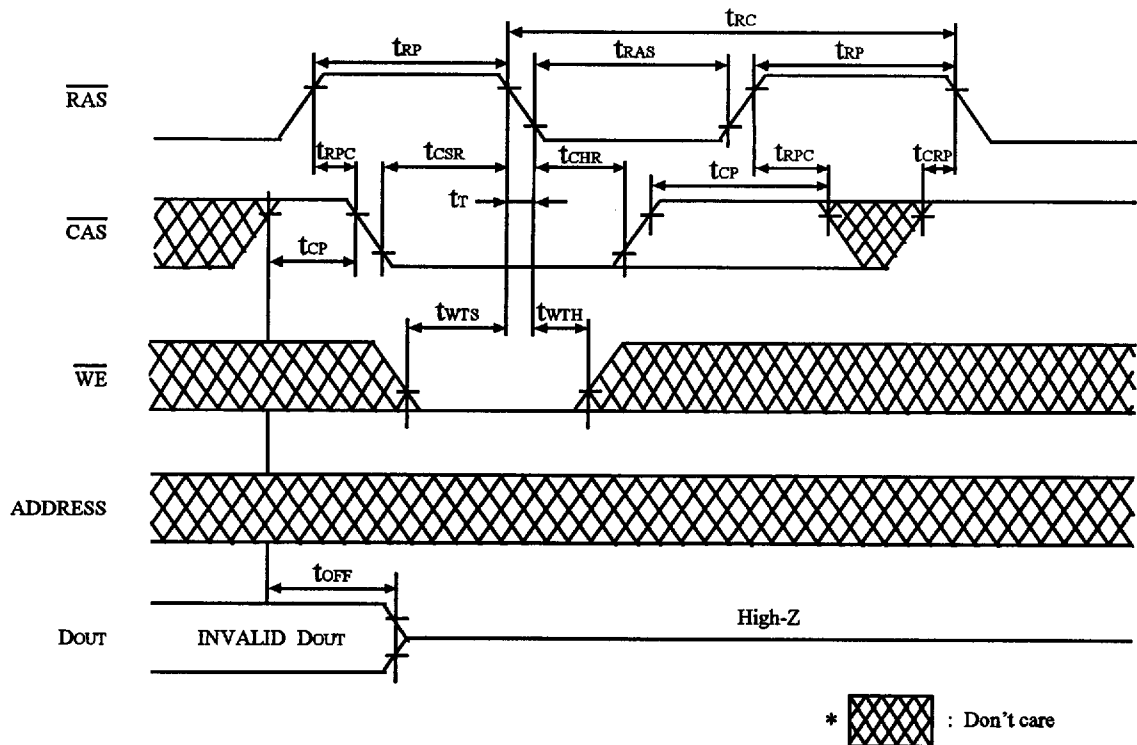


FIGURE 13. TEST MODE SET CYCLE

Test Mode Reset Cycle

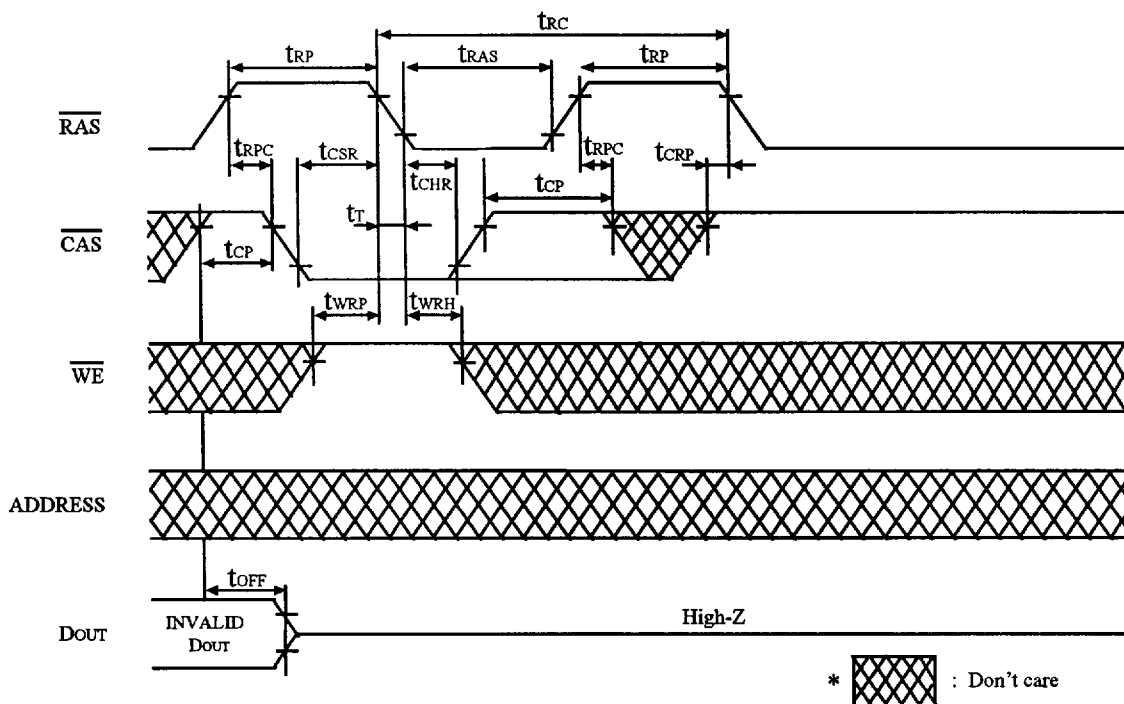


FIGURE 14. $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ REFRESH CYCLE

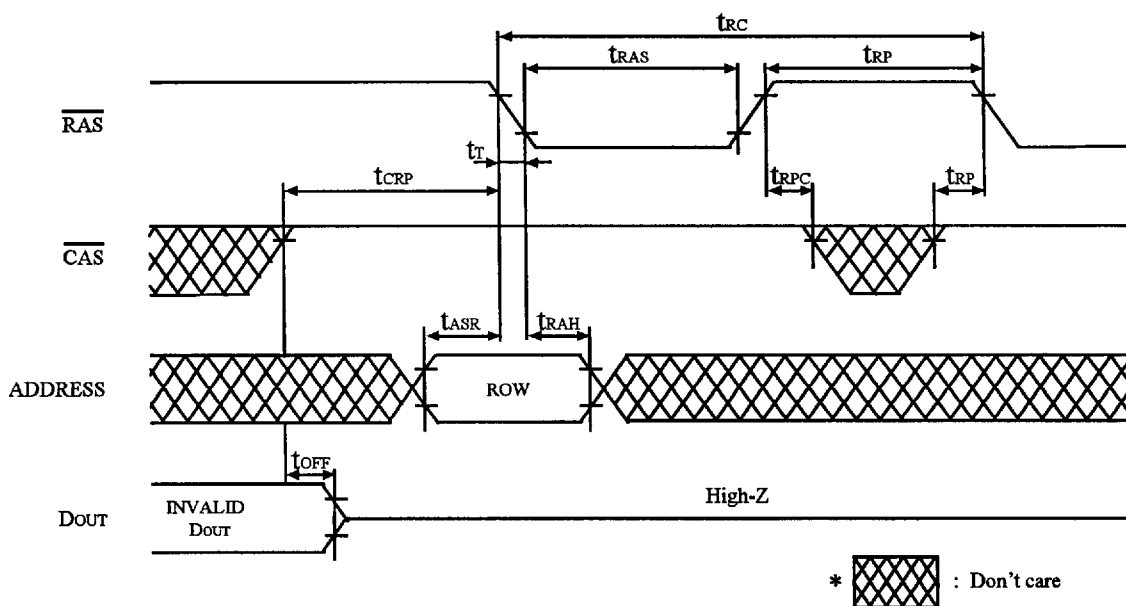


FIGURE 15. $\overline{\text{RAS}}$ ONLY REFRESH CYCLE

Package Dimension

Unit: Inches (mm)

24(26) SOJ

