HMC743LP6C / 743LP6CE

v04.0311

0.5 dB LSB GaAs MMIC DUAL 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER, DC - 4 GHz

Designer's Kit Available

Typical Applications

The HMC743LP6C(E) is ideal for:

- Cellular/3G Infrastructure
- WiBro, WiMAX & LTE/4G
- Microwave Radio & VSAT
- Test Equipment and Sensors
- IF & RF Applications

Features

-45 to +18 dB Gain Control in 0.5 dB Steps

Power-up State Selection

High Output IP3: +33 dBm

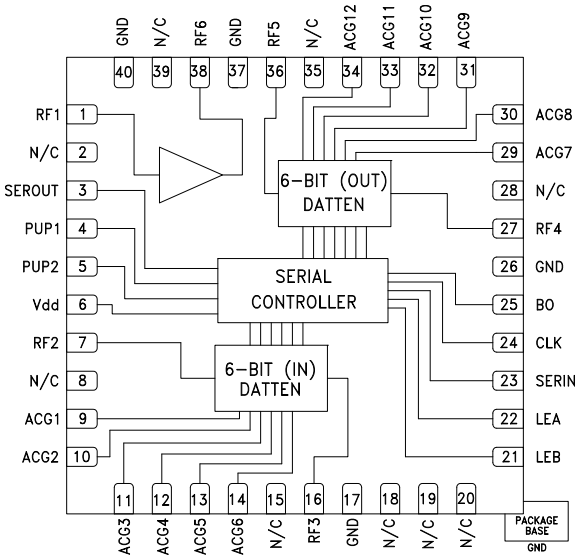
TTL/CMOS Compatible Serial Control

±0.25 dB Typical Gain Step Error

Single +5V Supply

40 Lead 6x6 mm SMT Package: 36 mm^2

Functional Diagram



General Description

The HMC743LP6C(E) is a digitally controlled variable gain amplifier which operates from DC to 4 GHz, can be programmed to provide 63 dB of gain control in 0.5 dB steps and delivers output IP3 of up to +33 dBm. The gain control interface accepts a three wire serial input word and allows independent or simultaneous control of two 6-bit digital attenuators. The HMC743LP6C(E) also features a user selectable power up state and a serial output for cascading other serially controlled Hittite products. The HMC743LP6C(E) is housed in an RoHS compliant 6x6 mm QFN leadless package, and requires minimal external components.

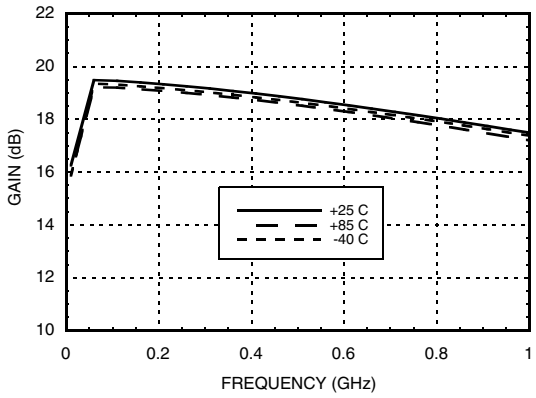
Electrical Specifications, T_A = +25° C, 50 Ohm System Vdd = +5V, Vcc = +5V

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		70 - 1000			700 - 4000		MHz
Gain (Maximum Gain State)	15.5	18.5		6	13		dB
Gain Control Range		63			63		dB
Input Return Loss		18			19		
Output Return Loss		15			17		dB
Gain Accuracy: (Referenced to Maximum Gain State) All Gain States		70 - 350 MHz: ± (0.3 + 3.5%) 350 - 750 MHz: ± (0.3 + 6.0%) 750 - 1000 MHz: ± (0.3 + 4.0%)			0.7 - 1.7 GHz: ± (0.3 + 4.5%) 1.7 - 3.2 GHz: ± (0.3 + 4.0%) 3.2 - 4.0 GHz: ± (0.3 + 5.0%)		dB dB dB
Output Power for 1 dB Compression		18			17		dBm
Output Third Order Intercept Point (Two-Tone Output Power= 8 dBm Each Tone)		33			28		dBm
Noise Figure		6			7		dB
Switching Characteristics tRISE, tFall (10 / 90% RF) tON, tOFF (Latch Enable to 10 / 90% RF)		 100 160			 100 160		 ns ns
Supply Current (Idd)		2			2		mA
Supply Current (Icc)		82	102		82	102	mA

0.5 dB LSB GaAs MMIC DUAL 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER, DC - 4 GHz

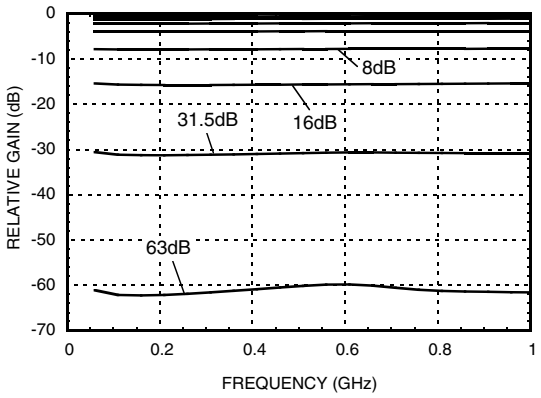
70 to 1000 MHz Tuning

Maximum Gain vs. Temperature

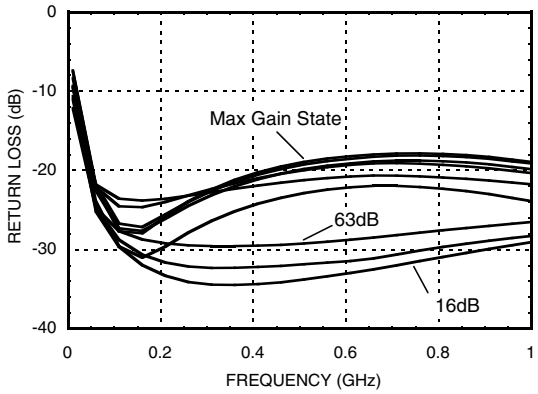


Relative Gain Setting

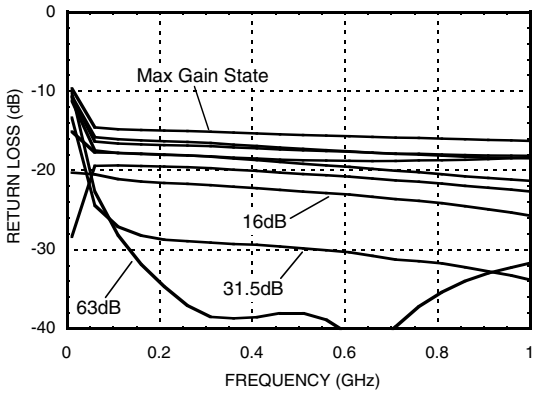
(Referenced to Maximum Gain State)



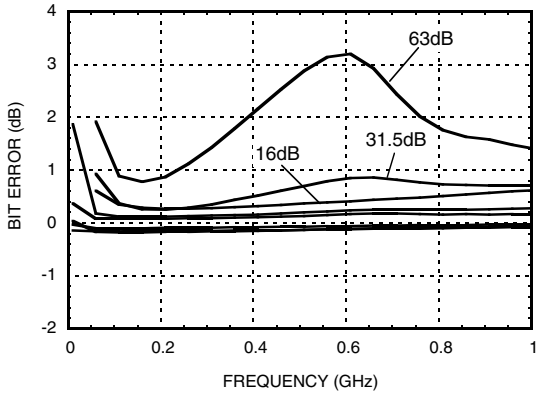
Input Return Loss



Output Return Loss

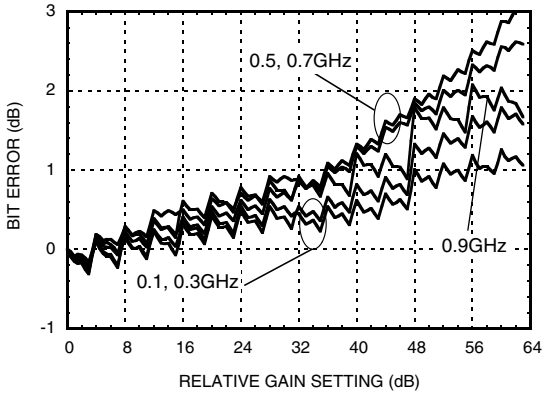


Bit Error vs. Frequency



Bit Error vs. Relative Gain State

(Major Frequencies)



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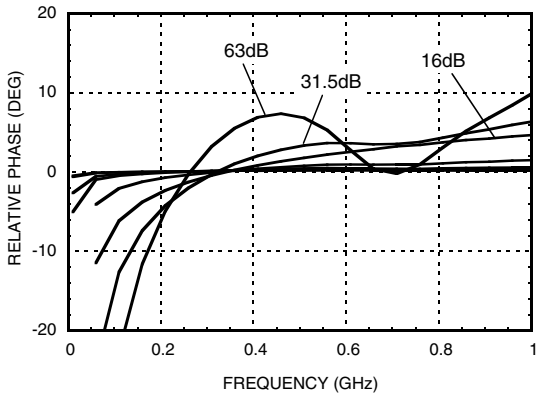
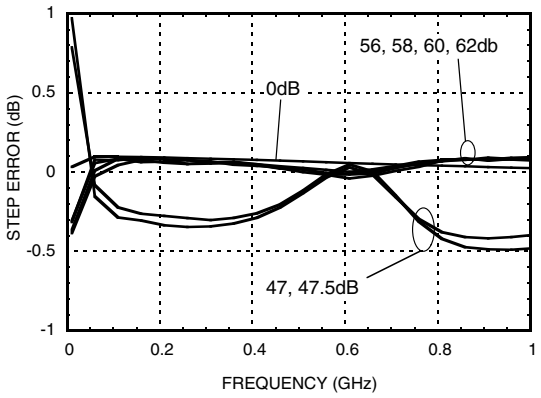
70 to 1000 MHz Tuning

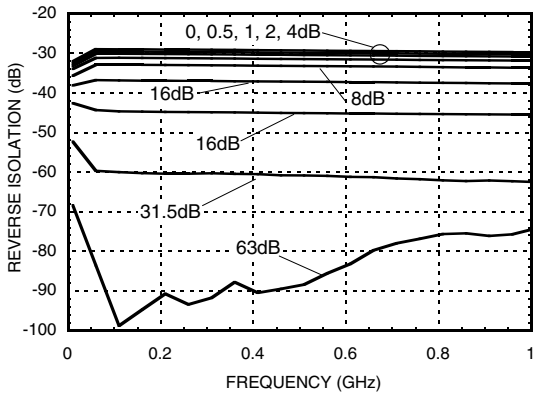
Relative Phase vs. Frequency



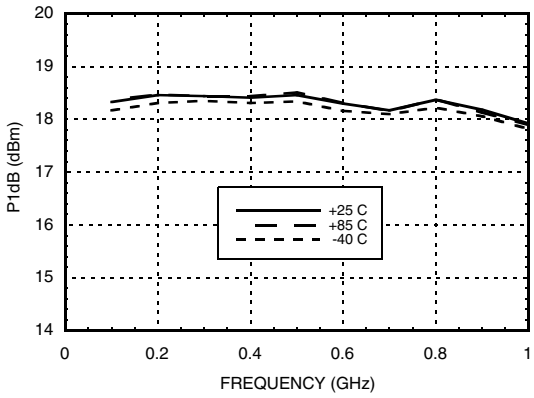
Step Error vs. Frequency *(Worst Case)*



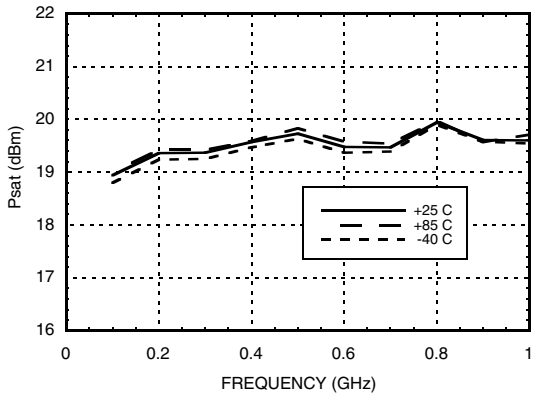
Reverse Isolation *(Major States)*



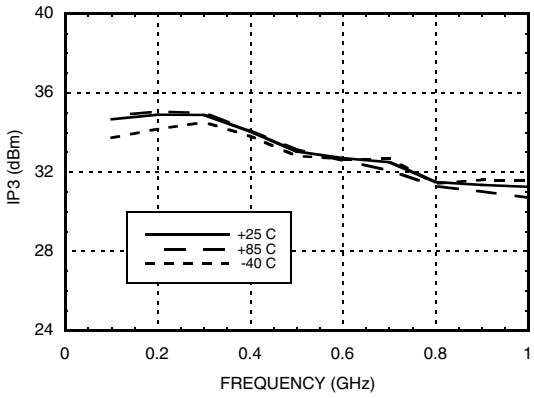
Output P1dB vs. Temperature [1]



Psat vs. Temperature [1]



Output IP3 vs. Temperature [1]



[1] Max Gain State

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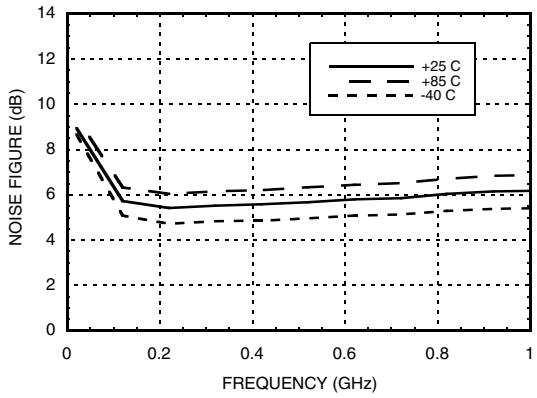
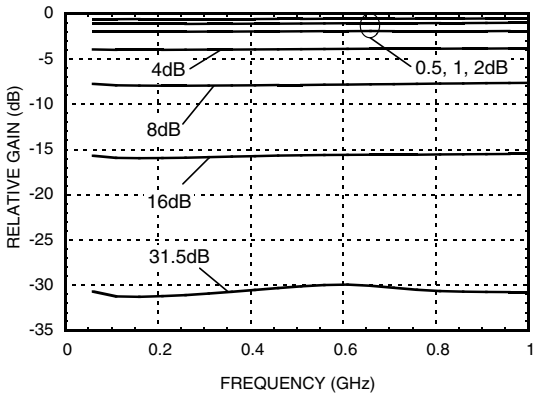
70 to 1000 MHz Tuning

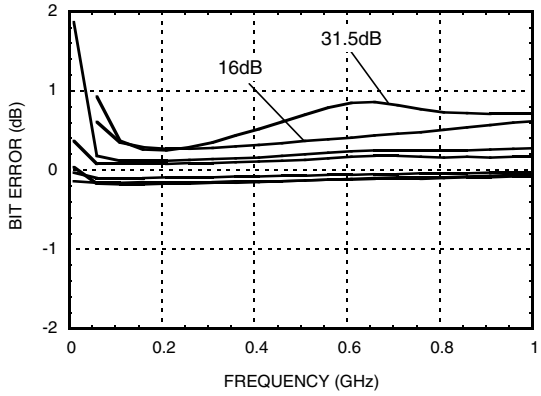
Noise Figure vs. Frequency [1]



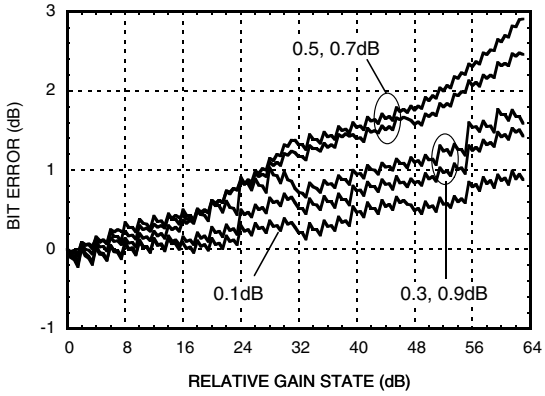
Input Attenuator Relative Attenuation
(Major States)



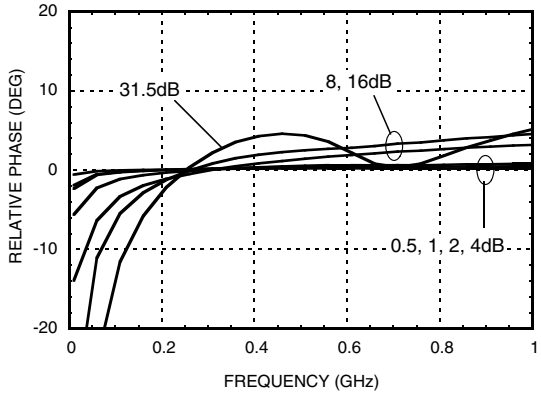
Input Attenuator Bit Error vs. Frequency *(Major States)*



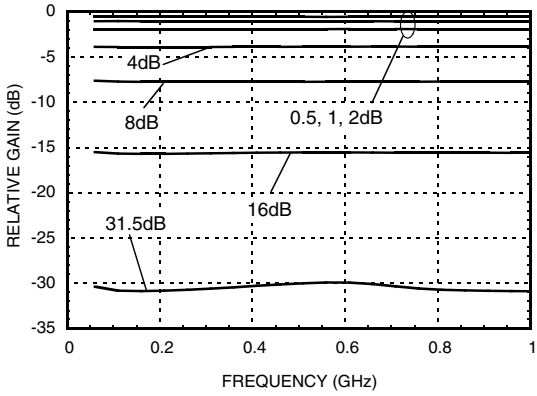
Input Attenuator Bit Error vs. Attenuation State *(Major Frequencies)*



Input Attenuator Relative Phase vs. Frequency *(Major States)*



Output Attenuator Relative Attenuation
(Major States)



[1] Max Gain State

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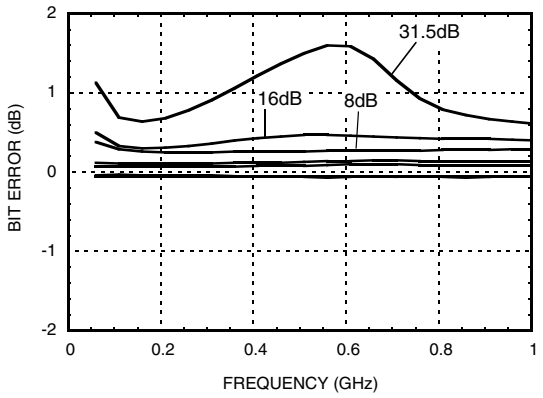
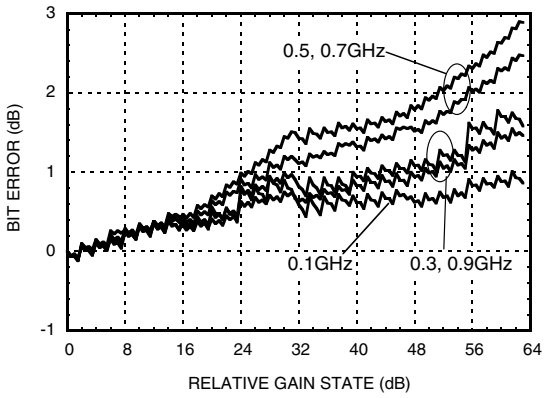
70 to 1000 MHz Tuning

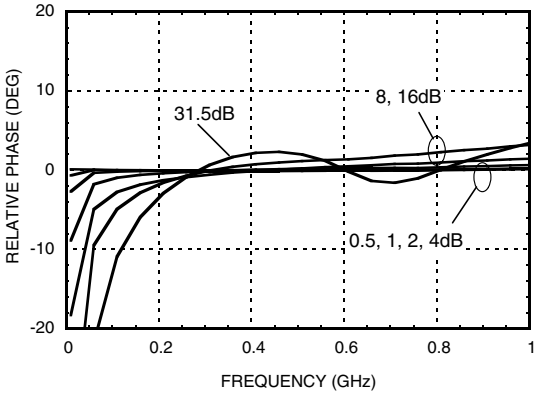
Output Attenuator Bit Error vs. Frequency *(Major States)*



Output Attenuator Bit Error vs. Attenuation State *(Major Frequencies)*



Output Attenuator Relative Phase vs. Frequency *(Major States)*



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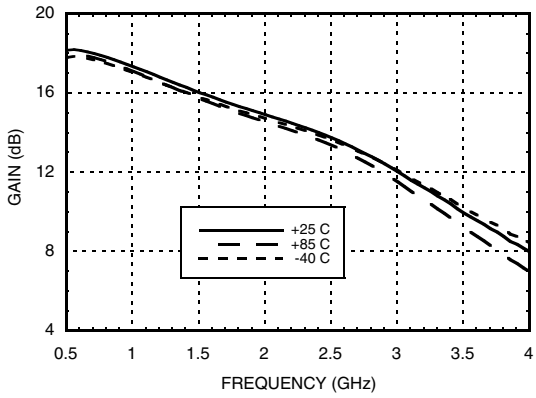
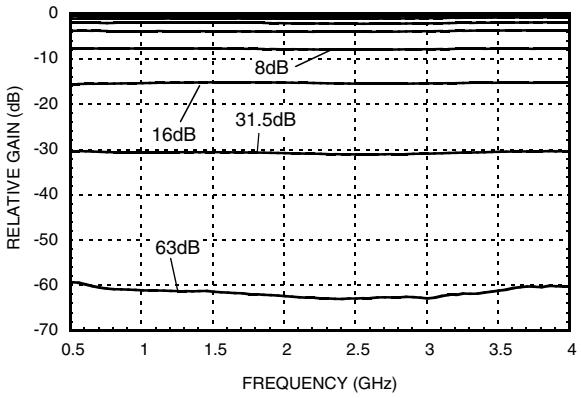
0.7 to 4.0 GHz Tuning

Maximum Gain vs. Temperature

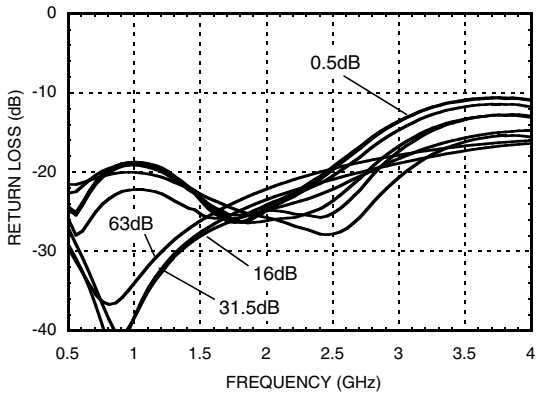


Relative Gain Setting

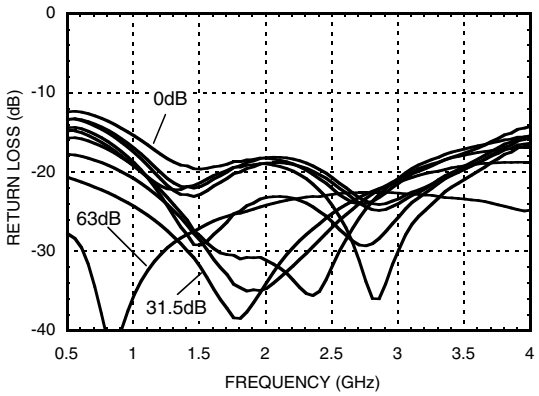
(Referenced to Maximum Gain State)



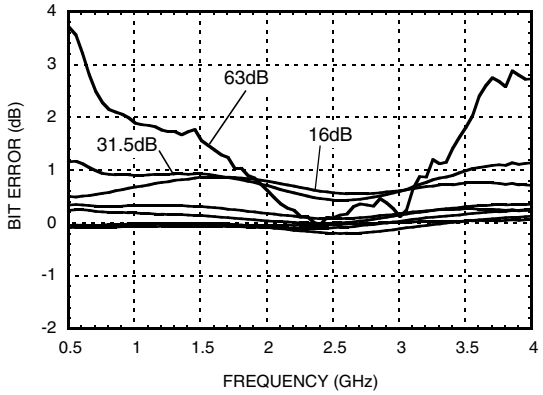
Input Return Loss



Output Return Loss

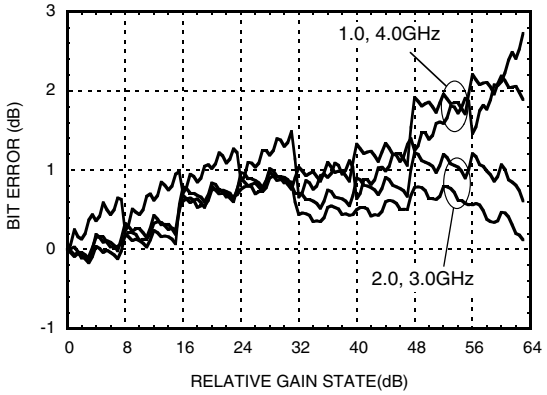


Bit Error vs. Frequency



Bit Error vs. Relative Gain State

(Major Frequencies)



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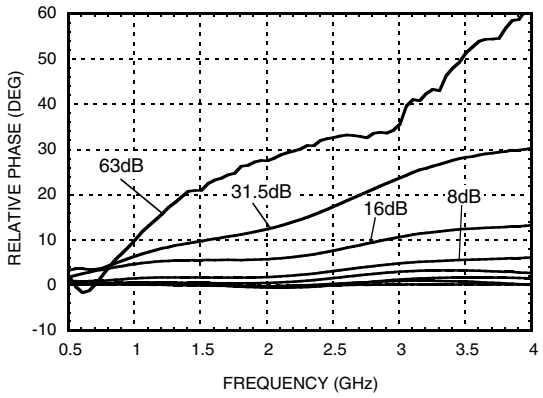
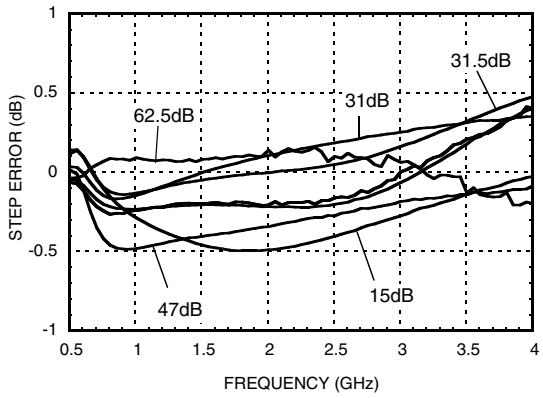
0.7 to 4.0 GHz Tuning

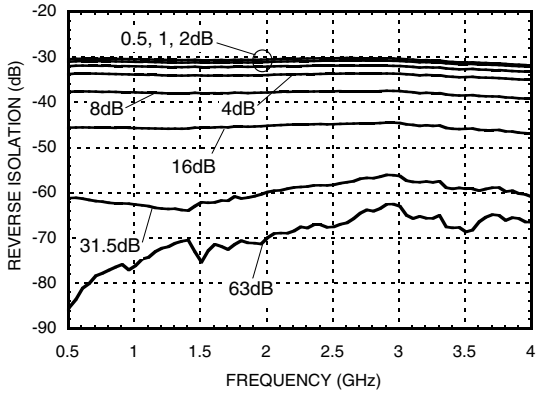
Relative Phase vs. Frequency



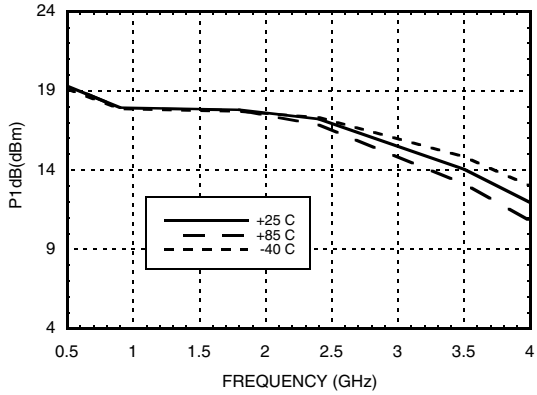
Step Error vs. Frequency (Worst Case)



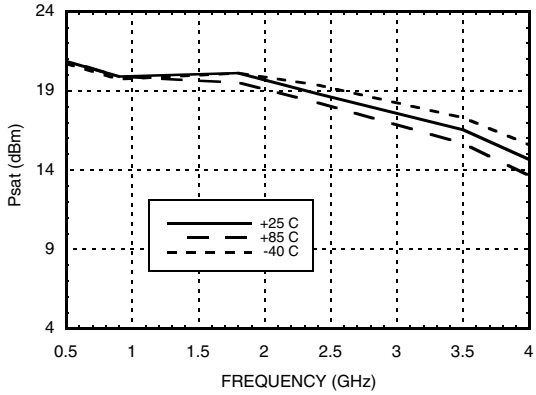
Reverse Isolation



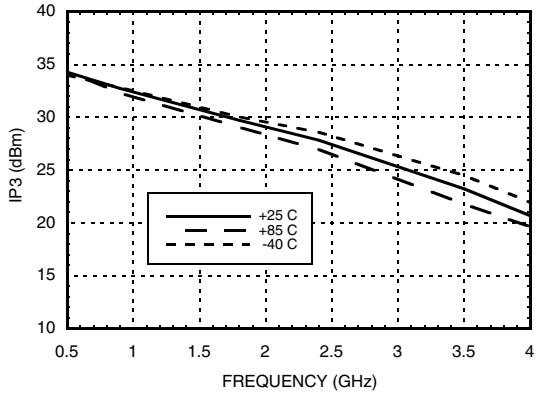
Output P1dB vs. Temperature [1]



Psat vs. Temperature [1]



Output IP3 vs. Temperature [1]



[1] Max Gain State

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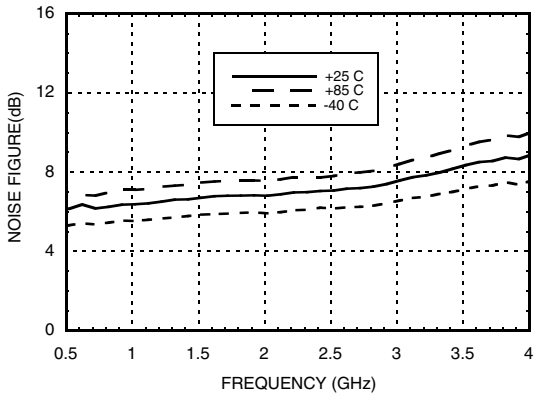
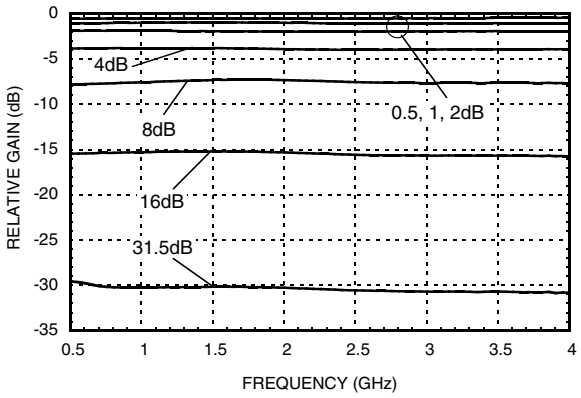
0.7 to 4.0 GHz Tuning

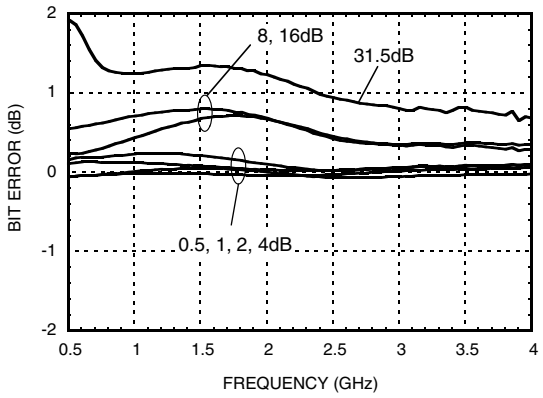
Noise Figure vs. Frequency [1]



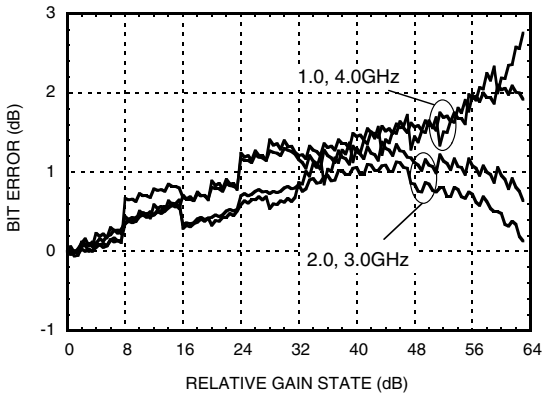
Input Attenuator Relative Attenuation
(Major States)



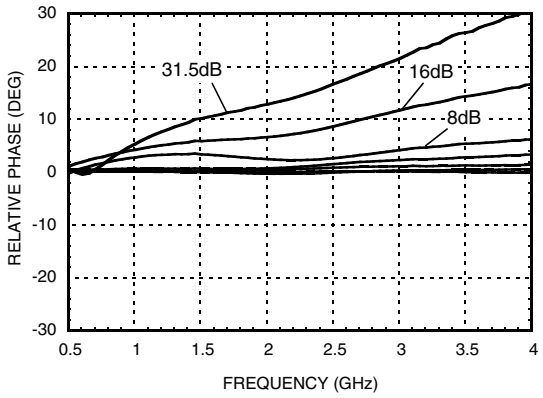
Input Attenuator Bit Error vs. Frequency *(Major States)*



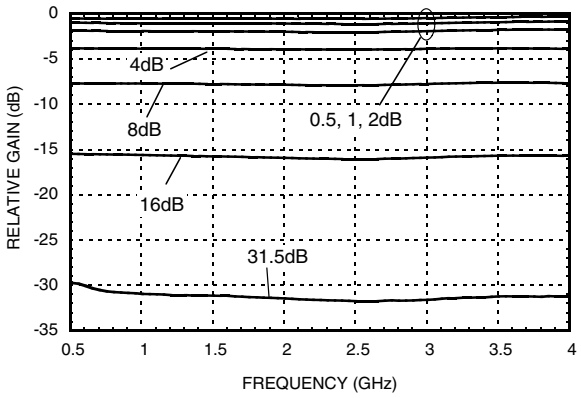
Input Attenuator Bit Error vs. Attenuation State *(Major Frequencies)*



Input Attenuator Relative Phase vs. Frequency *(Major States)*



Output Attenuator Relative Attenuation
(Major Steps)



[1] Max Gain State

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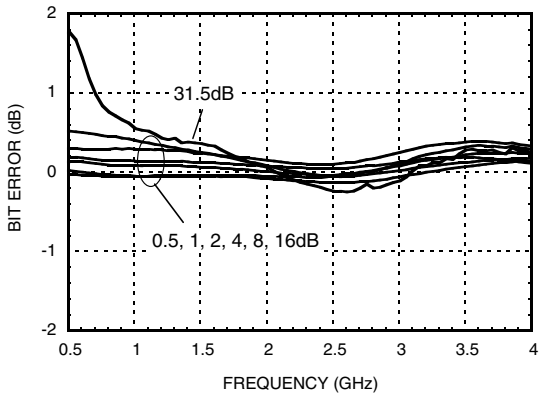
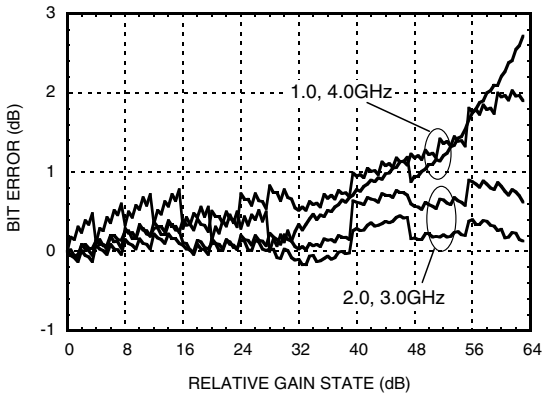
0.7 to 4.0 GHz Tuning

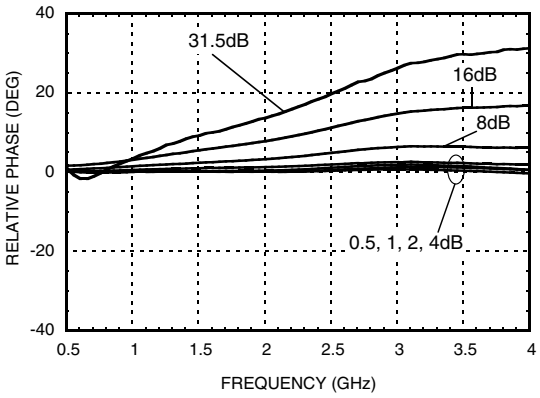
Output Attenuator Bit Error vs. Frequency *(Major States)*



Output Attenuator Bit Error vs. Attenuation State *(Major Frequencies)*



Output Attenuator Relative Phase vs. Frequency *(Major States)*

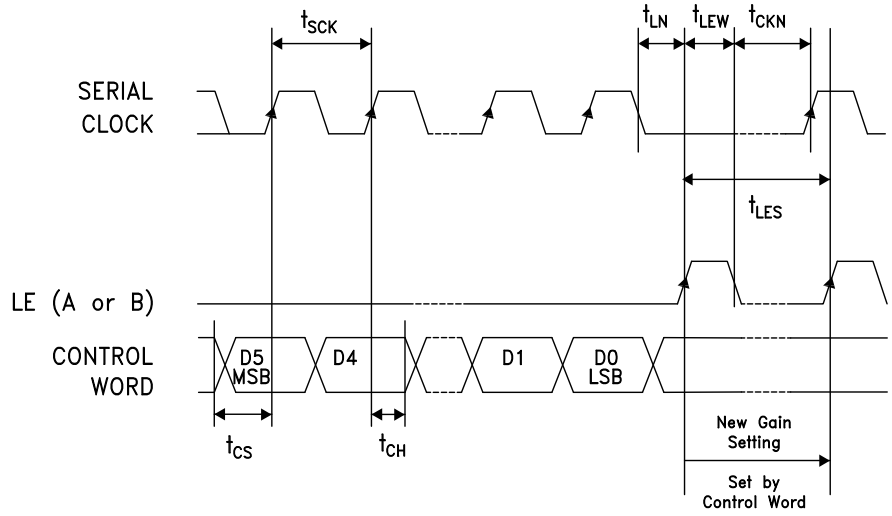


Serial Control Interface

The HMC743LP6C(E) contains a 3-wire SPI compatible digital interface (SERIN, CLK, LEA (or LEB)) that is used to control the input and output gain control elements (digital attenuators). The input (IN) and output (OUT) attenuators can be individually controlled thru the latch enable pins. The LEA pin latches the serial 6-bit control word to the output attenuator. The LEB pin latches the serial 6-bit control word to the input attenuator.

The 6-bit serial word can be loaded either MSB first or LSB first depending on the state of the BO (bit order) pin. Setting BO to high configures the serial controller to operate in LSB first mode. Setting BO to low configures the serial controller to operate in MSB first mode.

When LEA or LEB (or both) is raised to a logic high, 6-bit data in the serial input register is transferred to the input attenuator or the output attenuator (or both). While either LEA or LEB are high, CLK signal must be masked or stopped to prevent data transition during output loading.



Timing Diagram

Timing diagram is used for either input or output digital gain control. Control word is shown with MSB first (BO = Low) configuration.

Parameter	Typ.
Min. serial period, t_{SCK}	100 ns
Control set-up time, t_{CS}	20 ns
Control hold-time, t_{CH}	20 ns
LE setup-time, t_{LN}	10 ns
Min. LE pulse width, t_{LEW}	10 ns
Min LE pulse spacing, t_{LES}	630 ns
Serial clock hold-time from LE, t_{CKN}	10 ns

PUP Truth Table

LE (A and B)	PUP1	PUP2	Gain Relative to Max Setting
0	0	0	-63 dB
0	1	1	0 dB

Power-Up States

The HMC743LP6C offers two different power up states, either full attenuation or maximum gain mode. See truth table.

Power-On Sequence

The ideal power-up sequence is: GND, Vdd, digital inputs, RF inputs. The relative order of the digital inputs are not important as long as they are powered after Vdd / GND

0.5 dB LSB GaAs MMIC DUAL 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER, DC - 4 GHz

Truth Table *(for each attenuator)*

Control Voltage Input						Attenuation
D5	D4	D3	D2	D1	D0	
High	High	High	High	High	High	0 dB
High	High	High	High	High	Low	-0.5 dB
High	High	High	High	Low	High	-1 dB
High	High	High	Low	High	High	-2 dB
High	High	Low	High	High	High	-4 dB
High	Low	High	High	High	High	-8 dB
Low	High	High	High	High	High	-16 dB
Low	Low	Low	Low	Low	Low	-31.5 dB
Any combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.						

Absolute Maximum Ratings

RF Input Power [1]	11.5 dBm (T = +85 °C)
Digital Inputs (CLK, LEA, LEB, SERIN, PUP1, PUP2 & B0)	-0.5V to Vdd +0.5V
Bias Voltage (Vdd)	5.6V
Collector Bias Voltage (Vcc)	5.5V
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 14.5 mW/°C above 85 °C) [1]	1.09 W
Thermal Resistance	69 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

[1] At max gain settling

Bias Voltage

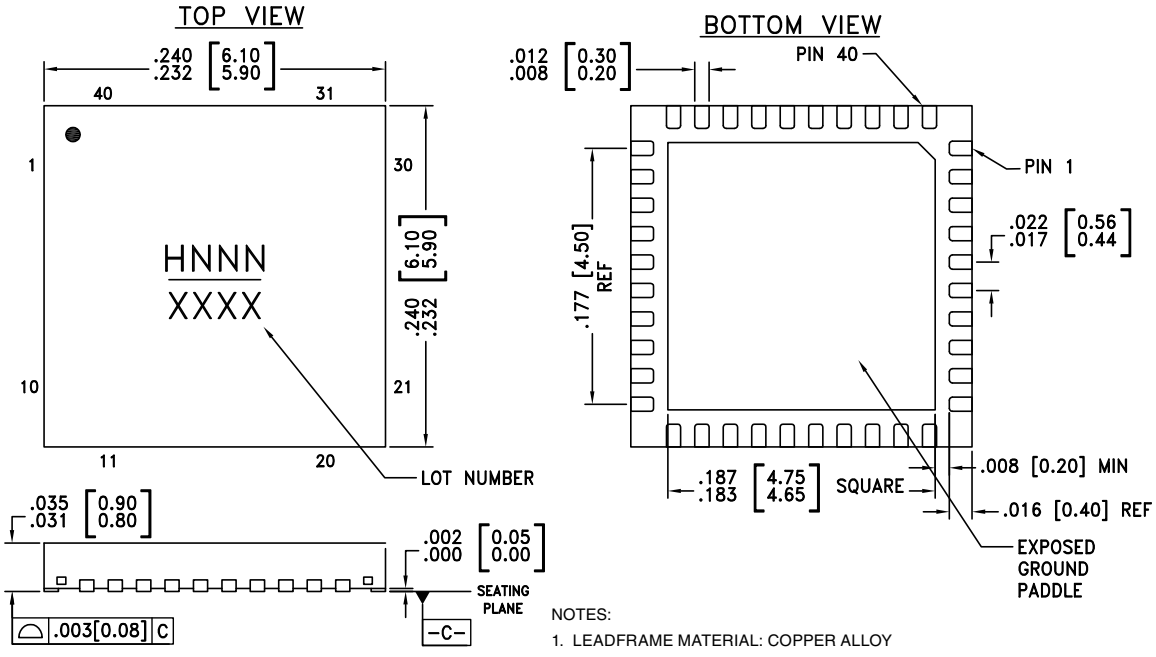
	Voltage (V)	Current (Typ.) (mA)
Vdd	+ 3.0	1
	+ 5.0	2
Vcc	+ 5.0	82

Control Voltage Table

State	Vdd = +3V , Vcc = + 5V	Vdd = Vcc = +5V
Low	0 to 0.5V @ <1 µA	0 to 0.8V @ <1 µA
High	2 to 3V @ <1 µA	2 to 5V @ <1 µA

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

For price, delivery and to place orders: Hittite Microwave Corporation, 20 Alpha Road, Chelmsford, MA 01824
Phone: 978-250-3343 Fax: 978-250-3373 Order On-line at www.hittite.com
Application Support: Phone: 978-250-3343 or apps@hittite.com

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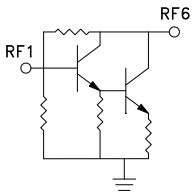
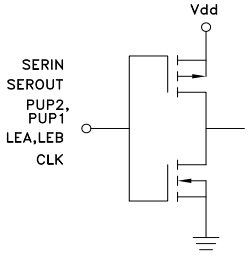
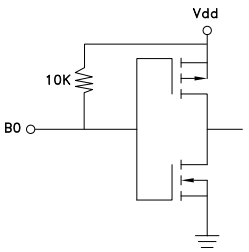
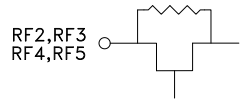
Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC743LP6C	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H743 XXXX
HMC743LP6CE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H743 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	RF1	This pin is DC coupled. An off chip DC blocking capacitor is required.	
38	RF6	RF output and DC bias for the output stage of the amplifier.	
2, 8, 15, 18 - 20, 28, 35, 39	N/C	No Connection	
3, 23	SEROUT, SERIN	Data in and out pins	
4, 5	PUP1, PUP2	Controls power up state	
21, 22	LEB, LEA	LEA is the latch enable for the output attenuator. LEB is the latch enable for the input attenuator.	
24	CLK	Clock input	
25	BO	Controls bit order of control word. B0 - High = LSB first B0 - Low = MSB first	
6	Vdd	Supply Voltage	
7, 16, 27, 36	RF2, RF3, RF4, RF5	These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required. Select value based on lowest frequency of operation.	
9 - 14	ACG1 - ACG6	External capacitors to ground are required. Place capacitor as close to pins as possible. See “Components for Selected Frequencies” table.	
17, 26, 37, 40 Paddle	GND	These pins and the exposed ground paddle must be connected to RF/DC ground.	
29 - 34	ACG7 - ACG12	External capacitors to ground are required. Place capacitor as close to pins as possible. See “Components for Selected Frequencies” table.	

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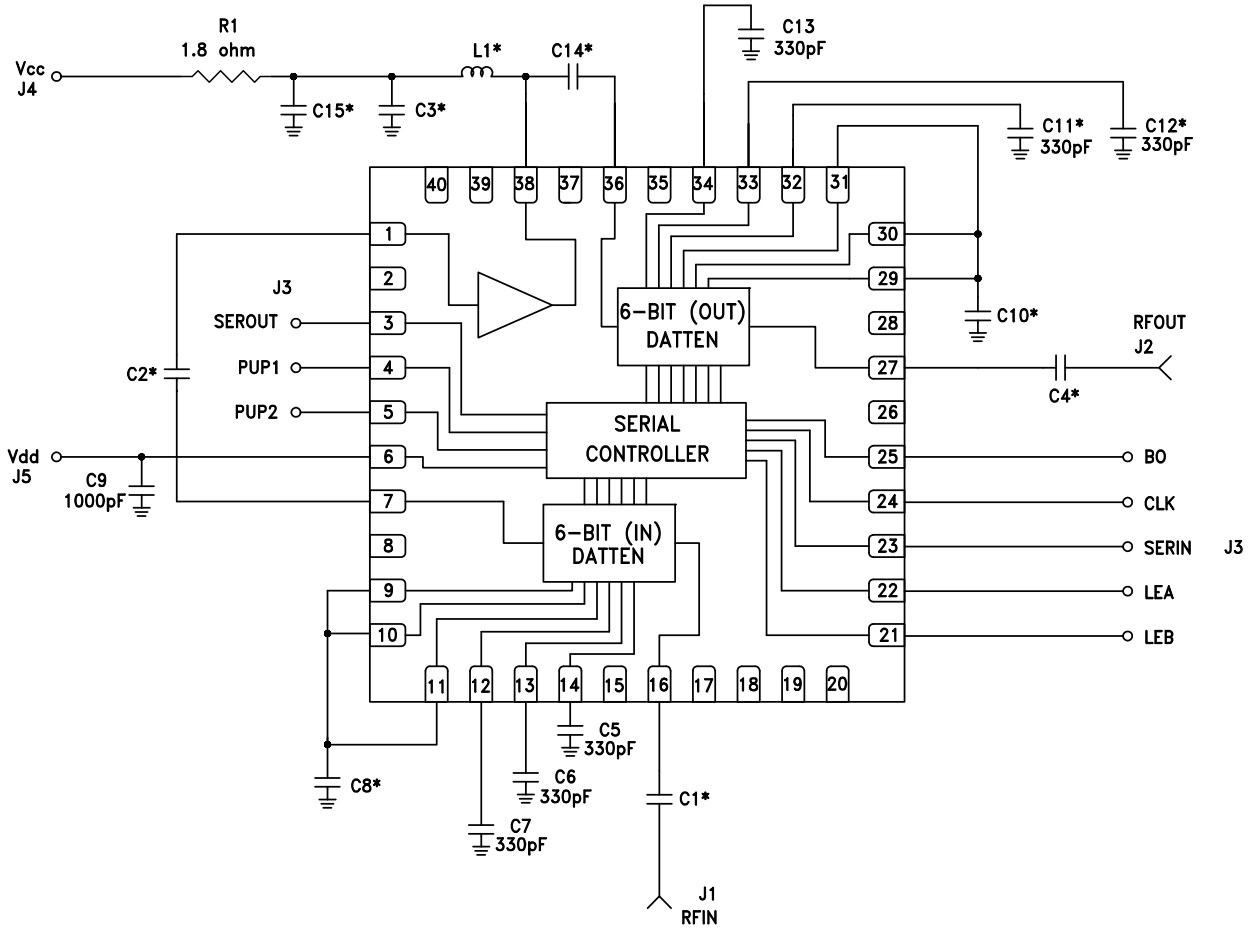
Application Circuit

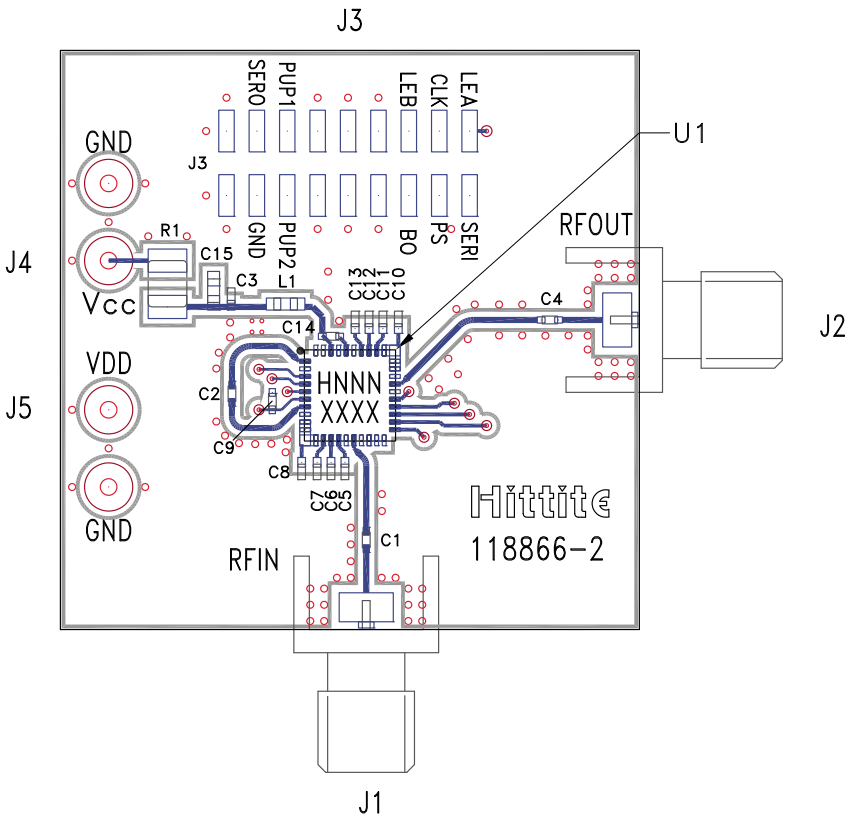


Components for Selected Frequencies *

Tuned Frequency	70 - 1000 MHz	700 - 4000 MHz
Evaluation PCB	124459 [1]	124460 [1]
C3 (pF)	1000	100
C1, C2, C4, C14 (pF)	3300	100
C8, C10 (pF)	100	330
C15 (pF)	2200	1000
L1 (nH)	560	36

[1] Reference this number when ordering complete evaluation PCB.

Evaluation PCB



List of Materials for Evaluation [1]

Item	Description
J1, J2	PCB Mount SMA Connector
J3	18 pos Header, 2mm
J4, J5	DC Pin
C1 - C4	Capacitor, 0402 Pkg. [1]
C5 - C7	330 pF Capacitor, 0402 Pkg.
C8, C10	Capacitor, 0402 Pkg. [1]
C9	100 pF Capacitor, 0402 Pkg.
C15	Capacitor, 0603 Pkg. [1]
L1	Inductor, 0603 Pkg.
R1	1.8 Ohm Resistor, 1206 Pkg.
U1	HMC743LP6(E) Variable Gain Amplifier
PCB [2]	118866 Evaluation PCB

[1] Please reference Components for Selected Frequencies Table

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.