19-3014; Rev 1; 10/04

MAXIM

Dual Per-Pin Parametric Measurement Units

General Description

The MAX9949/MAX9950 dual parametric measurement units (PMUs) feature a small package size, wide force and measurement range, and high accuracy, making the devices ideal for automatic test equipment (ATE) and other instrumentation that requires a PMU per pin or per site.

The MAX9949/MAX9950 force or measure voltages in the -2V to +7V through -7V to +13V ranges, dependent upon the supply voltage (V_{CC} and V_{EE}). The devices handle supply voltages of up to +30V (V_{CC} to V_{EE}) and a 20V device under test (DUT) voltage swing at full current. The MAX9949/MAX9950 also force or measure currents up to ±25mA with a lowest full-scale range of ±2µA. Integrated support circuitry facilitates use of an external buffer amplifier for current ranges greater than ±25mA.

A voltage proportional to the measured output voltage or current is provided at the MSR_ output. Integrated comparators, with externally set voltage thresholds, provide detection for both voltage and current levels. The MSR_ and comparator outputs can be placed in a high-Z state. Integrated voltage clamps limit the force output to levels set externally. The force-current or the measure-current voltage can be offset -0.2V to +4.4V (IOS). This feature allows for the centering of the control or measured signal within the external DAC or ADC range.

The MAX9949D/MAX9950D feature an integrated 10kΩ force-sense resistor between FORCE_ and SENSE_. The MAX9949F/MAX9950F have no internal force-sense resistor. These devices are available in a 64-pin 10mm x 10mm, 0.5mm pitch TQFP package with an exposed 8mm x 8mm die pad on the top (MAX9949) or the bottom (MAX9950) of the package for efficient heat removal. The exposed paddle is internally connected to V_{EE}. The MAX9949/MAX9950 are specified over the commercial (0°C to +70°C) temperature range.

Applications

Memory Testers

VLSI Testers

System-on-a-Chip Testers

Structural Testers

Pin Configurations appear at end of data sheet.

Features

- ♦ **Force Voltage/Measure Current (FVMI)**
- ♦ **Force Current/Measure Voltage (FIMV)**
- ♦ **Force Voltage/Measure Voltage (FVMV)**
- ♦ **Force Current/Measure Current (FIMI)**
- ♦ **Force Nothing/Measure Voltage (FNMV)**
- ♦ **Five Programmable Current Ranges**
  - **±2µA**
  - **±20µA**
  - **±200µA**
  - **±2mA**
  - **±25mA**
- ♦ **-2V to +7V Through -7V to +13V Input Voltage Range and Higher (Up to 20V Voltage Swing at Full Current)**
- ♦ **Force-Current/Measure-Current Voltage Offset (IOS)**
- ♦ **Programmable Voltage Clamps for the Force Output**
- ♦ **Low-Leakage, High-Z Measure State**
- ♦ **3-Wire Serial Interface**
- ♦ **Low Power, 8mA (max) per PMU**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9949DCCB	0°C to +70°C	64 TQFP-EPR*
MAX9949FCCB	0°C to +70°C	64 TQFP-EPR*
MAX9950DCCB	0°C to +70°C	64 TQFP-EP**
MAX9950FCCB	0°C to +70°C	64 TQFP-EP**

Exposed pad is internally connected to V_{EE}.

**EPR = Exposed pad on top.*

***EP = Exposed pad on bottom.*

Selector Guide

PART	DESCRIPTION
MAX9949DCCB	Internal 10kΩ force-sense resistor
MAX9949FCCB	No internal force-sense resistor
MAX9950DCCB	Internal 10kΩ force-sense resistor
MAX9950FCCB	No internal force-sense resistor

Dual Per-Pin Parametric Measurement Units

ABSOLUTE MAXIMUM RATINGS

V_{CC} to AGND .....+20V
V_{EE} to AGND .....-15V
V_{CC} to V_{EE} .....+32V
V_L to AGND .....+6V
AGND to DGND .....-0.5V to +0.5V
All Other Pins .....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Digital Inputs/Outputs .....-0.3V to (V_L + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
64-Pin TQFP-EP (derate 43.5mW/°C above +70°C) 3478mW
Θ_{JA} .....+23.0°C/W
Θ_{JC} .....+8°C/W
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Operating Temperature (commercial) Range .....0°C to +70°C
Lead Temperature (soldering 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +12V, V_{EE} = -7V, V_L = +3.3V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FORCE VOLTAGE (Note 2)							
Force Input Voltage Range	$V_{IN0\_}$, $V_{IN1\_}$			V_{EE} + 3.5V		V_{CC} - 3.5V	V
Forced Voltage	V_{DUT}	DUT current at full scale	V_{CC} = +12V, V_{EE} = -7V	-2		+7	V
			V_{CC} = +18V, V_{EE} = -	-7		+13	
		DUT current = 0		V_{EE} + 3.5V		V_{CC} - 3.5V	
Input Bias Current					±1		µA
Forced-Voltage Offset Error	V_{FOS}	T_A = +25°C		-25		+25	mV
Forced-Voltage Offset Temperature Coefficient					±100		µV/°C
Forced-Voltage Gain Error	V_{FGE}	T_A = +25°C, nominal gain of +1		-1	0.005	+1	%
Forced-Voltage Gain Temperature Coefficient					±10		ppm/°C
Forced-Voltage Linearity Error	V_{FLER}	T_A = +25°C, gain and offset errors calibrated out (Notes 3, 4)		-0.02		+0.02	%FSR
MEASURE CURRENT (Note 2)							
Measure-Current Offset	I_{MOS}	T_A = +25°C (Note 3)		-1		+1	%FSR
Measure-Current Offset Temperature Coefficient					±20		ppm/°C
Measure-Current Gain Error	I_{MGE}	T_A = +25°C (Note 6)		-1		+1	%
Measure-Current Gain Temperature Coefficient					±20		ppm/°C
Linearity Error	I_{MLER}	T_A = +25°C, gain, offset, and common-mode errors calibrated out (Notes 3, 4, 5)	Ranges A–D	-0.02		+0.02	%FSR
			Range E	-1		+1	nA
Measure Output Voltage Range over Full Current Range (Note 7)	V_{MSR}	V_{IOS} = V_{DUTGND}		-4		+4	V
		V_{IOS} = 4V + V_{DUTGND}		0		8	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +12V, V_{EE} = -7V, V_L = +3.3V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current-Sense Amp Offset Voltage Input	V_{IOS}	Relative to V_{DUTGND}		-0.2		+4.4	V
Rejection of Output Measure Error Due to Common-Mode Sense Voltage	$CMVR_{LER}$	Specified as the percent of full-scale range change at the measure output per volt change in the DUT voltage			0.001	0.007	%FSR/V
Measure Current Range		Range E, R_E = 1MΩ		-2		+2	µA
		Range D, R_D = 100kΩ		-20		+20	
		Range C, R_C = 10kΩ		-200		+200	
		Range B, R_B = 1kΩ		-2		+2	mA
		Range A, R_A = 80Ω		-25		+25	
FORCE CURRENT (Note 2)							
Input Voltage Range for Setting Forced Current Over Full Range	V_{INI}	V_{IOS} = V_{DUTGND}		-4		+4	V
		V_{IOS} = 4V + V_{DUTGND}		0		+8	
Current-Sense Amp Offset Voltage Input	V_{IOS}	Relative to V_{DUTGND}		-0.2		+4.4	V
V_{IOS} Input Bias Current					±1		µA
Forced-Current Offset	I_{FOS}	T_A = +25°C (Note 3)		-1		+1	%FSR
Forced-Current Offset Temperature Coefficient					±20		ppm/°C
Forced-Current Gain Error	I_{FGE}	T_A = +25°C (Note 6)		-1		+1	%
Forced-Current Gain Temperature Coefficient					±20		ppm/°C
Forced-Current Linearity Error	I_{FLER}	T_A = +25°C, gain, offset, and common-mode errors calibrated out (Notes 3, 4, 5)	Ranges A–D	-0.02		+0.02	%FSR
			Range E	-1		+1	nA
Rejection of Output Error Due to Common-Mode Load Voltage	$CMRI_{OER}$	Specified as the percent of full-scale range change of the forced current per volt change in the DUT voltage			+0.001	+0.007	%FSR/V
Forced-Current Range		Range E, R_E = 1MΩ		-2		+2	µA
		Range D, R_D = 100kΩ		-20		+20	
		Range C, R_C = 10kΩ		-200		+200	
		Range B, R_B = 1kΩ		-2		+2	mA
		Range A, R_A = 80Ω		-25		+25	
MEASURE VOLTAGE (Note 2)							
Measure-Voltage Offset	V_{MOS}	T_A = +25°C		-25		+25	mV
Measure-Voltage Offset Temperature Coefficient					±100		µV/°C
Gain Error	V_{MGER}	T_A = +25°C, nominal gain of +1		-1	±0.005	+1	%
Measure-Voltage Gain Temperature Coefficient					±10		ppm/°C

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +12V, V_{EE} = -7V, V_L = +3.3V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Measure-Voltage Linearity Error	V_{MLER}	T_A = +25°C, gain and offset errors calibrated out (Notes 3, 4, 5)		-0.02		+0.02	%FSR
Measure Output Voltage Range over Full DUT Voltage (V_{DUT})	V_{MSR}	DUT current at full scale	V_{CC} = +12V, V_{EE} = -7V	-2		+7	V
			V_{CC} = +18V, V_{EE} = -12V	-7		+13	
		DUT current = 0V		V_{EE} + 3.5V		V_{CC} - 3.5V	
FORCE OUTPUT							
Off-State Leakage Current		T_A = +25°C		-5		+5	nA
Short-Circuit Current Limit	I_{LIM-}			-45		-28	mA
	I_{LIM+}			+28		+45	
Force-to-Sense Resistor	R_{FS}	D option only		7.8	10	13.3	kΩ
SENSE INPUT							
Input Voltage Range				V_{EE} + 3.5V		V_{CC} - 3.5V	V
Leakage Current				-5		+5	nA
COMPARATOR INPUTS							
Input Voltage Range				V_{EE} + 3.5V		V_{CC} - 3.5V	V
Offset Voltage		T_A = +25°C		-25		+25	mV
Input Bias Current					±1		µA
VOLTAGE CLAMPS							
Input Control Voltage	$V_{CLLO\_}$, $V_{CLHI\_}$			V_{EE} + 3.4V		V_{CC} - 3.4V	V
Clamp Voltage Range				V_{EE} + 3.5V		V_{CC} - 3.5V	V
Clamp Voltage Accuracy				-100		+100	mV
DIGITAL INPUTS							
Input High Voltage (Note 8)	V_{IH}	5V logic		+3.5			V
		3.3V logic		+2.0			
		2.7V logic		+1.7			
Input Low Voltage (Note 8)	V_{IL}	5V and 3.3V logic				+0.8	V
		2.5V logic				+0.7	
Input Current	I_{IN}				±1		µA
Input Capacitance	C_{IN}				3.0		pF
COMPARATOR OUTPUTS (Note 8)							
Output High Voltage	V_{OH}	V_L = +2.375V to +5.5V, R_{PUP} = 1kΩ		V_L - 0.2			V
Output Low Voltage	V_{OL}	V_L = +2.375V to +5.5V, R_{PUP} = 1kΩ				+0.4	V
High-Z State Leakage Current					±1		µA
High-Z State Output Capacitance					6.0		pF

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +12V, V_{EE} = -7V, V_L = +3.3V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS (Note 8)						
Output High Voltage	V_{OH}	I_{OUT} = 1mA, V_L = +2.375V to +5.5V, relative to DGND	V_L - 0.25			V
Output Low Voltage	V_{OL}	I_{OUT} = -1mA, V_L = +2.375V to +5.5V, relative to DGND			0.2	V
POWER SUPPLY						
Positive Supply	V_{CC}	(Note 1)	+10	+12	+18	V
Negative Supply	V_{EE}	(Note 1)	-15	-7	-5	V
Total Supply Voltage	V_{CC} - V_{EE}				+30	V
Logic Supply	V_L		+2.375		+5.5	V
Positive Supply Current	I_{CC}	No load, clamps enabled			16.0	mA
Negative Supply Current	I_{EE}	No load, clamps enabled			16.0	mA
Logic Supply Current	I_L	No load, all digital inputs at rails			1.2	mA
Analog Ground Current	I_{AGND}	No load, clamps enabled			0.9	mA
Digital Ground Current	I_{DGND}	No load, all digital inputs at rails			1.4	mA
Power-Supply Rejection Ratio	PSRR	1MHz, measured at force output		20		dB
		60Hz, measured at force output		85		

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +12V, V_{EE} = -7V, V_L = +3.3V, C_{CM} = 120pF, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FORCE VOLTAGE (Notes 9, 10)						
Settling Time		Range E, R_E = 1MΩ		160		µs
		Range D, R_D = 100kΩ		35		
		Range C, R_C = 10kΩ		25	30	
		Range B, R_B = 1kΩ		20		
		Range A, R_A = 80Ω		25		
Maximum Stable Load Capacitance			2500			pF
FORCE VOLTAGE/MEASURE CURRENT (Notes 9, 10)						
Settling Time		Range E, R_E = 1MΩ		480		µs
		Range D, R_D = 100kΩ		50		
		Range C, R_C = 10kΩ		35	45	
		Range B, R_B = 1kΩ		20		
		Range A, R_A = 80Ω		25		
Range Change Switching		In addition to force-voltage and measure-current settling times, range A to range B, R_A = 80Ω, R_B = 1kΩ		10		µs

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +12V, V_{EE} = -7V, V_L = +3.3V, C_{CM} = 120pF, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FORCE CURRENT (Notes 9, 10)						
Settling Time		Range E, R_E = 1MΩ		300		µs
		Range D, R_D = 100kΩ		100		
		Range C, R_C = 10kΩ		40	45	
		Range B, R_B = 1kΩ		25		
		Range A, R_A = 80Ω		25		
FORCE CURRENT/MEASURE VOLTAGE (Notes 9, 10, 11)						
Settling Time		Range E, R_E = 1MΩ		1600		µs
		Range D, R_D = 100kΩ		170		
		Range C, R_C = 10kΩ		40	50	
		Range B, R_B = 1kΩ		25		
		Range A, R_A = 80Ω		25		
Range Change Switching		In addition to force-voltage and measure-current settling times, range A to range B, R_A = 80Ω, R_B = 1kΩ		12		µs
SENSE INPUT TO MEASURE OUTPUT PATH (Note 11)						
Settling Time		C_{LMSR} = 100pF		0.2		µs
MEASURE OUTPUT						
$\overline{HIZ\_}$ or $\overline{HIZMSR}$ True (0) to High-Z		C_{LMSR} = 100pF, measured from 50% of digital input voltage to 10% of output voltage		250		ns
$\overline{HIZ\_}$ or $\overline{HIZMSR}$ False (1) to Active		C_{LMSR} = 100pF, measured from 50% of digital input voltage to 90% of output voltage		5		µs
Maximum Stable Load Capacitance			1000			pF
FORCE OUTPUT						
$\overline{HIZFORCE}$ True (0) to High-Z		Measured from 50% of digital input voltage to 10% of output voltage		2		µs
$\overline{HIZFORCE}$ False (1) to Active		Measured from 50% of digital input voltage to 90% of output voltage		2		µs
COMPARATORS						
Propagation Delay		50mV overdrive, $1V_{P-P}$, C_{LCOMP} = 20pF, R_{PUP} = 1kΩ measured from input-threshold zero crossing to 50% of output voltage (Note 12)		75		ns
Rise Time		C_{LCOMP} = 20pF, R_{PUP} = 1kΩ measured from input-threshold zero crossing to 50% of output voltage		60		ns
Fall Time		C_{LCOMP} = 20pF, R_{PUP} = 1kΩ, 20% to 80%		5		ns

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +12V, V_{EE} = -7V, V_L = +3.3V, C_{CM} = 120pF, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{DISABLE}$ True (0) to High-Z		C_{LCOMP} = 20pF, measured from 50% of digital input voltage to 10% of output voltage		300		ns
$\overline{DISABLE}$ False (1) to Active		C_{LCOMP} = 20pF, measured from 50% of digital input voltage to 90% of output voltage		100		ns
SERIAL PORT (V_L = +3.0V, C_{DOUT} = 10pF)						
Serial Clock Frequency	f_{SCLK}				20	MHz
SCLK Pulse-Width High	t_{CH}		12			ns
SCLK Pulse-Width Low	t_{CL}		12			ns
SCLK Fall to DOUT Valid	t_{DO}				22	ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		10			ns
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}		22			ns
SCLK High to $\overline{CS}$ Low Hold	t_{CSH0}		0			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		5			ns
DIN to SCLK High Setup	t_{DS}		10			ns
DIN to SCLK High Hold	t_{DH}	(Note 13)	0			ns
$\overline{CS}$ Pulse-Width High	t_{CSWH}		10			ns
$\overline{CS}$ Pulse-Width Low	t_{CSWL}		10			ns
$\overline{LOAD}$ Pulse-Width Low	t_{LDW}		20			ns
V_{DD} High to $\overline{CS}$ Low (Power-Up)		(Note 13)			500	µs

Note 1: The device operates properly with different supply voltages with equally different voltage swings.

Note 2: Tested at V_{CC} = +18V and V_{EE} = -12V.

Note 3: Interpret errors expressed in terms of %FSR (percent of full-scale range) as a percentage of the end-point to end-point range, i.e., for the ±25mA range, the full-scale range = 50mA and a 1% error = 500µA.

Note 4: Case must be maintained ±5°C for linearity specifications.

Note 5: Current linearity specifications are maintained to within 700mV of the clamp voltages when the clamps are enabled.

Note 6: Tested in range C.

Note 7: Linearity of the measured output is only guaranteed within the specified current range.

Note 8: The digital interface accepts +5V, +3.3V, and +2.5V CMOS logic levels. The voltage at V_L adjusts the threshold.

Note 9: Settling times are to 0.1% of FSR. Cx = 47pF.

Note 10: All settling times are specified using a single compensation capacitor (Cx) across all current-sense resistors. Use an individual capacitor across each sense resistor for better performance across all current ranges, particularly the lower ranges.

Note 11: The actual settling time of the measured voltage path (SENSE_ input to MSR_ output) is less than 1µs. However, the R-C time constant of the sense resistor and the load capacitance causes a longer overall settling time of the DUT voltage. This settling time is a function of the current-range resistor used.

Note 12: The propagation delay time is only guaranteed over the force-voltage output range. Propagation delay is measured by holding the SENSE_ input voltage steady and transitioning THMAX_ or THMIN_.

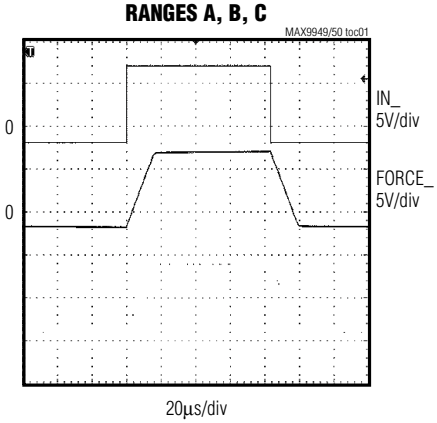
Note 13: Guaranteed by design.

Dual Per-Pin Parametric Measurement Units

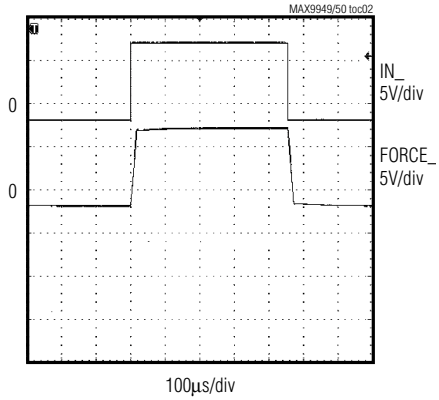
Typical Operating Characteristics

(V_{CC} = +12V, V_{EE} = -7V, C_L = 100pF, R_L to +2.5V, range A: R_A = 80Ω, R_L = 180Ω; range B: R_B = 1kΩ, R_L = 2.25kΩ; range C: R_C = 10kΩ, R_L = 22.5kΩ; range D: R_D = 100kΩ, R_L = 225kΩ; range E: R_E = 1MΩ, R_L = 2.25MΩ, T_A = +25°C.

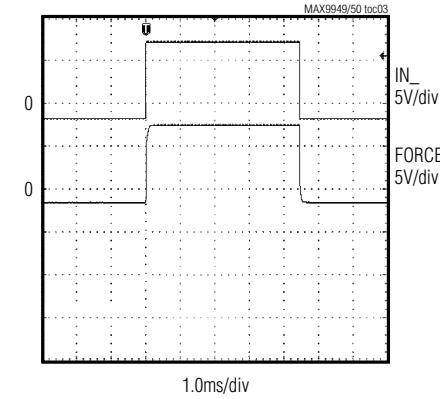
TRANSIENT RESPONSE FVMI MODE RANGES A, B, C



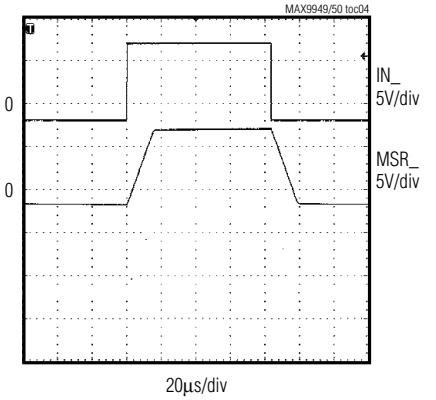
TRANSIENT RESPONSE FVMI MODE RANGE D



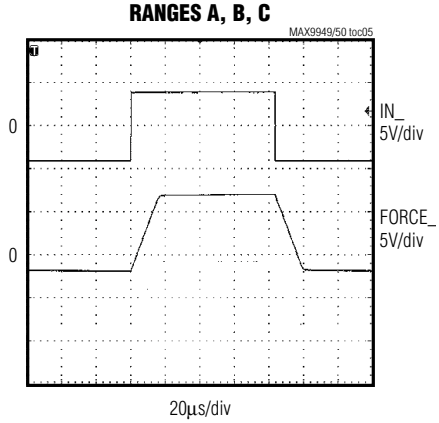
TRANSIENT RESPONSE FVMI MODE RANGE E



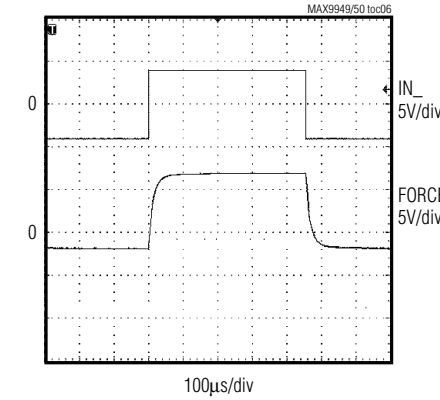
TRANSIENT RESPONSE FVMV MODE RANGE C



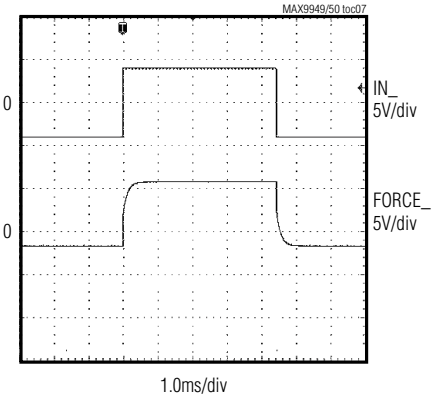
TRANSIENT RESPONSE FIMI MODE RANGES A, B, C



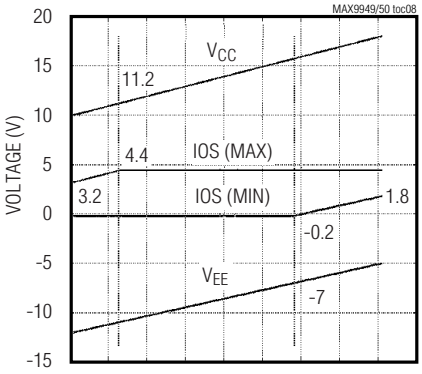
TRANSIENT RESPONSE FIMI MODE RANGE D



TRANSIENT RESPONSE FIMI MODE RANGE E



IOS vs. POWER SUPPLIES



Pin Description

PIN		NAME	FUNCTION
MAX9950	MAX9949		
1, 16, 33, 48	1, 16, 33, 48	V_{EE}	Negative Analog Supply Input
2, 15, 34, 47	2, 15, 34, 47	V_{CC}	Positive Analog Supply Input
3	14	RBCOM	PMU-B Range-Setting-Resistor Common Connection. Connect to one end of all the range-setting resistors (RB_) for PMU-B. Also serves as the input to an external current-range buffer for PMU-B.
4	13	RBE	PMU-B Range E Resistor Connection
5	12	RBD	PMU-B Range D Resistor Connection
6	11	RBC	PMU-B Range C Resistor Connection
7	10	RBB	PMU-B Range B Resistor Connection
8	9	RBA	PMU-B Range A Resistor Connection
9	8	FORCEB	PMU-B Driver Output. Forces a current or voltage to the DUT for PMU-B.
10	7	SENSEB	PMU-B Sense Input. A Kelvin connection to the DUT. Provides the feedback signal in FVMI mode and the measured signal in FIMV mode for PMU-B.
11	6	CC1B	PMU-B Compensation Capacitor Connection 1. Provides compensation for the PMU-B main amplifier.
12	5	CC2B	PMU-B Compensation Capacitor Connection 2. Provides compensation for the PMU-B main amplifier.
13	4	RXDB	PMU-B Current-Range Sense-Resistor Connection. Connects to the external current-range sense resistor on the DUT side for PMU-B. See Figure 5.
14	3	RXAB	PMU-B Current-Range Sense-Resistor Connection. Connects to the external current-range sense resistor on the amplifier side for PMU-B. See Figure 5.
17	64	$\overline{CS}$	Chip-Select Input. Force $\overline{CS}$ low to enable communication with the serial port.
18	63	$\overline{LOAD}$	Serial Port Load Input. A logic low asynchronously loads data from the input registers into the PMU registers.
19	62	SCLK	Serial Clock Input
20	61	DIN	Serial Data Input. Data loads into DIN MSB first.
21	60	$\overline{DUTHB}$	PMU-B Window-Comparator High-Comparator Output. A sense-B voltage above the V_{THMAXB} level forces the $\overline{DUTHB}$ output low. $\overline{DUTHB}$ is an open-drain output.
22	59	$\overline{DUTLB}$	PMU-B Window-Comparator Low-Comparator Output. A sense-B voltage below the V_{THMINB} level forces the $\overline{DUTLB}$ output low. $\overline{DUTLB}$ is an open-drain output.
23	58	EXTBSEL	PMU-B External Current-Range Selector. Selects the external current range for PMU-B.
24, 27	54, 57	DGND	Digital Ground
25	56	DOUT	Serial Data Output. Provides data out from the shift register. Facilitates daisy-chaining to DIN of a downstream PMU. DOUT clocks out data MSB first.
26	55	V_L	Logic Supply Voltage Input. The voltage applied at VL sets the upper logic-voltage level.
28	53	EXTASEL	PMU-A External Current-Range Selector. Selects the external current range for PMU-A.
29	52	$\overline{DUTLA}$	PMU-A Window-Comparator Low-Comparator Output. A sense-A voltage below the V_{THMINA} level forces the $\overline{DUTLA}$ output low. $\overline{DUTLA}$ is an open-drain output.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX9950	MAX9949		
30	51	$\overline{\text{DUTHA}}$	PMU-A Window-Comparator High-Comparator Output. A sense-A voltage above the V_{THMAXA} level forces the $\overline{\text{DUTHA}}$ output low. $\overline{\text{DUTHA}}$ is an open-drain output.
31	50	$\overline{\text{HI-ZB}}$	PMU-B MSRB Output State Control. A logic low places the MSRB output in a high-impedance state.
32	49	$\overline{\text{HI-ZA}}$	PMU-A MSRA Output State Control. A logic low places the MSRA output in a high-impedance state.
35	46	RXAA	PMU-A Current-Range Sense-Resistor Connection. Connects to the external current-range sense resistor on the amplifier side for PMU-A. See Figure 5.
36	45	RXDA	PMU-A Current-Range Sense-Resistor Connection. Connects to the external current-range sense resistor on the DUT side for PMU-A. See Figure 5.
37	44	CC2A	PMU-A Compensation Capacitor Connection 2. Provides compensation for the PMU-A main amplifier.
38	43	CC1A	PMU-A Compensation Capacitor Connection 1. Provides compensation for the PMU-A main amplifier.
39	42	SENSEA	PMU-A Sense Input. A Kelvin connection to the DUT. Provides the feedback signal in FVMI mode and the measured signal in FIMV mode for PMU-A.
40	41	FORCEA	PMU-A Driver Output. Forces a current or voltage to the DUT for PMU-A.
41	40	RAA	PMU-A Range A Resistor Connection
42	39	RAB	PMU-A Range B Resistor Connection
43	38	RAC	PMU-A Range C Resistor Connection
44	37	RAD	PMU-A Range D Resistor Connection
45	36	RAE	PMU-A Range E Resistor Connection
46	35	RACOM	PMU-A Range-Setting-Resistor Common Connection. Connect to one end of all range-setting resistors (RA_) for PMU-A. Also serves as the input to an external current range buffer for PMU-A.
49	32	THMAXA	PMU-A Window-Comparator Upper Threshold Voltage Input. Sets the upper voltage threshold for the PMU-A window comparator.
50	31	THMINA	PMU-A Window-Comparator Lower Threshold Voltage Input. Sets the lower voltage threshold for the PMU-A window comparator.
51	30	CLHIA	PMU-A Upper Clamp Voltage Input. Sets the upper clamp voltage level for PMU-A.
52	29	CLLOA	PMU-A Lower Clamp Voltage Input. Sets the lower clamp voltage level for PMU-A.
53	28	IN0A	Input Voltage 0 for PMU-A. Sets the forced current in FI mode or the forced voltage in FV mode for PMU-A.
54	27	IN1A	Input Voltage 1 for PMU-A. Sets the forced voltage in FV mode or the forced current in FI mode for PMU-A.
55	26	MSRA	PMU-A Measurement Output. Provides a voltage equal to the SENSE voltage in FIMV mode and provides a voltage proportional to the DUT current in FVMI mode for PMU-A. Force $\overline{\text{HI-ZA}}$ low to place MSRA in a high-impedance state.
56	25	IOS	Offset Voltage Input. Sets an offset voltage for the internal current-sense amplifier for both PMU-A and -B.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX9950	MAX9949		
57	24	AGND	Analog Ground
58	23	MSRB	PMU-B Measurement Output. Provides a voltage equal to the SENSE voltage in FIMV mode and provides a voltage proportional to the DUT current in FVMI mode for PMU-B. Force $\overline{HI\text{-}ZB}$ low to place MSRB in a high-impedance state.
59	22	IN1B	Input Voltage 1 for PMU-B. Sets the forced voltage in FV mode or the forced current in FI mode for PMU-B.
60	21	IN0B	Input Voltage 0 for PMU-B. Sets the forced current in FI mode or the forced voltage in FI mode for PMU-B.
61	20	CLLOB	PMU-B Lower-Clamp Voltage Input. Sets the lower clamp voltage level for PMU-B.
62	19	CLHIB	PMU-B Upper-Clamp Voltage Input. Sets the upper clamp voltage level for PMU-B.
63	18	THMINB	PMU-B Window-Comparator Lower Threshold Voltage Input. Sets the lower voltage threshold for the PMU-B window comparator.
64	17	THMAXB	PMU-B Window-Comparator Upper Threshold Voltage Input. Sets the upper voltage threshold for the PMU-B window comparator.

Detailed Description

The MAX9949/MAX9950 force or measure voltages in the -2V to +7V through -7V to +13V ranges, dependent upon the supply voltage range (V_{CC} and V_{EE}). However, the devices can handle supply voltages up to +30V (V_{CC} to V_{EE}) and a 20V DUT voltage swing at full current. The MAX9949/MAX9950 PMU also force or measure currents up to ±25mA, with a lowest full-scale range of ±2µA. Use an external buffer amplifier for current ranges greater than ±25mA.

The MSR_ output presents a voltage proportional to the measured voltage or current. Place MSR_ in a low-leakage, high-impedance state by pulling $\overline{HI\text{-}Z\_}$ low. Integrated comparators with externally programmable voltage thresholds provide "too low" ($\overline{DUTL\_}$) and "too high" ($\overline{DUTH\_}$) voltage-monitoring outputs. Each comparator output features a selectable high-impedance state. The devices feature separate FORCE_ and SENSE_ connections and are fully protected against short circuits. The FORCE_ output has two voltage clamps, negative (CLLO_) and positive (CLHI_), to limit the voltage to externally provided levels. Two control voltage inputs, selected independently of the PMU mode, allow for greater flexibility.

Serial Interface

The MAX9949/MAX9950 use a standard 3-wire SPI™/QSPI™/MICROWIRE™-compatible serial port. Once the input data register fills, the data becomes available at DOUT MSB first. This data output allows for daisy-chaining multiple devices. Figures 1, 2, and 3 show the serial interface timing diagrams.

Serial Port Speed

The serial port timing specifications are measured at a logic supply voltage (V_L) of +3.0V, ensuring operation of the serial port at rated speed for V_L from +3.0V to +5.5V.

The serial interface has two ranks. Each PMU has an input register that loads from the serial port shift register. Each PMU also has a PMU register that loads from the input register. Data does not affect the PMU until it reaches the PMU register. This register configuration permits loading of the PMU data into the input register at one time and then latching the input register data into the PMU register later, at which time the PMU function changes accordingly. The register configuration also provides the ability to change the state of the PMU asynchronously with respect to the loading of that PMU's data into the serial port. Thus, the PMU easily updates simultaneously with other PMUs or other devices.

Use the $\overline{LOAD}$ input to asynchronously load all input registers into the PMU registers. If $\overline{LOAD}$ remains low when data latches into an input register, the data also transfers to the PMU register.

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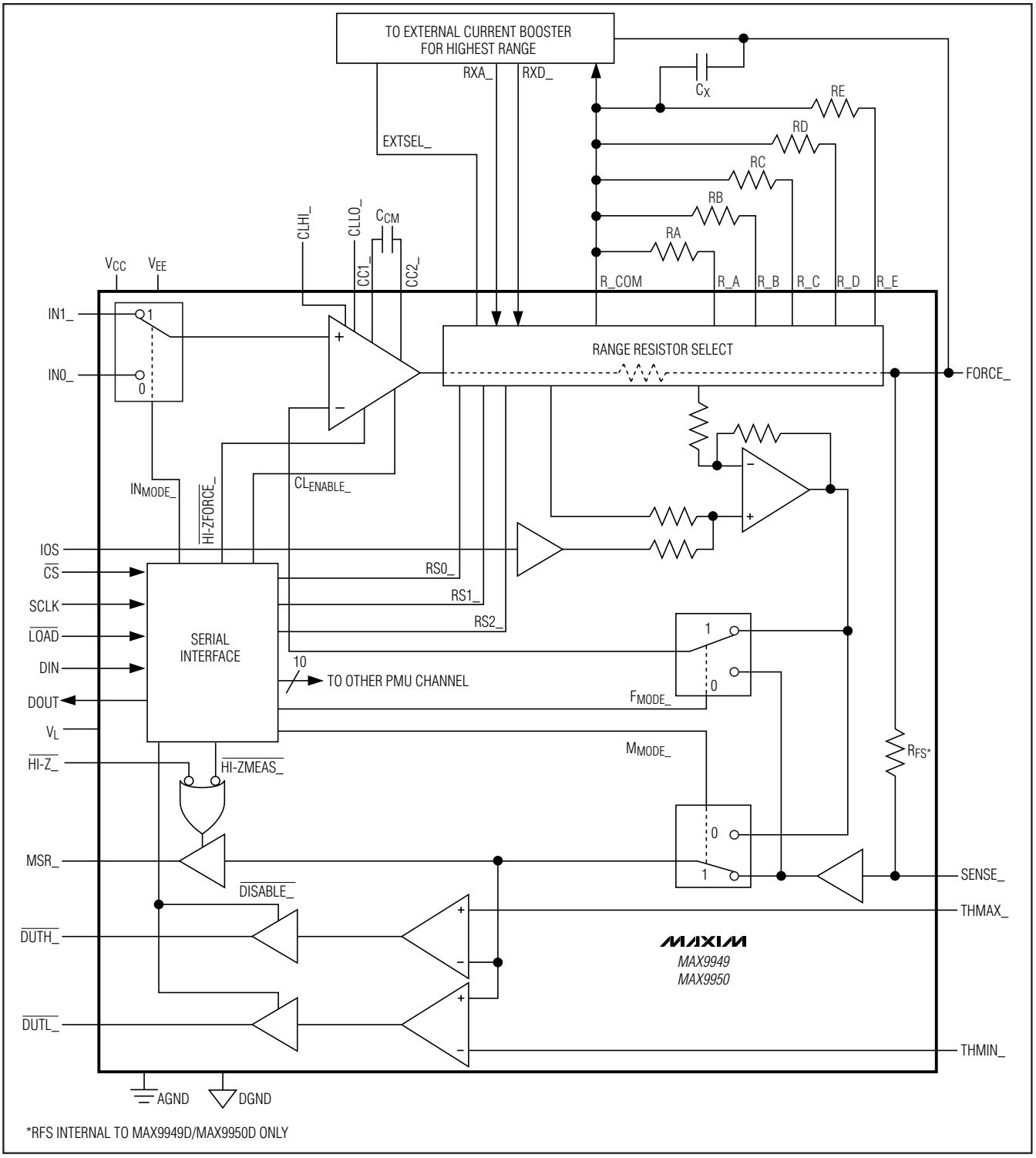
MICROWIRE is a trademark of National Semiconductor, Corp.

Dual Per-Pin Parametric Measurement Units

Functional Diagram



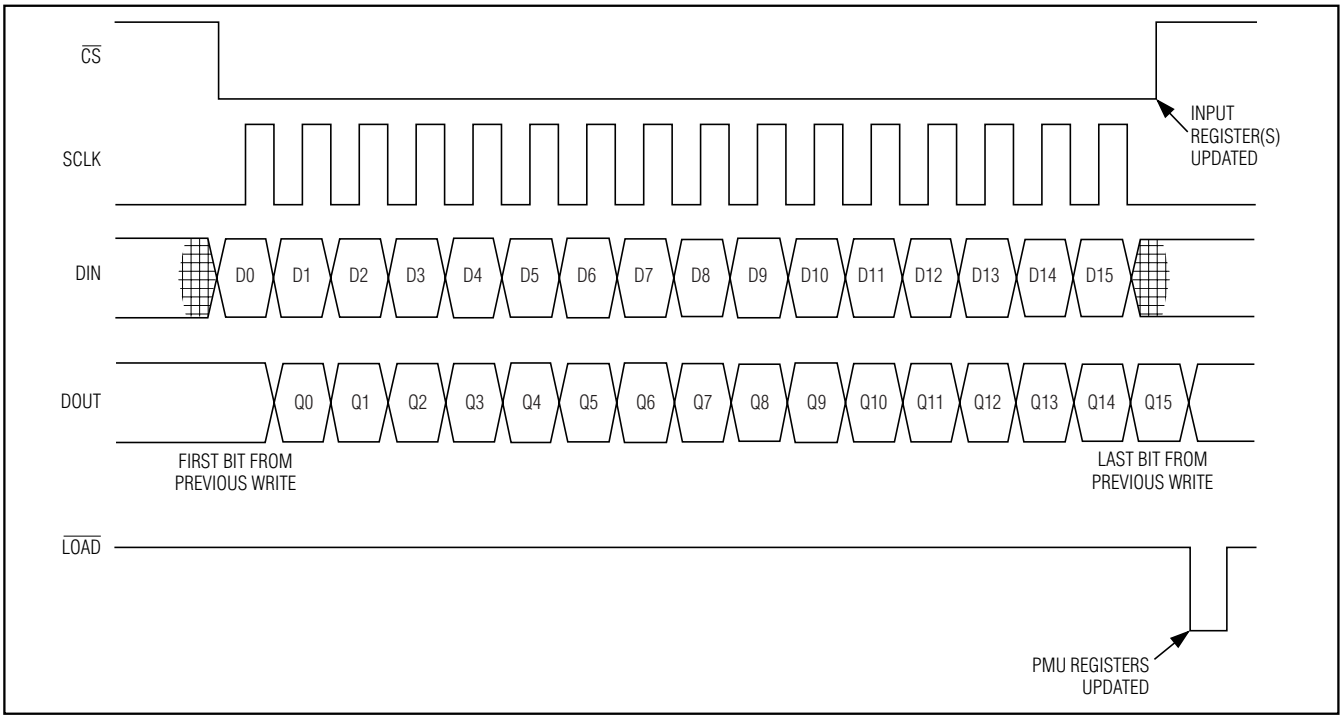


Figure 1. Serial Port Timing with Asynchronous Load

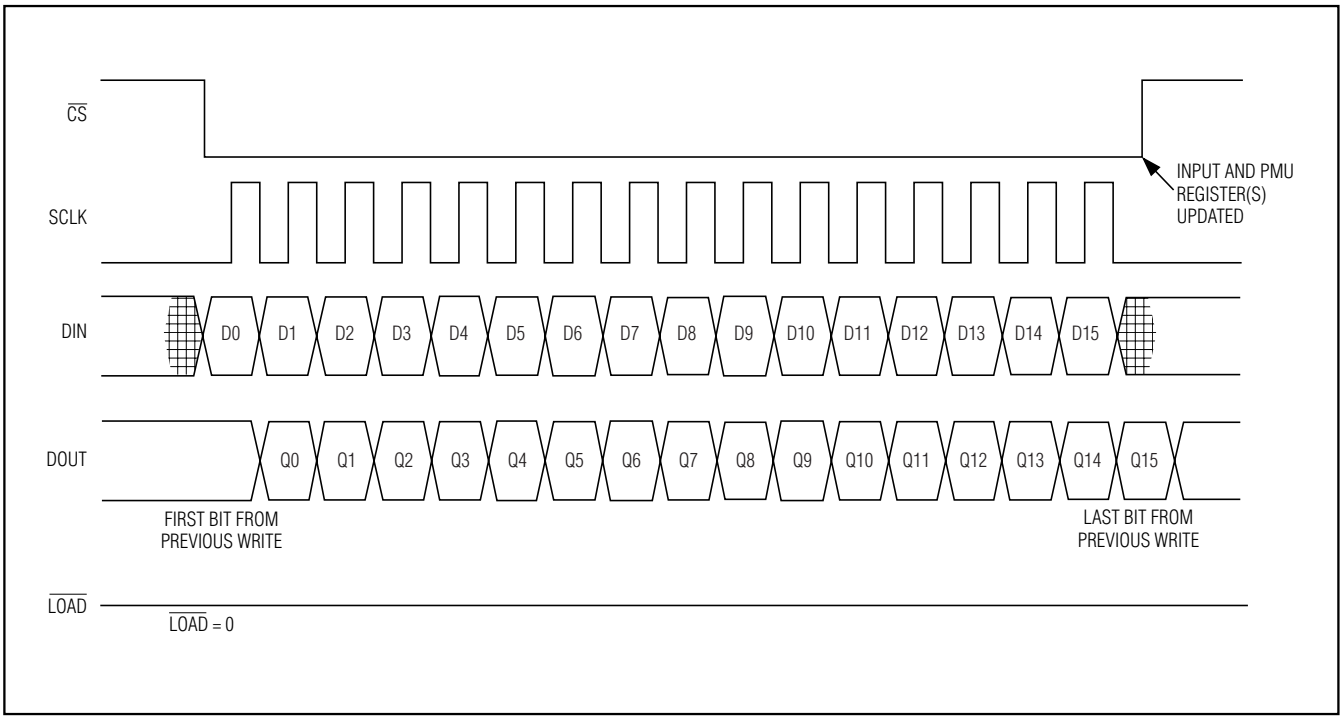


Figure 2. Serial Port Timing with Synchronous Load

Dual Per-Pin Parametric Measurement Units

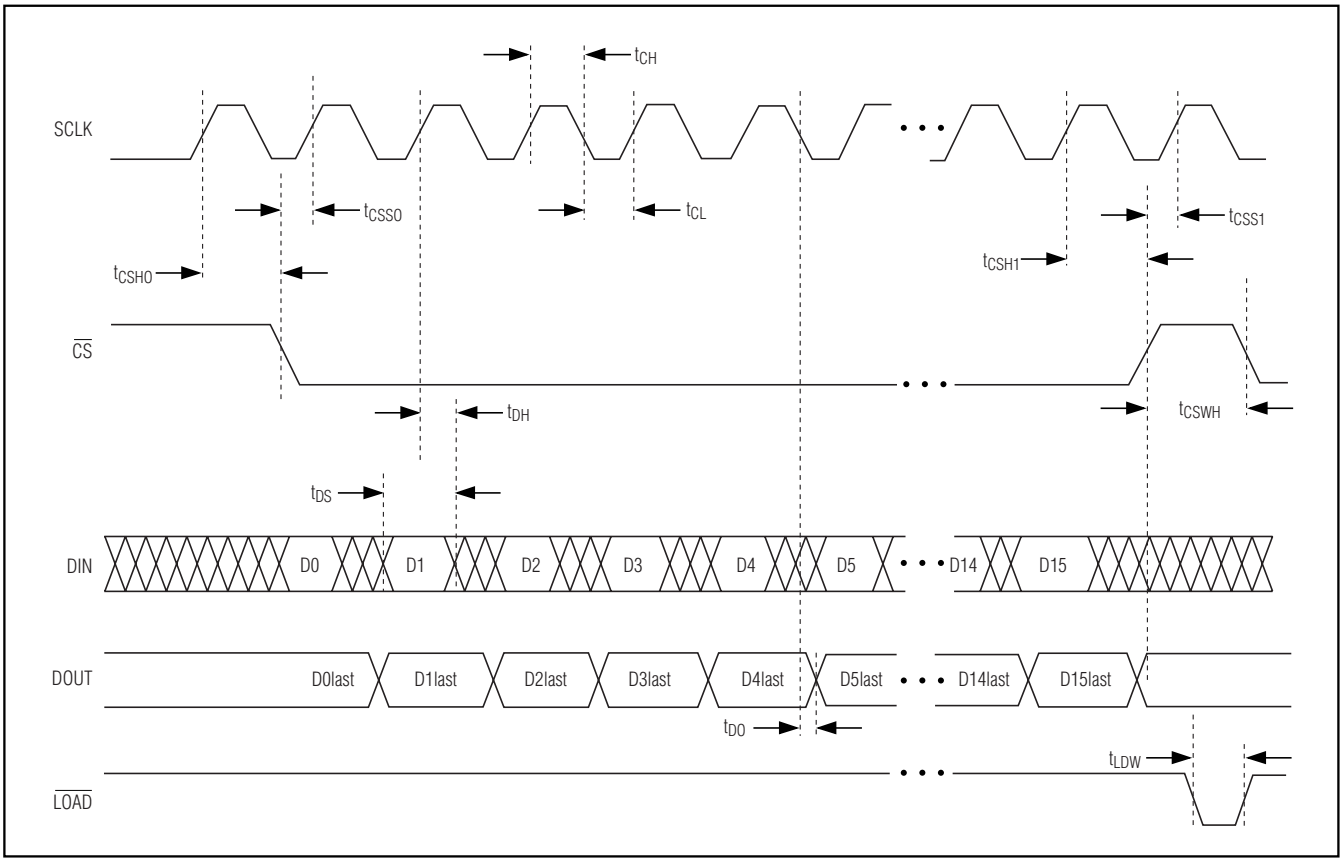


Figure 3. Detailed Serial Port Timing Diagram

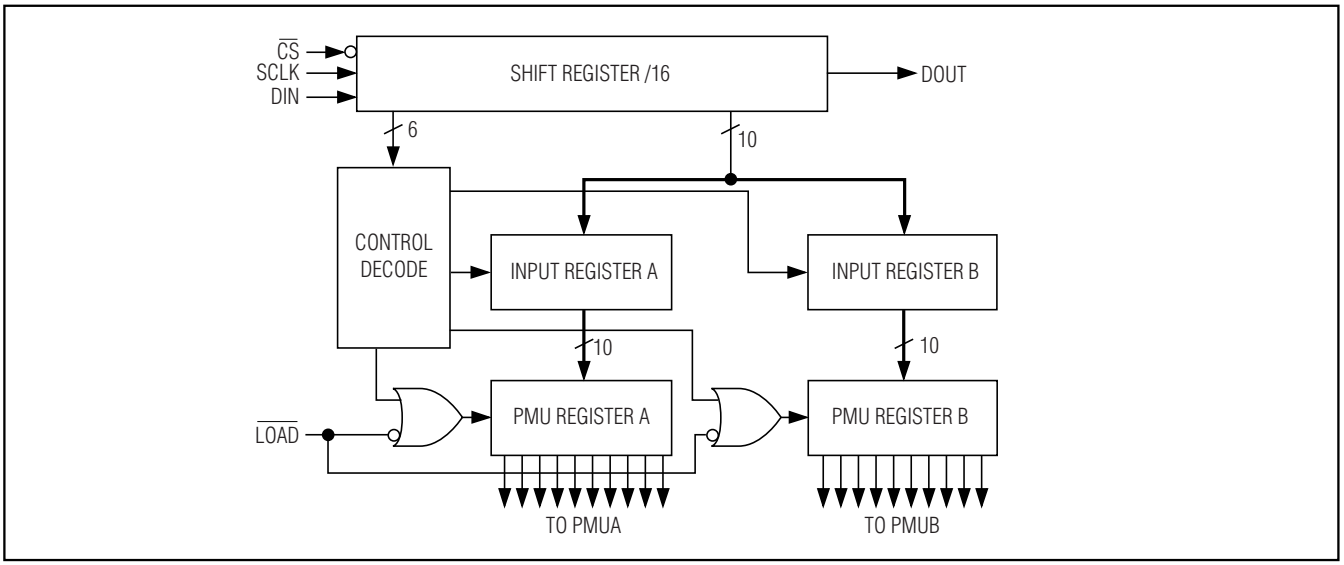


Figure 4. Dual PMU Serial Port Block Diagram

Table 1. Bit Order

BIT	BIT NAME
15 (MSB)	IN_{MODE}
14	F_{MODE}
13	M_{MODE}
12	RS2
11	RS1
10	RS0
9	CL_{ENABLE}
8	$\overline{HI\text{-}ZFORCE}$
7	$\overline{HI\text{-}ZMSR}$
6	$\overline{DISABLE}$
5	Don't care
4	Don't care
3	A2
2	A1
1	C2
0 (LSB)	C1

Table 2. Address Bit

(BIT 3) A2	(BIT 2) A1	OPERATION
0	0	Do not update any input register (NOP).
0	1	Only update input register A.
1	0	Only update input register B.
1	1	Update both input registers with the same data.

Table 3. Control Bit

(BIT 1) C2	(BIT 0) C1	OPERATION
0	0	Data stays in input register.
0	1	Transfer PMU-A input register to PMU register.
1	0	Transfer PMU-B input register to PMU register.
1	1	Transfer both input registers to the PMU registers.

Bit Order

The MAX9949/MAX9950 use the bit order, MSB first in and first out, as shown in Table 1.

PMU Control

Programming both PMUs with the same data requires a 16-bit word. Programming each PMU with separate data requires two 16-bit words.

The address bits specify which input registers the shift register loads. Table 2 describes the function of the address bits.

Bits (C2, C1) specify how the data loads into the second rank PMU registers. These two control bits serve a similar function as the $\overline{LOAD}$ input. The specified actions occur when $\overline{CS}$ goes high, whereas the $\overline{LOAD}$ input loads the PMU register anytime. When either C2 or C1 is low, the corresponding PMU register is transparent. Table 3 describes the function of the two control bits.

The NOP operation requires A1 = A2 = C1 = C2 = 0. In this case, the data transfers through the shift register without changing the state of the MAX9949/MAX9950.

C1 = C2 = 0 allows for data transfer from the shift register to the input register without transferring data to the PMU register (unless the $\overline{LOAD}$ input is low). This permits the latching of data into the PMU register at a later time by the $\overline{LOAD}$ input or subsequent command.

Table 4 summarizes the possible control and address bit combinations.

When asynchronously latching only one PMU's data, the input register of the other PMU maintains the same data. Therefore, loading both PMU registers would update the one PMU with new data while the other PMU remains in its current state.

Mode Selection

Four bits from the control word select between the various modes of operation. IN_{MODE} selects between the two input analog control voltages. F_{MODE} selects whether the PMU forces a voltage or a current. M_{MODE} selects whether the DUT current or DUT voltage is directed to the MSR_ output. $\overline{HI\text{-}ZFORCE}$ places the driver amplifier in a high-output impedance state. Table 5 describes the various force and measure modes of operation.

Current-Range Selection

Three bits from the control word, RS0, RS1, RS2, control the full-scale current range for either FI (force current) or MI (measure current). Table 6 describes the full-scale current-range control.

Table 4. PMU Operation Using Control and Address Bits

BIT (3:2)		BIT (1:0)		PMU-B OPERATION	PMU-A OPERATION
A2	A1	C2	C1		
0	0	0	0	NOP: data just passes through.	
0	0	0	1	NOP.	Load PMU register A from input register A.
0	0	1	0	Load PMU register B from input register B.	NOP.
0	0	1	1	Load PMU register B from input register B.	Load PMU register A from input register A.
0	1	0	0	NOP.	Load input register A from shift register.
0	1	0	1	NOP.	Load input register A and PMU register A from shift register.
0	1	1	0	Load PMU register B from input register B.	Load input register A from shift register.
0	1	1	1	Load PMU register B from input register B.	Load input register A and PMU register A from shift register.
1	0	0	0	Load input register B from shift register.	NOP.
1	0	0	1	Load input register B from shift register.	Load PMU register A from input register A.
1	0	1	0	Load input register B and PMU register B from shift register.	NOP.
1	0	1	1	Load input register B and PMU register B from shift register.	Load PMU register A from input register A.
1	1	0	0	Load input register B from shift register.	Load input register A from shift register.
1	1	0	1	Load input register B from shift register.	Load input register A and PMU register A from shift register.
1	1	1	0	Load input register B and PMU register B from shift register.	Load input register A from shift register.
1	1	1	1	Load input register B and PMU register B from shift register.	Load input register A and PMU register A from shift register.

Table 5. PMU Force/Measure Mode Selection

(BIT 15) IN MODE	(BIT 14) F MODE	(BIT 13) M MODE	(BIT 8) $\overline{\text{HI-Z}}$FORCE	PMU MODE	FORCE OUTPUT	MEASURE OUTPUT	ACTIVE INPUT
0	0	0	1	FVMI	Voltage	I_{DUT}	V_{IN0}
1	0	0	1	FVMI	Voltage	I_{DUT}	V_{IN1}
0	0	1	1	FVMV	Voltage	V_{DUT}	V_{IN0}
1	0	1	1	FVMV	Voltage	V_{DUT}	V_{IN1}
0	1	0	1	FIMI	Current	I_{DUT}	V_{IN0}
1	1	0	1	FIMI	Current	I_{DUT}	V_{IN1}
0	1	1	1	FIMV	Current	V_{DUT}	V_{IN0}
1	1	1	1	FIMV	Current	V_{DUT}	V_{IN1}
x	x	0	0	FNMI—Meaningless mode			
x	x	1	0	FNMV	HI-Z	V_{DUT}	x

Table 6. Current Range Selection

(BIT 12) RS2	(BIT 11) RS1	(BIT 10) RS0	RANGE	NOMINAL RESISTOR VALUE
0	0	0	±2µA	R_E = 1MΩ
0	0	1	±2µA	R_E = 1MΩ
0	1	0	±20µA	R_D = 100kΩ
0	1	1	±200µA	R_C = 10kΩ
1	0	0	±2mA	R_B = 1kΩ
1	0	1	±25mA	R_A = 80Ω
1	1	0	External	—
1	1	1	±25mA	R_A = 80Ω

Table 7. Clamp Enable

CL_{ENABLE}	MODE
1	Clamps enabled
0	Clamps disabled

Clamp Enable

The CL_{ENABLE} bit enables the force-output voltage clamps when high and disables the clamps when low. Table 7 depicts the various clamp mode options.

Measure Output High-Impedance Control

The MSR_ output attains a low-leakage, high-impedance state by using the $\overline{HI\text{-}ZMSR}$ control bit or the $\overline{HI\text{-}Z\_}$ input. The 2 bits are logically ORed together to control the MSR_ output. The $\overline{HI\text{-}Z\_}$ input allows external multiplexing among several PMU MSR_ outputs without using the serial interface. Table 8 explains the various output modes for the MSR_ output.

Digital Output (DOUT)

The digital output follows the last output of the serial shift register and clocks out on the falling edge of the input clock. DOUT provides the first bit of the incoming serial data word 16.5 clock cycles later. This allows for daisy-chaining an additional device using DOUT and the same clock.

Table 8. MSR_ Output Truth Table

(BIT 7) $\overline{HI\text{-}ZMSR}$	$\overline{HI\text{-}Z\_}$	MSR_ STATE
1	1	Measure output enabled
0	1	High-Z
1	0	High-Z
0	0	High-Z

"Quick Load" Using Chip Select

If $\overline{CS}$ goes low and then returns high without any clock activity, the data from the input registers latch into the PMU registers. This extra function is not standard for SPI/QSPI/MICROWIRE interfaces. The quick load mimics the function of $\overline{LOAD}$ without forcing $\overline{LOAD}$ low.

Comparators

Two comparators configured as a window comparator monitor the MSR_ output. THMAX_ and THMIN_ set the high and low thresholds that determine the window. Both outputs are open drain and share a single disable control that places the outputs in a high-Z, low-leakage state. Table 9 describes the comparator output states of the MAX9949/MAX9950.

Table 9. Comparator Truth Table

(BIT 6) $\overline{DISABLE}$	CONDITION	$\overline{DUTH\_}$	$\overline{DUTL\_}$
0	X	High-Z	High-Z
1	$V_{MSR} > V_{THMAX}$ and V_{THMIN}	0	1
1	$V_{THMAX} > V_{MSR} > V_{THMIN}$	1	1
1	V_{THMAX} and $V_{THMIN} > V_{MSR}$	1	0
1	$V_{THMIN} > V_{MSR} > V_{THMAX}$*	0	0

**$V_{THMAX} > V_{THMIN}$ constitutes normal operation. This condition, however, has $V_{THMIN} > V_{THMAX}$ and does not cause any problems with the operation of the comparators.*

Dual Per-Pin Parametric Measurement Units

Applications Information

In force-voltage (FV) mode, the output FORCE_ voltage is directly proportional to the input control voltage. In force-current (FI) mode, the current flowing out of the FORCE_ output is proportional to the input control voltage. Positive current flows out of the PMU.

In force-nothing (FN) mode, the FORCE_ output is high impedance.

In measure-current (MI) mode, the voltage at the MSR_ output is directly proportional to the current exiting the FORCE_ output. Positive current flows out of the PMU.

In measure-voltage (MV) mode, the voltage at the MSR_ output is directly proportional to the voltage at the SENSE_ input.

Current-Sense-Amplifier Offset Voltage Input

IOS is a buffered input to the current-sense amplifier. The current-sense amplifier converts the input control voltage (IN0_ or IN1_) to the forced DUT current (FI) AND converts the sensed DUT current to the MSR_ output voltage (MI). When IOS equals zero relative to DUT-GND (the GND voltage at the DUT, which the level-setting DACs and the ADC are presumed to use as a ground reference), the nominal voltage range that corresponds to ± full-scale current is -4V to +4V. Any voltage applied to the IOS input adds directly to this control input/measure output voltage range, i.e., applying +4V to IOS forces the voltage range that corresponds to ± full-scale current from 0 to +8V.

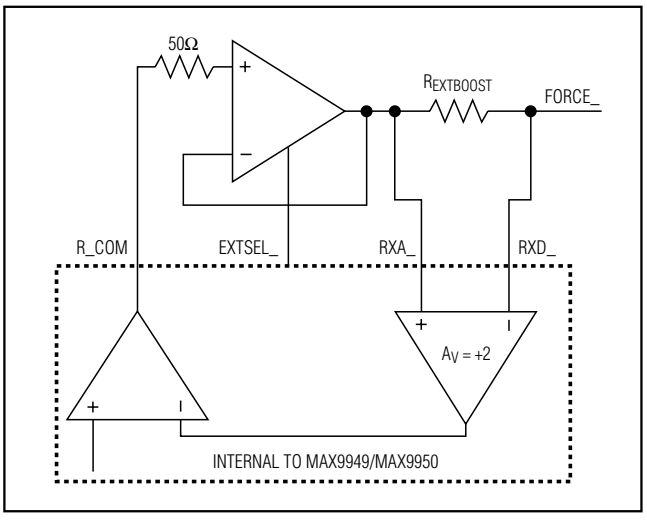


Figure 5. External Current Boost

The following equations determine the minimum and maximum currents for each current range corresponding to the input voltage or measure voltage:

$$V_{MAXCURRENT} = V_{IOS} + 4V$$

$$V_{MINCURRENT} = V_{IOS} - 4V$$

Choose IOS so the limits of the MSR_ output do not go closer than 2.8V to either V_{EE} or V_{CC}. For example, with supplies of +10V and -5V, limit the MSR_ output to -2.2V and +7.2V. Therefore, set IOS between +1.8V and +3.2V. The MSR_ output could clip if IOS is not within this range. Use these general equations for the limits on IOS:

$$\text{Minimum } V_{IOS} = V_{EE} + 6.8V$$

$$\text{Maximum } V_{IOS} = V_{CC} - 6.8V$$

Current Booster for Highest Current Range

An external buffer amplifier can be used to provide a current range greater than the MAX9949/MAX9950 maximum output current (Figure 5). This function operates as follows.

A digital output decoded from the range select bits, EXTSEL_, indicates when to activate the booster. The R_COM output serves as an input to an external buffer through a 50Ω current-limit series resistor. Each side of the external current-sense resistor feeds back to RXA_ and RXD_. Ensure that the buffer circuit enters a high-Z output state when not selected. Any leakage in the buffer adds to the leakage of the PMU.

Voltage Clamps

The voltage clamps limit the FORCE_ output and operate over the entire specified current range. Set the clamp voltages externally at CLHI_ and CLLO_. The voltage at the FORCE_ output triggers the clamps independent of the voltage at the SENSE_ input. When enabled, the clamps function in both FI and FV modes.

Current Limit

The current-limiting circuitry on the FORCE_ output ensures a well-behaved MSR_ output for currents between the full current range and the current limits, i.e., for currents greater than the full-scale current, the MSR_ voltage is greater than +4V and for currents less than the full-scale current, the MSR_ voltage is less than -4V.

Independent Control of the Feedback Switch and the Measure Switch

Two single-pole-double-throw (SPDT) switches determine the mode of operation of the PMU. One switch determines whether the sensed DUT current or DUT voltage feeds back to the input (sensing), and thus

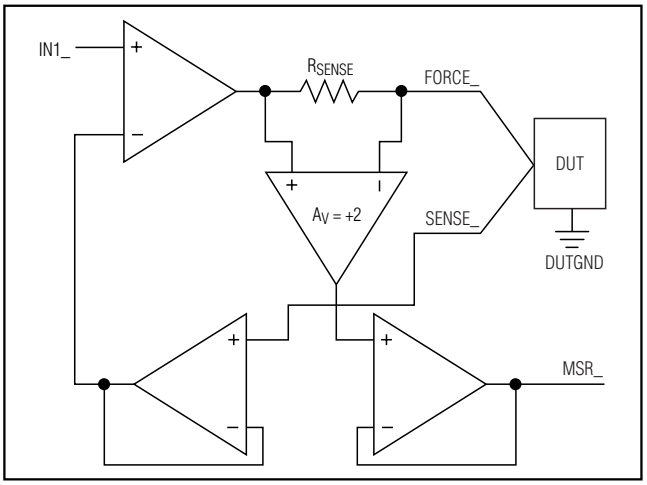


Figure 6. Force-Voltage/Measure-Current Functional Diagram

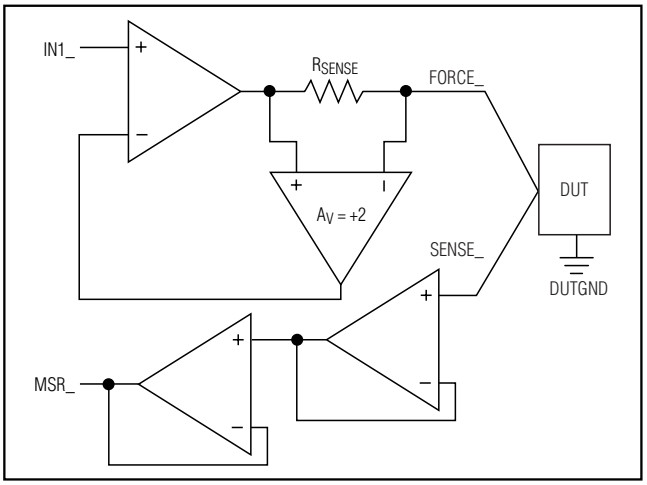


Figure 7. Force-Current/Measure-Voltage Functional Diagram

determines whether the MAX9949/MAX9950 force current or voltage. The other switch determines whether the MSR_ output senses the DUT current or DUT voltage.

Independent control of these switches and the HI-ZFORCE state permits flexible modes of operation beyond the traditional force-voltage/measure-current (FVMI) and force-current/measure-voltage (FIMV) modes. The MAX9949/MAX9950 support the following five modes:

- FVMI
- FIMV
- FVMV
- FIMI
- FNMV

Figure 6 shows the internal path structure for force-voltage/measure-current mode. In force-voltage/measure-current mode, the current across the appropriate external sense resistor (R_A to R_E) provides a voltage to the MSR_ output. The SENSE_ input samples the voltage at the DUT and feeds the buffered result back to the negative input of the voltage amplifier. The voltage at MSR_ is proportional to the FORCE_ current in accordance with the following formula:

$$V_{MSR\_} = I_{FORCE\_} \times R_{SENSE} \times 2$$

Figure 7 shows the internal path structure for the force-current/measure-voltage mode. In force-current/measure-voltage mode, the appropriate external sense resistor (R_A to R_E) provides a feedback voltage to the inverting input of the voltage amplifier. The SENSE_ input samples the voltage at the DUT and provides a buffered result at the MSR_ output.

High-Z States

The FORCE_, MSR_, and comparator outputs feature individual high-Z control that places them into a high-impedance, low-leakage state. The high-Z state allows busing of MSR_ and comparator outputs with other PMU measure and comparator outputs. The FORCE_ output high-Z state allows for additional modes of operation as described in Table 5 and can eliminate the need for a series relay in some applications.

The FORCE_, MSR_, and comparator outputs power up in the high-Z state.

Input Source Selection and Gating

Either one of two input signals, IN0_ or IN1_, can control both the forced voltage and the forced current. In this case, the two input signals represent alternate forcing values that can be selected with the serial interface. Alternatively, each input signal can be dedicated to control a single forcing function (i.e., voltage or current).

Ground, DUT Ground, IOS

The MAX9949/MAX9950 utilize two local grounds, AGND (analog ground) and DGND (digital ground). Connect AGND and DGND together on the PC board. In a typical ATE system, the PMU force voltage is relative to the DUT ground. In this case, reference the input voltages IN0_ and IN1_ to the DUT ground. Similarly, reference IOS to the DUT ground. If it is not desired to offset the current control and measure voltages, connect IOS to the DUT ground potential.

Reference the MSR_ output to the DUT ground.

Dual Per-Pin Parametric Measurement Units

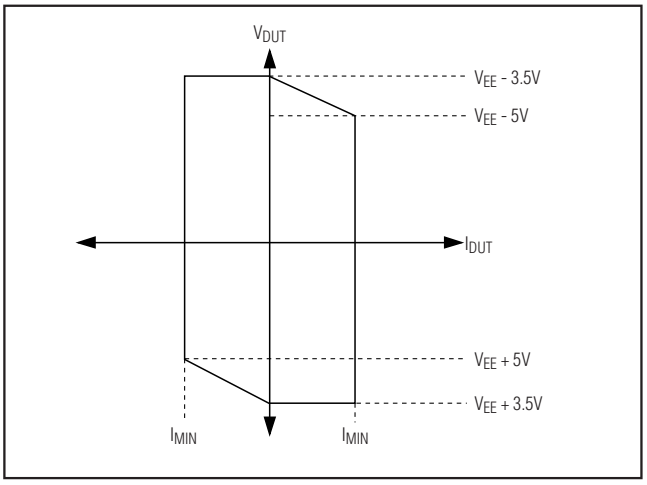


Figure 8. PMU Force Output Capability

Short-Circuit Protection

The FORCE_ output and SENSE_ input can withstand a short to any voltage between the supply rails.

Mode and Range Change Transients

The MAX9949/MAX9950 feature make-before-break switching to minimize glitches. The integrated voltage clamps also reduce glitching on the output.

DUT Voltage Swing vs. DUT Current and Power-Supply Voltages

Several factors limit the actual DUT voltage that the PMU delivers:

1) The overhead required by the amplifiers and other integrated circuitry—this is typically 3.5V from each rail for no load current and 5V under full load
2) The voltage drop across the current-range select resistor and internal circuitry in series with the sense resistor—at full current, the combined voltage drop is typically 2.75V
3) Variations in the power supplies—system implementation determines the variance
4) Variation of DUT ground vs. PMU ground—system implementation determines the variance

Neglecting the effects of the third and fourth items, Figure 8 demonstrates the force output capabilities of the PMU.

Figure 8 indicates that, for zero DUT current, the DUT voltage swings from (V_{EE} + 3.5V) to (V_{CC} - 3.5V). For larger positive DUT currents, the positive swing drops off linearly until it reaches (V_{CC} - 5V) at full current. Similarly, for larger negative DUT currents, the negative voltage swing drops off linearly until it reaches (V_{EE} + 5V) at full current.

Settling Times and Compensation Capacitors

The data in the *Electrical Characteristics* table reflects the circuit shown in the block diagram that includes a single compensation capacitor (Cx) effectively across all the sense resistors. Placing individual capacitors, C_{RA}, C_{RB}, C_{RC}, C_{RD}, and C_{RE} directly across the sense resistors, R_A, R_B, R_C, R_D, and R_E, independently optimizes each range.

The combination of the capacitance across the sense resistors (Cx or C_{RA}, C_{RB}, C_{RC}, C_{RD}, and C_{RE}) and the main amplifier compensation comparator, C_{CM}, ensures stability into the maximum expected load capacitance while optimizing settling time.

Digital Inputs (SCLK, DIN, $\overline{CS}$, $\overline{LOAD}$)

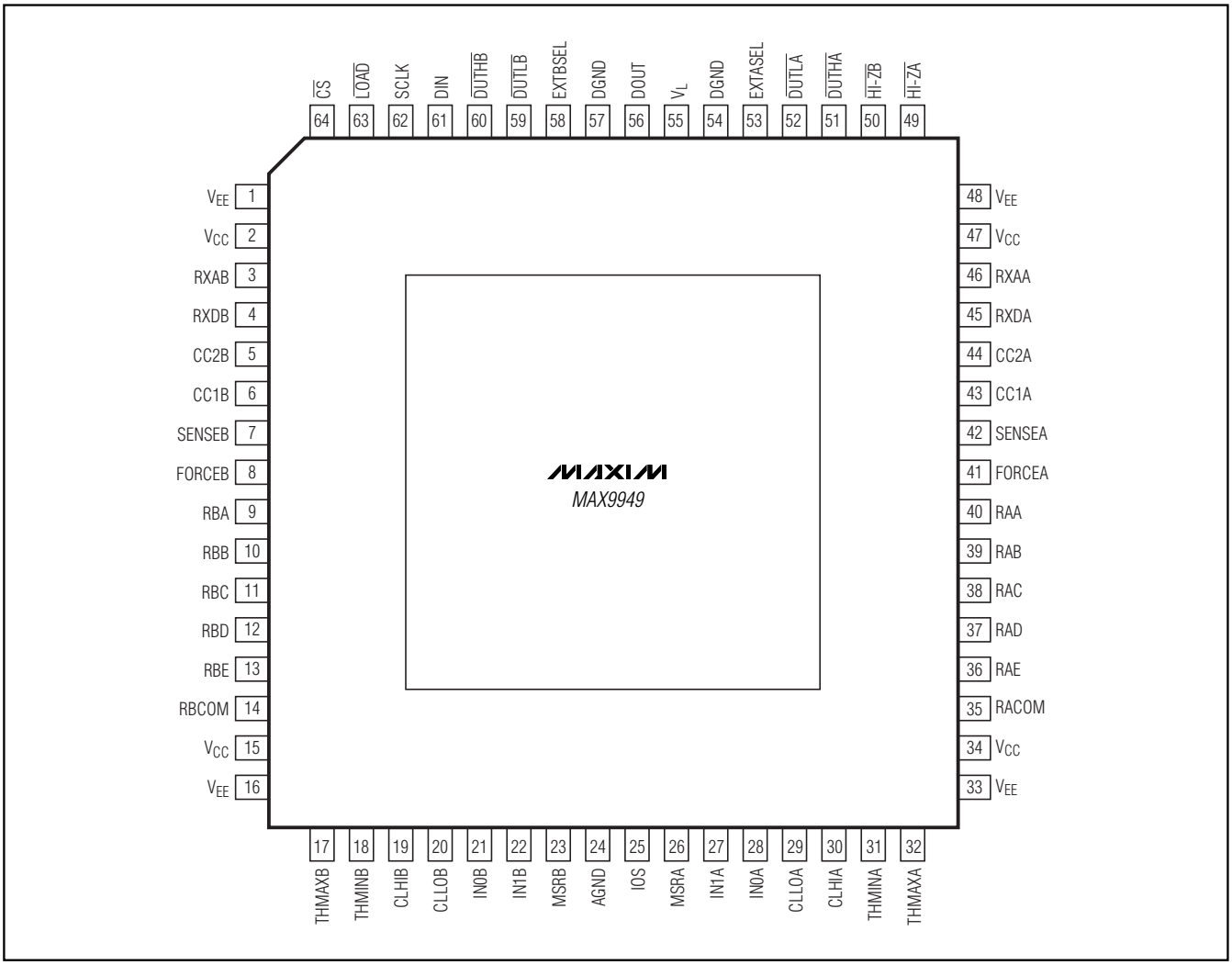
The digital inputs incorporate hysteresis to mitigate issues with noise, as well as provide for compatibility with opto-isolators that can have slow edges.

Chip Information

TRANSISTOR COUNT: 7800

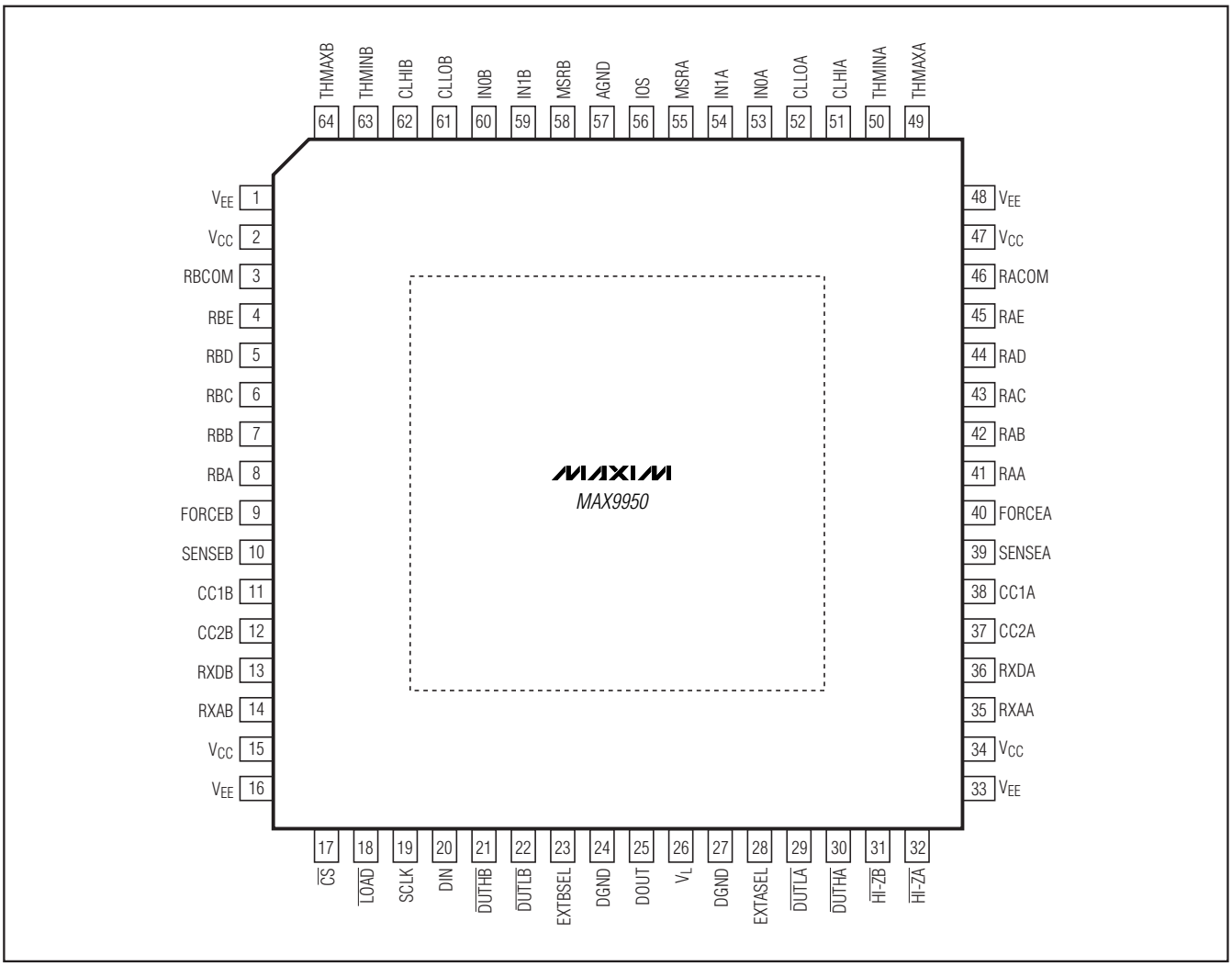
PROCESS: BiCMOS

MAX9949 Pin Configuration



Dual Per-Pin Parametric Measurement Units

MAX9950 Pin Configuration



Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.