

Section 14 Electrical Specifications

14.1 Absolute Maximum Ratings

Table 14-1 gives the absolute maximum ratings for the H8/3724 Series.

Table 14-1 Absolute Maximum Ratings (provisional values)

Item	Symbol	Rating	Unit	Notes
Supply voltage	V_{CC}	-0.3 to +7.0	V	1, 2
Programming voltage	V_{PP}	-0.3 to +14.0	V	1, 2, 3
Analog supply voltage	AV_{CC}	-0.3 to +7.0	V	1, 2
Analog input voltage	AV_{IN}	-0.3 to $AV_{CC} + 0.3$	V	1, 2
Pin voltage (standard pins)	V_T	-0.3 to $V_{CC} + 0.3$	V	1, 2, 4
Pin voltage (high-voltage pins)	V_T	$V_{CC} - 45$ to $V_{CC} + 0.3$	V	1, 2, 5
Operating temperature	T_{op}	-20 to +75	°C	1, 2
Storage temperature	T_{stg}	-55 to +125	°C	1, 2

- Notes:
1. Operation in excess of these absolute maximum ratings may result in permanent damage to the LSI. Normally the LSI should be operated within the conditions given under electrical characteristics on the following pages, so as to avoid malfunction and assure maximum reliability.
 2. All voltages are based on V_{SS} as a reference voltage.
 3. Applies to the ZTAT™ version.
 4. Applies to standard-voltage pins.
 5. Applies to high-voltage pins.

14.2 HD6473724 and HD6473726 Electrical Characteristics

14.2.1 HD6473724 and HD6473726 DC Characteristics

Table 14-2 gives the allowable current values of the HD6473724 and HD6473726, and table 14-3 gives the electrical characteristics.

Table 14-2 Allowable Current Sink Values

Conditions: $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Rating	Unit	Notes
Allowable input current (into LSI)	I_O	2	mA	1, 2
Allowable output current (from LSI)	$-I_O$	2	mA	2, 3
Allowable output current (from LSI)	$-I_O$	20	mA	3, 4
Total allowable input current (into LSI)	ΣI_O	50	mA	5
Total allowable output current (from LSI)	$-\Sigma I_O$	150	mA	6

- Notes:
1. Allowable input current means the maximum current that can flow from each I/O pin to V_{SS} .
 2. Applies to standard-voltage pins.
 3. Allowable output current means the maximum current that can flow from V_{CC} to each I/O pin.
 4. Applies to high-voltage pins.
 5. Total allowable input current means the sum of current that can flow at one time from all I/O pins to V_{SS} .
 6. Total allowable output current means the sum of current that can flow from V_{CC} to all I/O pins.

Table 14-3 DC Characteristics

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{disp} = V_{CC} - 40$ to V_{CC} ,
 $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes	
				Min	Typ	Max			
Input high voltage	V_{IH}	\overline{RES}		$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V		
		$\overline{IRQ_0}$ to $\overline{IRQ_5}$							
		SCK_1, SCK_2 SI_1, SI_2	$V_{CC} = 2.7$ to 5.5 V incl. subactive mode	$0.9 V_{CC}$	—	$V_{CC} + 0.3$			
		\overline{EVENT}, UD	$V_{CC} = 2.7$ to 5.5 V incl. subactive mode	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V		
		OSC_1			$V_{CC} - 0.5$	—	$V_{CC} + 0.3$	V	
				$V_{CC} = 2.7$ to 5.5 V incl. subactive mode	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$		
		$P0_0$ to $P0_7$ $P1_0$ to $P1_6$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0 to PA_1	$V_{CC} = 2.7$ to 5.5 V incl. subactive mode	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V		
Input low voltage	V_{IL}	$\overline{RES},$ SCK_1, SCK_2		-0.3	—	$0.2 V_{CC}$	V		
		$\overline{IRQ_0}$ to $\overline{IRQ_5}$ SI_1, SI_2	$V_{CC} = 2.7$ to 5.5 V incl. subactive mode	-0.3	—	$0.1 V_{CC}$			
		\overline{EVENT}, UD	$V_{CC} = 2.7$ to 5.5 V incl. subactive mode	-0.3	—	$0.3 V_{CC}$	V		
		OSC_1			-0.3	—	0.5	V	
				$V_{CC} = 2.7$ to 5.5 V incl. subactive mode	-0.3	—	0.3		
		$P0_1$ to $P0_7$ $P1_0$ to $P1_6$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0 to PA_1	$V_{CC} = 2.7$ to 5.5 V incl. subactive mode	-0.3	—	$0.3 V_{CC}$	V		
		$P3_0$ to $P3_3$ $P4_0$ to $P4_7$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P1_7$	$V_{CC} = 2.7$ to 5.5 V incl. subactive mode	$V_{CC} - 40$	—	$0.3 V_{CC}$	V		

Note: TEST pin should be connected to V_{SS} .

Table 14-3 DC Characteristics (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{disp} = V_{CC} - 40$ to V_{CC} ,
 $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Output high voltage	V_{OH}	P1 ₀ to P1 ₅	$-I_{OH} = 1.0$ mA	$V_{CC} - 1.0$	—	—	V	
		P8 ₀ to P8 ₇						
		P9 ₀ to P9 ₇	$-I_{OH} = 0.5$ mA	$V_{CC} - 0.5$	—	—		
		PWM, SO ₁ , SO ₂	$V_{CC} = 2.7$ to 5.5 V	$V_{CC} - 0.5$	—	—		
		PA ₀ , PA ₁	$-I_{OH} = 0.3$ mA					
		P3 ₀ to P3 ₃	$-I_{OH} = 15$ mA	$V_{CC} - 3.0$	—	—	V	
Output low voltage	V_{OL}	P4 ₀ to P4 ₇	$-I_{OH} = 10$ mA	$V_{CC} - 2.0$	—	—		
		P5 ₀ to P5 ₇	$-I_{OH} = 4$ mA	$V_{CC} - 1.0$	—	—		
		P6 ₀ to P6 ₇						
		P7 ₀ to P7 ₇	$V_{CC} = 2.7$ to 5.5 V	—	$V_{CC} - 1.0$	—	V	Reference value
			$-I_{OH} = 4$ mA					
Output low voltage	V_{OL}	P1 ₀ to P1 ₅	$V_{CC} = 4.0$ to 5.5 V	—	—	0.4	V	
		P8 ₀ to P8 ₇	$I_{OL} = 1.6$ mA					
		P9 ₀ to P9 ₇						
		PWM, SO ₁ , SO ₂	$V_{CC} = 2.7$ to 5.5 V	—	0.4	—	V	Reference value
Input leakage current	I_{IL}	RES	$V_{IN} = 0$ to V_{CC}			40	μA	

Table 14-3 DC Characteristics (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{disp} = V_{CC} - 40$ to V_{CC} ,
 $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
I/O leakage current	I_{IL}	TEST SCK ₁ , SCK ₂ SI ₁ , SI ₂ IRQ ₀ to IRQ ₅ EVENT, UD OSC ₁ P0 ₁ to P0 ₇ P1 ₀ to P1 ₆ P8 ₀ to P8 ₇ P9 ₀ to P9 ₇ PA ₀ , PA ₁	$V_{IN} = 0$ to V_{CC}	—	—	1	μA	
		P3 ₀ to P3 ₃ P4 ₀ to P4 ₇ P5 ₀ to P5 ₇ P6 ₀ to P6 ₇ P7 ₀ to P7 ₇ P1 ₇	$V_{IN} = V_{CC} - 40$ to V_{CC}	—	—	20	μA	
Input capacitance	C_{IN}	Input pins and I/O pins other than power source pin	$f = 1$ MHz, $V_{IN} = 0$ V $T_a = 25^\circ\text{C}$	—	—	20	pF	
		P1 ₆ /EVENT		—	—	35		
		RES		—	—	70		

Table 14-3 DC Characteristics (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{disp} = V_{CC} - 40$ to V_{CC} ,
 $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Power dissipation when CPU operating in active mode	I_{OPE}	V_{CC}	$V_{CC} = 5$ V, $f_{OSC} = 8$ MHz	—	17	—	mA	Reference value 1
			$V_{CC} = 5$ V, $f_{OSC} = 4$ MHz	—	9	—		
			$V_{CC} = 3$ V, $f_{OSC} = 4$ MHz	—	6	—		
Power dissipation during reset in active mode	I_{RES}	V_{CC}	$V_{CC} = 5$ V, $f_{OSC} = 8$ MHz	—	6	9	mA	1
			$V_{CC} = 5$ V, $f_{OSC} = 4$ MHz	—	3	5		
			$V_{CC} = 3$ V, $f_{OSC} = 4$ MHz	—	1.5	—		
Power dissipation in sleep mode	I_{SLEEP}	V_{CC}	$V_{CC} = 5$ V, $f_{OSC} = 8$ MHz	—	2.5	3.5	mA	1
			$V_{CC} = 5$ V, $f_{OSC} = 4$ MHz	—	1.5	2.0		
			$V_{CC} = 3$ V, $f_{OSC} = 4$ MHz	—	1.0	—		
Power dissipation in subactive mode	I_{SUB}	V_{CC}	$V_{CC} = 2.7$ V 32 kHz crystal oscillator used	—	6	20	μA	2
			$V_{CC} = 5.0$ V 32 kHz crystal oscillator used	—	11	—		
			$V_{CC} = 5.0$ V 32 kHz crystal oscillator used	—	16	—	μA	Reference value 2
			$V_{CC} = 5.0$ V 32 kHz crystal oscillator used	—	22	—		
Power dissipation in watch mode	I_{WATCH}	V_{CC}	$V_{CC} = 2.7$ V 32 kHz crystal oscillator used	—	3.2	6	μA	2
			$V_{CC} = 5.0$ V 32 kHz crystal oscillator used	—	3.8	—		
			$V_{CC} = 5.0$ V 32 kHz crystal oscillator used	—	10	—	μA	Reference value 2
			$V_{CC} = 5.0$ V 32 kHz crystal oscillator used	—	12	—		
Power dissipation in standby mode	I_{STBY}	V_{CC}	32 kHz crystal oscillator not used $X_1 = V_{CC}$	—	—	10	μA	

Table 14-3 DC Characteristics (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{disp} = V_{CC} - 40$ to V_{CC} ,
 $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
RAM data retention voltage in standby mode	V_{STBY}	V_{CC}	32 kHz crystal oscillator not used $X_1 = V_{CC}$	2	—	—	V	

Notes: 1. Does not include current flowing to output buffer.
2. Reference value when bypass capacitor of 47 μF is connected between V_{CC} and V_{SS} .

14.2.2 HD6473724 and HD6473726 AC Characteristics

Regarding the AC characteristics, Table 14-4 gives the control signal timing of HD6473724 and HD6473726, and Table 14-5 gives the serial interface timing.

Table 14-4 Control Signal Timing

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{disp} = V_{CC} - 40$ to V_{CC} , $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
Clock pulse generator frequency	f_{OSC}	OSC ₁ , OSC ₂	$V_{CC} = 2.7$ to 5.5 V	2	—	8.4	MHz	
				2	—	4.2		
Clock cycle time	t_{CYC}	OSC ₁ , OSC ₂	$V_{CC} = 2.7$ to 5.5 V	119	—	500	ns	Figure 14-1
				238	—	500		
Instruction cycle time	ϕ		$V_{CC} = 2.7$ to 5.5 V	238	—	1000	ns	
				476	—	1000		
Subclock pulse generator frequency	f_x	X ₁ , X ₂	$V_{CC} = 2.7$ to 5.5 V	—	32.768	—	kHz	
Subclock cycle time	t_{subcyc}	X ₁ , X ₂	$V_{CC} = 2.7$ to 5.5 V	—	30.5	—	μs	
Subactive instruction cycle time	ϕ_{SUB}		$V_{CC} = 2.7$ to 5.5 V	—	244.14	—	μs	
Oscillator settling time (crystal oscillator)	t_{rc}	OSC ₁ , OSC ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	40	ms	
				—	—	60		
Oscillator settling time (ceramic oscillator)	t_{rc}	OSC ₁ , OSC ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	20	ms	
				—	—	40		
Oscillator settling time	t_{rc}	X ₁ , X ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	2	s	
External clock pulse width (high)	t_{CPH}	OSC ₁	$V_{CC} = 2.7$ to 5.5 V	40	—	—	ns	Figure 14-1
				100	—	—		
External clock pulse width (low)	t_{CPL}	OSC ₁	$V_{CC} = 2.7$ to 5.5 V	40	—	—	ns	
				100	—	—		
External clock rise time	t_{CPr}	OSC ₁	$V_{CC} = 2.7$ to 5.5 V	—	—	20	ns	
				—	—	20		
External clock fall time	t_{CPf}	OSC ₁	$V_{CC} = 2.7$ to 5.5 V	—	—	20	ns	
				—	—	20		

Table 14-4 Control Signal Timing (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{disp} = V_{CC} - 40$ to V_{CC} , $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
RES pin pulse width (low)	t_{REL}	RES	$V_{CC} = 2.7$ to 5.5 V	10	—	—	ϕ	Figure 14-2
IRQ pin pulse width (high)	t_{IH}	IRQ ₀ to IRQ ₅	$V_{CC} = 2.7$ to 5.5 V	2	—	—	ϕ ϕ_{SUB}	Figure 14-3
IRQ pin pulse width (low)	t_{IL}	IRQ ₀ to IRQ ₅	$V_{CC} = 2.7$ to 5.5 V	2	—	—	ϕ ϕ_{SUB}	
EVENT pin pulse width (high)	t_{EVH}	EVENT	$V_{CC} = 2.7$ to 5.5 V	2	—	—	ϕ	Figure 14-4
EVENT pin pulse width (low)	t_{EVL}	EVENT	$V_{CC} = 2.7$ to 5.5 V	2	—	—	ϕ	
UD pin minimum change width	t_{UDH} t_{UDL}	UD	$V_{CC} = 2.7$ to 5.5 V	2	—	—	ϕ	Figure 14-5

Table 14-5 Serial Interface Timing

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{disp} = V_{CC} - 40$ to V_{CC} , $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
Output transfer clock cycle time	t_{scyc}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	2	—	—	ϕ	Figure 14-6
Output transfer clock pulse width (high)	t_{SCKH}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	0.4	—	—	t_{scyc}	
Output transfer clock pulse width (low)	t_{SCKL}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	0.4	—	—	t_{scyc}	
Output transfer clock rise time	t_{SCKr}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	60	ns	
Output transfer clock fall time	t_{SCKf}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	60	ns	
Input transfer clock cycle time	t_{scyc}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	1	—	—	ϕ	
Input transfer clock pulse width (high)	t_{SCKH}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	0.4	—	—	t_{scyc}	

Table 14-5 Serial Interface Timing (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{disp} = V_{CC} - 40$ to V_{CC} , $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram	
				Min	Typ	Max			
Input transfer clock pulse width (low)	t_{SCKL}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	0.4	—	—	t_{scyc}	Figure 14-6	
Input transfer clock rise time	t_{SCKr}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	60	ns		
				—	—	80			
Input transfer clock fall time	t_{SCKf}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	60	ns		
				—	—	80			
Serial output data delay time	t_{dSO}	SO ₁ , SO ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	200	ns		
				—	—	350			
Serial input data setup time	t_{sSI}	SI ₁ , SI ₂	$V_{CC} = 2.7$ to 5.5 V	230	—	—	ns		
				470	—	—			
Serial input data hold time	t_{hSI}	SI ₁ , SI ₂	$V_{CC} = 2.7$ to 5.5 V	230	—	—	ns		
				470	—	—			
Transfer hold time	t_{SCK2}	SCK ₂	$V_{CC} = 2.7$ to 5.5 V	When pin SCK ₂ is input pin	0.2	—	40	μs	Figure 14-7
				When pin SCK ₂ is input pin	0.4	—	40		
				When pin SCK ₂ is output pin	—	—	1		
Transfer end acknowledge time	t_{CS}	\overline{CS}	$V_{CC} = 2.7$ to 5.5 V	3	—	4	ϕ		

14.2.3 HD6473724 and HD6473726 A/D Converter Characteristics

Table 14-6 gives the HD6473724 and HD6473726 A/D converter characteristics.

Table 14-6 A/D Converter Characteristics

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{disp} = V_{CC} - 40$ to V_{CC} , $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Analog supply voltage	AV_{CC}	AV_{CC}		$V_{CC} - 0.3$	V_{CC}	$V_{CC} + 0.3$	V	
Analog input voltage	AV_{IN}	AN_0 to AN_7		AV_{SS}	—	AV_{CC}	V	
Analog current	AI_{CC}	AV_{CC}	$AV_{CC} = 5$ V	—	—	200	μA	
	AI_{STOP}		Reset and power-down mode	—	—	10	μA	
Analog input capacitance	C_{AIN}	AN_0 to AN_7		—	—	30	pF	
Allowable signal source impedance	R_{AIN}	AN_0 to AN_7		—	—	10	$k\Omega$	
Resolution				—	—	8	Bit	
Absolute precision			$V_{CC} = AV_{CC} = 5$ V	—	—	± 2.5	LSB	Reference value
			$V_{CC} = AV_{CC} = 4.0$ to 5.5 V	—	± 2.5	—		
Conversion time				31	15.5	14.8	μs	

14.3 HD6433723, HD6433724, HD6433725, and HD6433726 Electrical Characteristics

14.3.1 HD6433723, HD6433724, HD6433725, and HD6433726 DC Characteristics

Table 14-7 gives the allowable current values of the HD6433723, HD6433724, HD6433725, and HD6433726 and table 14-8 gives the electrical characteristics.

Table 14-7 Allowable Current Sink Values

Conditions: $V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Rating	Unit	Notes
Allowable input current (into LSI)	I_O	2	mA	1, 2
Allowable output current (from LSI)	$-I_O$	2	mA	2, 3
Allowable output current (from LSI)	$-I_O$	20	mA	3, 4
Total allowable input current (into LSI)	$\sum I_O$	50	mA	5
Total allowable output current (from LSI)	$-\sum I_O$	150	mA	6
Total allowable output current to V_{disp}	$-\sum I_O$	30	mA	7

- Notes:
1. Allowable input current means the maximum current that can flow from each I/O pin to V_{SS} .
 2. Applies to standard-voltage pins.
 3. Allowable output current means the maximum current that can flow from V_{CC} to each I/O pin.
 4. Applies to high-voltage pins.
 5. Total allowable input current means the sum of current that can flow at one time from all I/O pins to V_{SS} .
 6. Total allowable output current means the sum of current that can flow from V_{CC} to all I/O pins.
 7. Total allowable output current to V_{disp} is the sum of current that can flow from all I/O pins to V_{disp} .

Table 14-8 DC Characteristics

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{disp} = V_{CC} - 40$ to V_{CC} ,
 $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Input high voltage	V_{IH}	\overline{RES}		$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	
		$\overline{IRQ_0}$ to $\overline{IRQ_5}$						
		SCK_1, SCK_2 SI_1, SI_2	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	$0.9 V_{CC}$	—	$V_{CC} + 0.3$		
		\overline{EVENT}, UD	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	
		OSC_1		$V_{CC} - 0.5$	—	$V_{CC} + 0.3$	V	
			$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$		
		$P0_0$ to $P0_7$ $P1_0$ to $P1_6$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0, PA_1	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	
Input low voltage	V_{IL}	$\overline{RES},$ SCK_1, SCK_2		-0.3	—	$0.2 V_{CC}$	V	
		$\overline{IRQ_0}$ to $\overline{IRQ_5}$ SI_1, SI_2	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	-0.3	—	$0.1 V_{CC}$		
		\overline{EVENT}, UD	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	-0.3	—	$0.3 V_{CC}$	V	
		OSC_1		-0.3	—	0.5	V	
			$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	-0.3	—	0.3		
		$P0_1$ to $P0_7$ $P1_0$ to $P1_6$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0, PA_1	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	-0.3	—	$0.3 V_{CC}$	V	
		$P3_0$ to $P3_3$ $P4_0$ to $P4_7$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P1_7$	$V_{CC} = 2.5$ to 5.5 V incl. subactive mode	$V_{CC} - 40$	—	$0.3 V_{CC}$	V	

Note: TEST pin should be connected to V_{SS} .

Table 14-8 DC Characteristics (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{disp} = V_{CC} - 40$ to V_{CC} , $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes		
				Min	Typ	Max				
Output high voltage	V_{OH}	P1 ₀ to P1 ₅	$-I_{OH} = 1.0$ mA	$V_{CC} - 1.0$	—	—	V			
		P8 ₀ to P8 ₇	$-I_{OH} = 0.5$ mA	$V_{CC} - 0.5$	—	—				
		P9 ₀ to P9 ₇	$V_{CC} = 2.7$ to 5.5 V	$V_{CC} - 0.5$	—	—				
				PWM, SO ₁ , SO ₂ , PA ₀ , PA ₁	$-I_{OH} = 0.3$ mA					
				P3 ₀ to P3 ₃	$-I_{OH} = 15$ mA	$V_{CC} - 3.0$	—	—	V	
				P4 ₀ to P4 ₇	$-I_{OH} = 10$ mA	$V_{CC} - 2.0$	—	—		
		P5 ₀ to P5 ₇	$-I_{OH} = 4$ mA	$V_{CC} - 1.0$	—	—				
		P6 ₀ to P6 ₇	$V_{CC} = 2.7$ to 5.5 V	—	$V_{CC} - 1.0$	—	V	Reference value		
		P7 ₀ to P7 ₇	$-I_{OH} = 4$ mA							
Output low voltage	V_{OL}	P1 ₀ to P1 ₅	$V_{CC} = 4.0$ to 5.5 V	—	—	0.4	V			
		P8 ₀ to P8 ₇	$I_{OL} = 1.6$ mA							
				P9 ₀ to P9 ₇	$V_{CC} = 2.7$ to 5.5 V	—	0.4	—	V	Reference value
				PWM, SO ₁ , SO ₂ , PA ₀ , PA ₁	$I_{OL} = 0.5$ mA					
		P3 ₀ to P3 ₃	$V_{disp} = V_{CC} - 40$ V	—	—	$V_{CC} - 37$	V	With pull-down MOS		
		P4 ₀ to P4 ₇								
		P5 ₀ to P5 ₇								
		P6 ₀ to P6 ₇	Pull-down resistance	—	—	$V_{CC} - 37$				
		P7 ₀ to P7 ₇	150 k Ω ; pull-down voltage $V_{CC} - 40$ V							
Input leakage current	I_{IL}	\bar{RES}	Mask ROM version: $V_{IN} = 0$ to V_{CC}	—	—	1	μA			

Table 14-8 DC Characteristics (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{disp} = V_{CC} - 40$ to V_{CC} ,
 $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
I/O leakage current	I_{IL}	TEST SCK ₁ , SCK ₂ SI ₁ , SI ₂ IRQ ₀ to IRQ ₅ EVENT, UD OSC ₁ P0 ₁ to P0 ₇ P1 ₀ to P1 ₆ P8 ₀ to P8 ₇ P9 ₀ to P9 ₇ PA ₀ , PA ₁	$V_{IN} = 0$ to V_{CC}	—	—	1	μA	
		P3 ₀ to P3 ₃ P4 ₀ to P4 ₇ P5 ₀ to P5 ₇ P6 ₀ to P6 ₇ P7 ₀ to P7 ₇ P1 ₇	$V_{IN} = V_{CC} - 40$ to V_{CC}	—	—	20	μA	Not including pins with pull-down MOS
Pull-up MOS current	$-I_p$	P1 ₀ to P1 ₆ P8 ₀ to P8 ₇ P9 ₀ to P9 ₇ PA ₀ , PA ₁	$V_{CC} = 5$ V, $V_{IN} = 0$ V	50	—	300	μA	
			$V_{CC} = 2.7$ V, $V_{IN} = 0$ V	—	25	—		Reference value
Pull-down MOS current	I_d	P3 ₀ to P3 ₃ P4 ₀ to P4 ₇ P5 ₀ to P5 ₇ P6 ₀ to P6 ₇ P7 ₀ to P7 ₇	$V_{disp} = V_{CC} - 36$ $V_{IN} = V_{CC}$	120	—	800	μA	
			$V_{disp} = V_{CC} - 18$ $V_{IN} = V_{CC}$	—	280	—		Reference value
Input capacitance	C_{IN}	Input pins other than power source pin	$f = 1$ MHz, $V_{IN} = 0$ V $T_a = 25^\circ\text{C}$	—	—	15	pF	
		P1 ₇		—	—	30		

Table 14-8 DC Characteristics (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{disp} = V_{CC} - 40$ to V_{CC} ,
 $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Power dissipation when CPU operating in active mode	I_{OPE}	V_{CC}	$V_{CC} = 5$ V, $f_{OSC} = 8$ MHz	—	15	—	mA	Reference value 1
			$V_{CC} = 5$ V, $f_{OSC} = 4$ MHz	—	8	—		
			$V_{CC} = 3$ V, $f_{OSC} = 4$ MHz	—	5	—		
Power dissipation during reset in active mode	I_{RES}	V_{CC}	$V_{CC} = 5$ V, $f_{OSC} = 8$ MHz	—	5	8	mA	1
			$V_{CC} = 5$ V, $f_{OSC} = 4$ MHz	—	2.5	4		
			$V_{CC} = 3$ V, $f_{OSC} = 4$ MHz	—	1.3	—		
Power dissipation in sleep mode	I_{SLEEP}	V_{CC}	$V_{CC} = 5$ V, $f_{OSC} = 8$ MHz	—	2	3	mA	1
			$V_{CC} = 5$ V, $f_{OSC} = 4$ MHz	—	1	1.5		
			$V_{CC} = 3$ V, $f_{OSC} = 4$ MHz	—	0.6	—		
Power dissipation in subactive mode	I_{SUB}	V_{CC}	$V_{CC} = 2.5$ V 32 kHz crystal oscillator used	—	5	20	μA	
				—	9	—		
			$V_{CC} = 5.0$ V 32 kHz crystal oscillator used	—	13	—	μA	Reference value
				—	20	—	μA	2
Power dissipation in watch mode	I_{WATCH}	V_{CC}	$V_{CC} = 2.5$ V 32 kHz crystal oscillator used	—	2.2	5	μA	
				—	2.8	—		
			$V_{CC} = 5.0$ V 32 kHz crystal oscillator used	—	6	—	μA	Reference value
				—	8	—	μA	2
Power dissipation in standby mode	I_{STBY}	V_{CC}	32 kHz crystal oscillator not used $X_1 = V_{CC}$	—	—	5	μA	

Table 14-8 DC Characteristics (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{disp} = V_{CC} - 40$ to V_{CC} ,
 $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
RAM data retention voltage in standby mode	V_{STBY}	V_{CC}	32 kHz crystal oscillator not used $X_1 = V_{CC}$	2	—	—	V	

Notes: 1. Does not include current flowing to pull-up MOS or output buffer.
2. Reference value when bypass capacitor of $47 \mu\text{F}$ is connected between V_{CC} and V_{SS} .

14.3.2 HD6433723, HD6433724, HD6433725, and HD6433726 AC Characteristics

As for the AC characteristics, Table 14-9 gives the control signal timing of HD6433723, HD6433724, HD6433725, and HD6433726, while Table 14-10 gives the serial interface timing.

Table 14-9 Control Signal Timing

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{disp} = V_{CC} - 40$ to V_{CC} , $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
Clock pulse generator frequency	f_{OSC}	OSC ₁ , OSC ₂	$V_{CC} = 2.7$ to 5.5 V	2	—	8.4	MHz	
				2	—	4.2		
Clock cycle time	t_{CYC}	OSC ₁ , OSC ₂	$V_{CC} = 2.7$ to 5.5 V	119	—	500	ns	Figure 14-1
				238	—	500		
Instruction cycle time	ϕ		$V_{CC} = 2.7$ to 5.5 V	238	—	1000	ns	
				476	—	1000		
Subclock pulse generator frequency	f_x	X ₁ , X ₂	$V_{CC} = 2.5$ to 5.5 V	—	32.768	—	kHz	
Subclock cycle time	t_{subcyc}	X ₁ , X ₂	$V_{CC} = 2.5$ to 5.5 V	—	30.5	—	μs	
Subactive instruction cycle time	ϕ_{SUB}		$V_{CC} = 2.5$ to 5.5 V	—	244.14	—	μs	
Oscillator settling time (crystal oscillator)	t_{rc}	OSC ₁ , OSC ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	40	ms	
				—	—	60		
Oscillator settling time (ceramic oscillator)	t_{rc}	OSC ₁ , OSC ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	20	ms	
				—	—	40		
Oscillator settling time	t_{rc}	X ₁ , X ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	2	s	
External clock pulse width (high)	t_{CPH}	OSC ₁	$V_{CC} = 2.7$ to 5.5 V	40	—	—	ns	Figure 14-1
				100	—	—		
External clock pulse width (low)	t_{CPL}	OSC ₁	$V_{CC} = 2.7$ to 5.5 V	40	—	—	ns	
				100	—	—		
External clock rise time	t_{CPr}	OSC ₁	$V_{CC} = 2.7$ to 5.5 V	—	—	20	ns	
				—	—	20		
External clock fall time	t_{CPf}	OSC ₁	$V_{CC} = 2.7$ to 5.5 V	—	—	20	ns	
				—	—	20		

Table 14-9 Control Signal Timing (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{disp} = V_{CC} - 40$ to V_{CC} , $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
RES pin pulse width (low)	t_{REL}	RES	$V_{CC} = 2.7$ to 5.5 V	10	—	—	ϕ	Figure 14-2
IRQ pin pulse width (high)	t_{IH}	IRQ ₀ to IRQ ₅	$V_{CC} = 2.7$ to 5.5 V	2	—	—	ϕ ϕ_{SUB}	Figure 14-3
IRQ pin pulse width (low)	t_{IL}	IRQ ₀ to IRQ ₅	$V_{CC} = 2.7$ to 5.5 V	2	—	—	ϕ ϕ_{SUB}	
EVENT pin pulse width (high)	t_{EVH}	EVENT	$V_{CC} = 2.7$ to 5.5 V	2	—	—	ϕ	Figure 14-4
EVENT pin pulse width (low)	t_{EVL}	EVENT	$V_{CC} = 2.7$ to 5.5 V	2	—	—	ϕ	
UD pin minimum change width	t_{UDH} t_{UDL}	UD	$V_{CC} = 2.7$ to 5.5 V	2	—	—	ϕ	Figure 14-5

Table 14-10 Serial Interface Timing

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{disp} = V_{CC} - 40$ to V_{CC} , $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
Output transfer clock cycle timing	t_{scyc}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	2	—	—	ϕ	Figure 14-6
Output transfer clock pulse width (high)	t_{SCKH}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	0.4	—	—	t_{scyc}	
Output transfer clock pulse width (low)	t_{SCKL}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	0.4	—	—	t_{scyc}	
Output transfer clock rise time	t_{SCKr}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	60	ns	
Output transfer clock fall time	t_{SCKf}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	60	ns	
Input transfer clock cycle timing	t_{scyc}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	1	—	—	ϕ	
Input transfer clock pulse width (high)	t_{SCKH}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	0.4	—	—	t_{scyc}	

Table 14-10 Serial Interface Timing (cont)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{disp} = V_{CC} - 40$ to V_{CC} , $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Reference Diagram
				Min	Typ	Max		
Input transfer clock pulse width (low)	t_{SCKL}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	0.4	—	—	t_{scyc}	Figure 14-6
Input transfer clock rise time	t_{SCKr}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	60	ns	
				—	—	80		
Input transfer clock fall time	t_{SCKf}	SCK ₁ , SCK ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	60	ns	
				—	—	80		
Serial output data delay time	t_{dSO}	SO ₁ , SO ₂	$V_{CC} = 2.7$ to 5.5 V	—	—	200	ns	
				—	—	350		
Serial input data setup time	t_{sSI}	SI ₁ , SI ₂	$V_{CC} = 2.7$ to 5.5 V	230	—	—	ns	
				470	—	—		
Serial input data hold time	t_{hSI}	SI ₁ , SI ₂	$V_{CC} = 2.7$ to 5.5 V	230	—	—	ns	
				470	—	—		
Transfer hold time	t_{SCK2}	SCK ₂	When pin SCK ₂ is input pin $V_{CC} = 2.7$ to 5.5 V	0.2	—	40	μs	Figure 14-7
				0.4	—	40		
				—	—	1	t_{scyc}	
Transfer end acknowledge time	t_{CS}	\overline{CS}	$V_{CC} = 2.7$ to 5.5 V	3	—	4	ϕ	

14.3.3 HD6433723, HD6433724, HD6433725, and HD6433726 A/D Converter Characteristics

Table 14-11 gives the HD6433723, HD6433724, HD6433725, and HD6433726 A/D converter characteristics.

Table 14-11 A/D Converter Characteristics (provisional values)

Conditions: Unless otherwise indicated, $V_{CC} = 4.0$ to 5.5 V, $V_{disp} = V_{CC} - 40$ to V_{CC} , $V_{SS} = 0.0$ V, $T_a = -20$ to $+75^\circ\text{C}$

Item	Symbol	Applicable Pins	Test Conditions	Rating			Unit	Notes
				Min	Typ	Max		
Analog supply voltage	AV_{CC}	AV_{CC}		$V_{CC} - 0.3$	V_{CC}	$V_{CC} + 0.3$	V	
Analog input voltage	AV_{IN}	AN_0 to AN_7		AV_{SS}	—	AV_{CC}	V	
Analog current	AI_{CC}	AV_{CC}	$AV_{CC} = 5$ V	—	—	200	μA	
	AI_{STOP}		Reset and power-down mode	—	—	10	μA	
Analog input capacitance	C_{AIN}	AN_0 to AN_7		—	—	30	pF	
Allowable signal source impedance	R_{AIN}	AN_0 to AN_7		—	—	10	$\text{k}\Omega$	
Resolution				—	—	8	Bit	
Absolute precision			$V_{CC} = AV_{CC} = 5$ V	—	—	± 2.5	LSB	Reference value
			$V_{CC} = AV_{CC} = 4.0$ to 5.5 V	—	± 2.5	—		
Conversion time				31	15.5	14.8	μS	

14.4 Operational Timing

This section provides the following timing charts (figures 14-1 to 14-8).

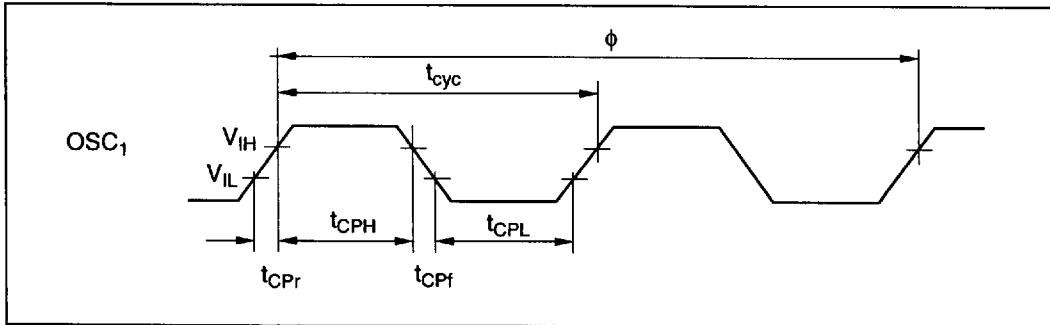


Figure 14-1 System Clock Input Timing

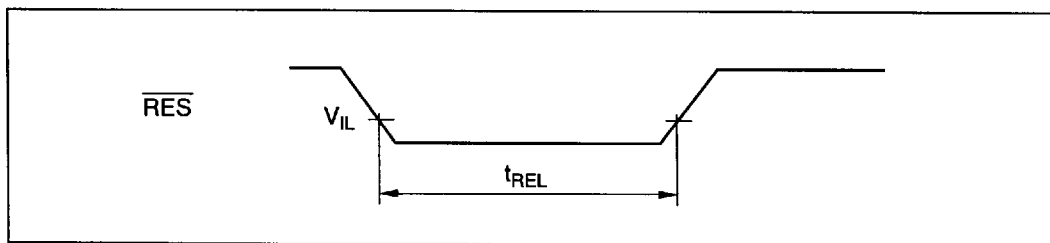


Figure 14-2 \overline{RES} Pin Pulse Width (low)

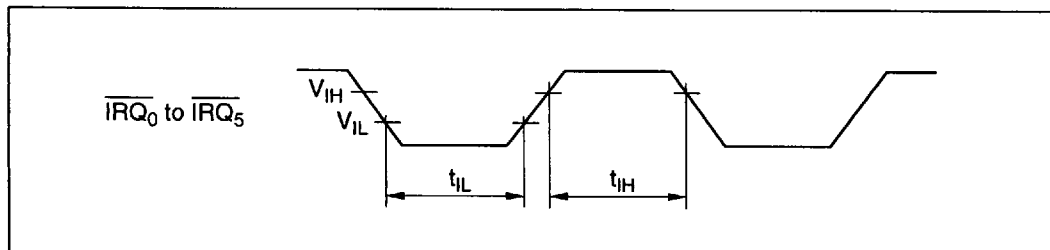


Figure 14-3 \overline{IRQ} Pin Input Timing

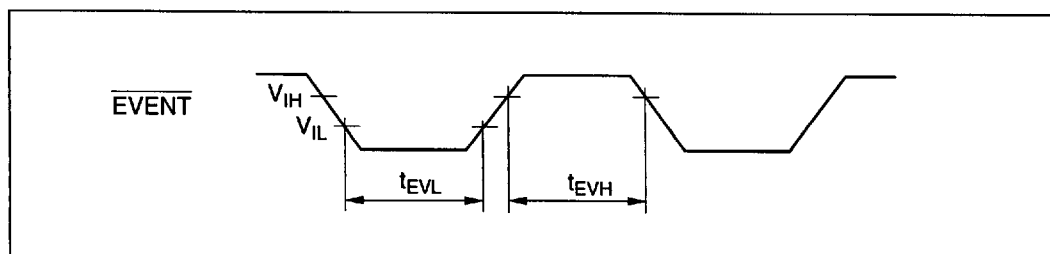


Figure 14-4 \overline{EVENT} Pin Minimum Pulse Width

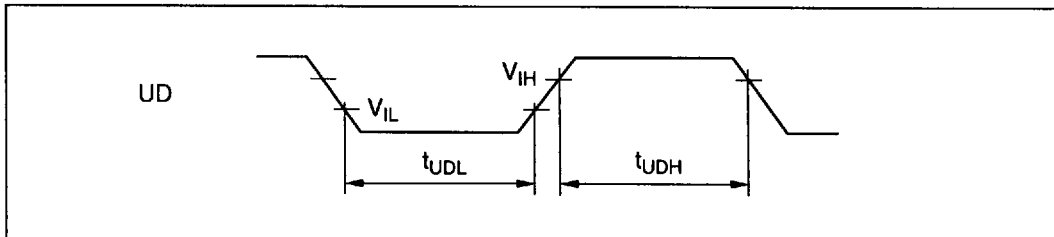


Figure 14-5 UD Pin Minimum Change Width

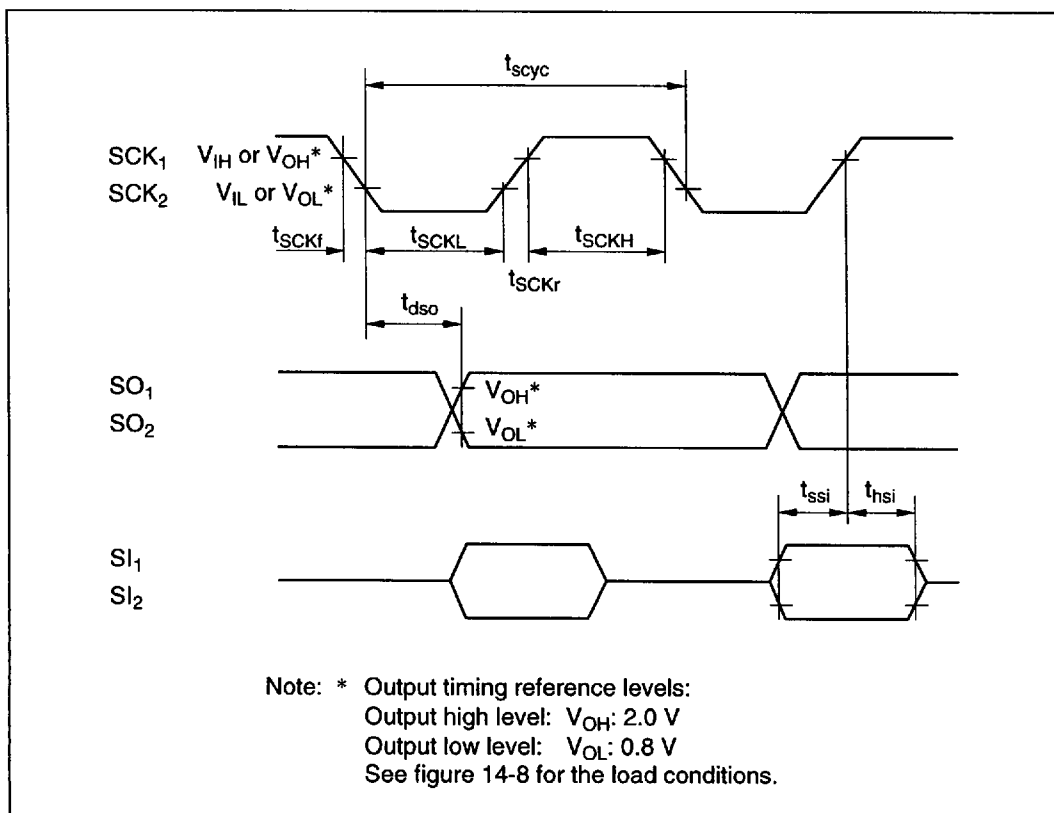


Figure 14-6 SCI I/O Timing

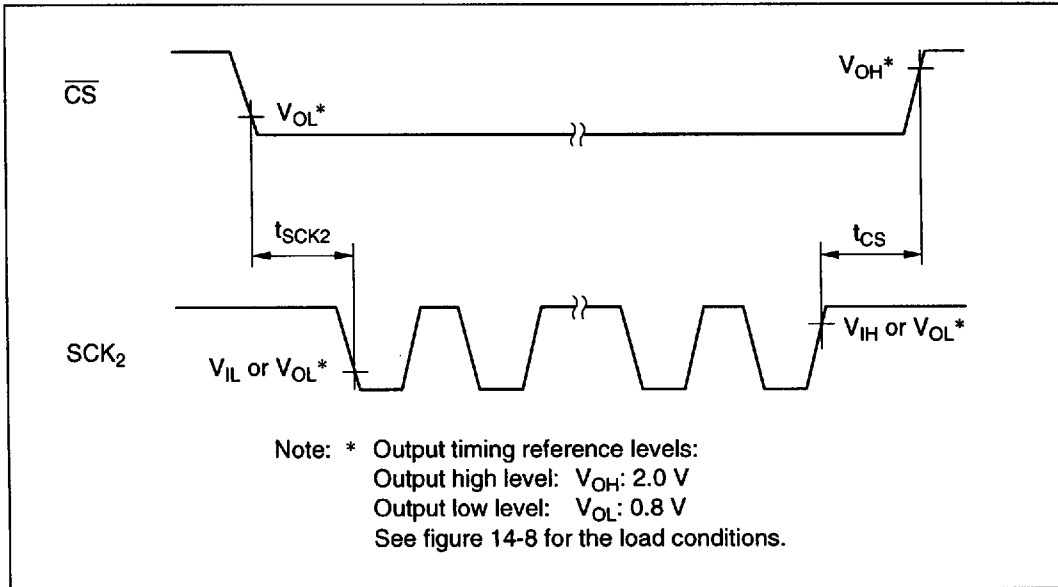


Figure 14-7 Serial Communication Interface 2 Chip Select Timing

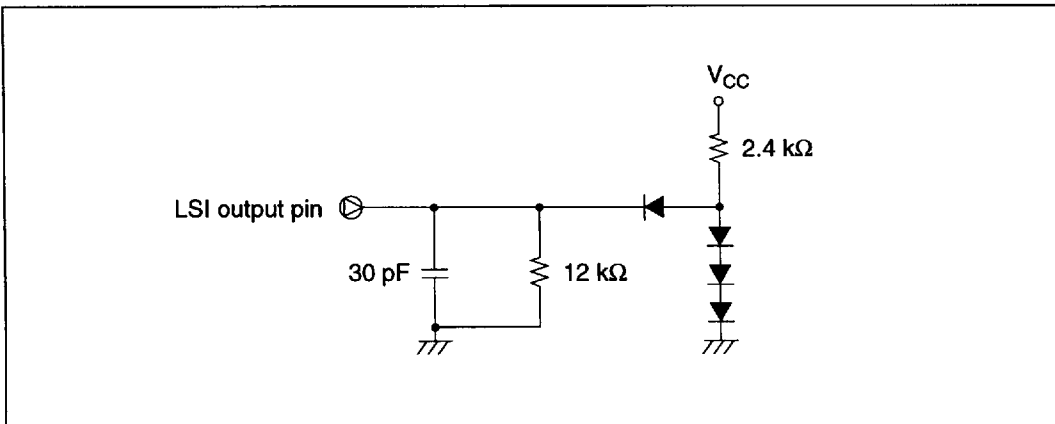


Figure 14-8 Output Load Conditions

14.5 Differences in Electrical Characteristics between Mask ROM and ZTAT™ Versions

Table 14-12 shows the difference in electrical characteristics between HD6473724/HD6473726 and HD6433723/HD6433724/HD6433725/HD6433726.

Table 14-12 Differences in Electrical Characteristics between Mask ROM and ZTAT™ Versions

Item	Symbol	Applicable Pins	Test Conditions	Mask ROM Version			ZTAT™ Version			Unit
				Min	Typ	Max	Min	Typ	Max	
Operation range in subactive mode		V _{CC}		2.5	—	5.5	2.7	—	5.5	V
Input leakage current	I _{IL}	RES		—	—	1	—	—	40	μA
Input capacitance	C _{IN}	P16/EVENT		—	—	15	—	—	35	pF
		P17/V _{disp}		—	—	30	—	—	20	
		RES		—	—	15	—	—	70	
Power dissipation when CPU operating in active mode	I _{OPe}	V _{CC}	V _{CC} = 5 V, f _{OSC} = 8 MHz	—	15	—	—	17	—	mA
			V _{CC} = 5 V, f _{OSC} = 4 MHz	—	8	—	—	9	—	
			V _{CC} = 3 V, f _{OSC} = 4 MHz	—	5	—	—	6	—	
Power dissipation during reset in active mode	I _{RES}	V _{CC}	V _{CC} = 5 V, f _{OSC} = 8 MHz	—	5	8	—	6	9	mA
			V _{CC} = 5 V, f _{OSC} = 4 MHz	—	2.5	4	—	3	5	
			V _{CC} = 3 V, f _{OSC} = 4 MHz	—	1.3	—	—	1.5	—	
Power dissipation in sleep mode	I _{SLEEP}	V _{CC}	V _{CC} = 5 V, f _{OSC} = 8 MHz	—	2	3	—	2.5	3.5	
			V _{CC} = 5 V, f _{OSC} = 4 MHz	—	1	1.5	—	1.5	2	
			V _{CC} = 3 V, f _{OSC} = 4 MHz	—	0.6	—	—	1	—	

Table 14-12 Differences in Electrical Characteristics between HD6473724 and HD6433723/HD6433724 (cont)

Item	Symbol	Applicable Pins	Test Conditions	Mask ROM Version			ZTAT™ Version			Unit
				Min	Typ	Max	Min	Typ	Max	
Power dissipation in subactive mode	I_{SUB}	V_{CC}	$V_{CC} = 2.5\text{ V}$ (no bypass capacitor)	—	5	20				μA
			$V_{CC} = 2.5\text{ V}$ (47 μF bypass capacitor)	—	9	—				
			$V_{CC} = 2.7\text{ V}$ (no bypass capacitor)				—	6	20	
			$V_{CC} = 2.7\text{ V}$ (47 μF bypass capacitor)				—	11	—	
			$V_{CC} = 5\text{ V}$ (no bypass capacitor)	—	13	—	—	16	—	
			$V_{CC} = 5\text{ V}$ (47 μF bypass capacitor)	—	20	—	—	22	—	
Power dissipation in watch mode	I_{WATCH}	V_{CC}	$V_{CC} = 2.5\text{ V}$ (no bypass capacitor)	—	2.2	5				μA
			$V_{CC} = 2.5\text{ V}$ (47 μF bypass capacitor)	—	2.8	—				
			$V_{CC} = 2.7\text{ V}$ (no bypass capacitor)				—	3.2	6	
			$V_{CC} = 2.7\text{ V}$ (47 μF bypass capacitor)				—	3.8	—	
			$V_{CC} = 5\text{ V}$ (no bypass capacitor)	—	6	—	—	10	—	
			$V_{CC} = 5\text{ V}$ (47 μF bypass capacitor)	—	8	—	—	12	—	
Power dissipation in standby mode	I_{STBY}	V_{CC}		—	—	5	—	—	10	μA